REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-02-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A									
	PAGE		1	2	3	4	5	6	7	8	9	10	11									

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO**
Original date of drawing YY MM DD 07-03-20	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, LOW-POWER SINGLE SCHMITT TRIGGER BUFFER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/07623**
	REV A	**PAGE** 1 **OF** 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low-power single Schmitt trigger buffer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07623	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AUP1G17-EP	Low-power single Schmitt Trigger buffer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	MO-203	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 4.6 V
Input voltage range (V_I) ..... -0.5 V to 4.6 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O) ..... -0.5 V to 4.6 V
Voltage range applied to any output in the high or low state (V_O) ..... -0.5 V to V_{CC} +0.5 V 2/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) ..... ±20 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}), Case outline X ..... 227°C/W 3/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 4/

Supply voltage (V_{CC}) ..... 0.8 V to 3.6 V
Input voltage (V_I) ..... 0 V to 3.6 V
Output voltage (V_O) ..... 0 to V_{CC}
Maximum high level output current (I_{OH}):
V_{CC} = 0.8 V ..... -20 µA
V_{CC} = 1.1 V ..... -1.1 mA
V_{CC} = 1.4 V ..... -1.7 mA
V_{CC} = 1.65 V ..... -1.9 mA
V_{CC} = 2.3 V ..... -3.1 mA
V_{CC} = 3 V ..... -4 mA
Maximum low level output current (I_{OL}):
V_{CC} = 0.8 V ..... 20 µA
V_{CC} = 1.1 V ..... 1.1 mA
V_{CC} = 1.4 V ..... 1.7 mA
V_{CC} = 1.65 V ..... 1.9 mA
V_{CC} = 2.3 V ..... 3.1 mA
V_{CC} = 3 V ..... 4 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figures 5 and 6.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits		Unit
					Min	Max	
Positive going input threshold volatge		V_{T+}		0.8 V	0.3	0.6	V
				1.1 V	0.53	0.9	
				1.4 V	0.74	1.11	
				1.65 V	0.91	1.29	
				2.3 V	1.37	1.77	
				3.0 V	1.88	2.29	
Negative going input threshold volatge		V_{T+}		0.8 V	0.1	0.6	V
				1.1 V	0.26	0.65	
				1.4 V	0.39	0.75	
				1.65 V	0.47	0.84	
				2.3 V	0.69	1.04	
				3.0 V	0.88	1.24	
Hysteresis (V_{T+} - V_{T-})		ΔV_T		0.8 V	0.07	0.5	V
				1.1 V	0.08	0.46	
				1.4 V	0.18	0.56	
				1.65 V	0.27	0.66	
				2.3 V	0.53	0.92	
				3.0 V	0.79	1.31	
High level output voltage		V_{OH}	I_{OH} = -20 μA	0.8 V to 3.6 V	V_{CC} – 0.2		V
			I_{OH} = -1.1 mA	1.1 V	0.7 x V_{CC}		
			I_{OH} = -1.7 mA	1.4 V	1.03		
			I_{OH} = -1.9 mA	1.65 V	1.3		
			I_{OH} = -2.3 mA	2.3 V	1.97		
			I_{OH} = -3.1 mA		1.85		
			I_{OH} = -2.7 mA	3 V	2.67		
			I_{OH} = -4 mA		2.55		
Low level output voltage		V_{OL}	I_{OH} = 20 μA	0.8 V to 3.6 V		0.1	V
			I_{OH} = 1.1 mA	1.1 V		0.3 x V_{CC}	
			I_{OH} = 1.7 mA	1.4 V		0.37	
			I_{OH} = 1.9 mA	1.65 V		0.35	
			I_{OH} = 2.3 mA	2.3 V		0.33	
			I_{OH} = 3.1 mA			0.45	
			I_{OH} = 2.7 mA	3 V		0.33	
			I_{OH} = 4 mA			0.475	
Input current	All input	I_I	V_I = GND to 3.6 V	0 to 3.6 V		0.5	μA

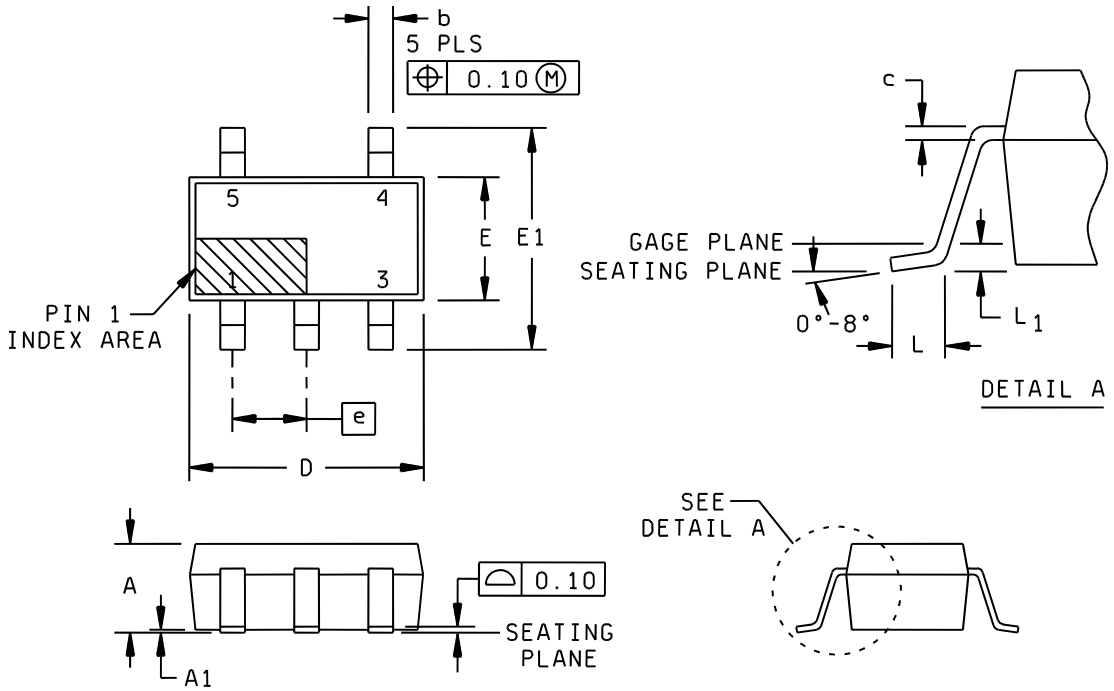
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits Min	Limits Max	Unit
Off current	I_{off}	V_I or V_O = 0 V to 3.6 V	0 V		5.0	µA
	ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V		5.0	µA
Supply current	I_{CC}	V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V		0.9	µA
	ΔI_{CC}	Vi = V_{CC} – 0.6 V, I_O = 0	3.3 V		50	µA
Input capacitance	C_i		0 V	1.5 Typ		pF
			3.6 V	1.5 Typ		
Output capacitance	C_o			2.5 Typ		
Switching characteristics						
Propagation delay from input A to output Y		CL = 50 pF See figure 5 and 6	1.2 V ±0.1 V	7.5	28	ns
			1.5 V ±0.1 V	5.6	20	
			1.8 V ±0.15 V	4.8	17	
			2.5 V ±0.2 V	4	13	
			3.3 V ±0.3 V	3.6	11	
Operating characteristic						
Power dissipation capacitance	C_{PD}	T_A = 25°C, f = 10 MHz	0.8 V	4 Typ		pF
			1.2 V ±0.1 V	4 Typ		
			1.5 V ±0.1 V	4 Typ		
			1.8 V ±0.15 V	4 Typ		
			2.5 V ±0.2 V	4.2 Typ		
			3.3 V ±0.3 V	4.4 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 NOM	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
4. Falls within JEDEC MO-203 variation AA.

FIGURE 1. Case outline - Continued.

Case X

Terminal number	Terminal symbol
1	NC
2	A
3	GND
4	Y
5	V_{CC}

NC = Not internal connection

FIGURE 2. Terminal connections.

Input A	Output Y
H	H
L	L

FIGURE 3. Function table.

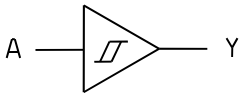
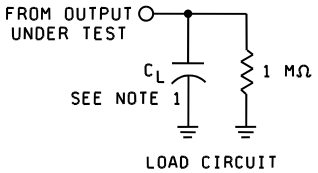
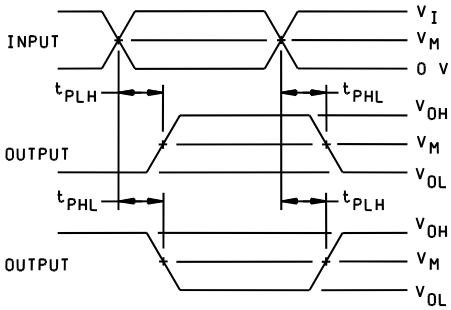


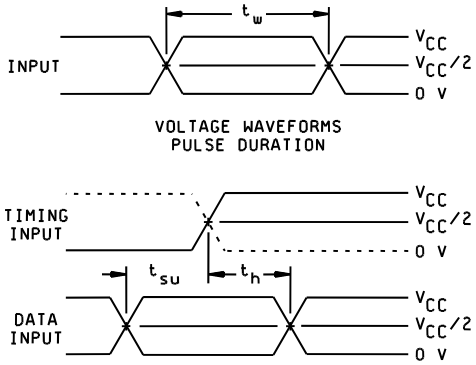
FIGURE 4. Logic diagram.



	V_{CC}=0.8 V	V_{CC}=1.2 V ±0.1 V	V_{CC}=1.5 V ±0.1 V	V_{CC}=1.8 V ±0.15 V	V_{CC}=2.5 V ±0.2 V	V_{CC}=3.3 V ±0.3 V
C_L	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

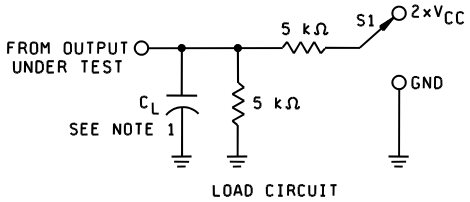


Propagation delays, setup and hold times, and pulse width

NOTES:

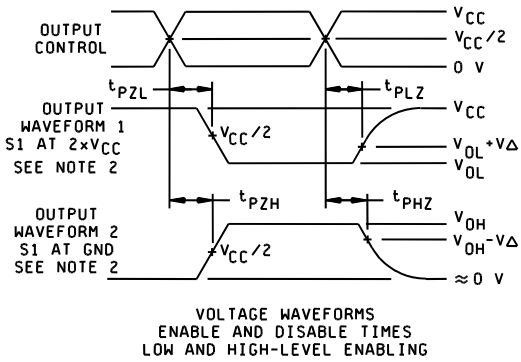
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
3. The outputs are measured one at a time with one input transition per measurement.
4. t_{PHL} and t_{PLH} are the same as t_{pd}.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	V_{CC}=0.8 V	V_{CC}=1.2 V ±0.1 V	V_{CC}=1.5 V ±0.1 V	V_{CC}=1.8 V ±0.15 V	V_{CC}=2.5 V ±0.2 V	V_{CC}=3.3 V ±0.3 V
C_L	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF	5,10,15,30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



Enable and disable times

NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. All parameters and waveforms are not applicable to all devices.

FIGURE 6. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking 2/
V62/07623-01XE	01295	SN74AUP1G17MDCKREP	BZU

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The actual top side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly.test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493