REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. - PHN	07-11-06	Thomas M. Hess
B	Add device type 03. - PHN	07-11-27	Thomas M. Hess
C	Add test conditions to the “P-channel MOSFET current limit” test under Table I. Add footnote 4/ under paragraph 1.4. Update document paragraphs to current requirements. - ro	14-11-21	Charles F. Saffle
D	Under the Operating quiescent current test in Table I for device type 01 only, delete 26 μA and replace with 29 μA. Add terminal pin descriptions to Figure 2. Update document paragraphs to current requirements. - ro	20-01-14	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV	D	D	D	D	D	D	D	D	D	D	D								
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 07-03-20	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, 17 V, 1.5 A SYNCHRONOUS STEP-DOWN CONVERTER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07622**
	REV **D**	**PAGE** 1 **OF** 11

AMSC N/A

5962-V121-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 17 V, 1.5 A synchronous step-down converter microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07622	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device	Generic	Output voltage	Circuit function
01	TPS62110-EP	Adjustable 1.2 V to 16 V	17-V, 1.5 A synchronous step-down converter
02	TPS62111-EP	3.3 V	17-V, 1.5 A synchronous step-down converter
03	TPS62112-EP	5.0 V	17-V, 1.5 A synchronous step-down converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-220	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage at VIN, VINA (V_{CC}) ..... -0.3 V to 20.0 V
Voltage at SW (V_I) ..... -0.3 V to V_I
Voltage at EN, SYNC, LBO, PG (V_I) ..... -0.3 V to 20.0 V
Voltage at LBI, FB (V_I) ..... -0.3 V to 7.0 V
Output current at SW (I_O) ..... 2400 mA
Maximum junction temperature (T_J) ..... 150°C 2/
Storage temperature (T_{STG}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 in) from case for 10 seconds ..... 300°C

Dissipation rating 3/

Case outline	$T_A \leq 25°C$ Power rating	Derating factor above $T_A = 25°C$	$T_A = 70°C$ Power rating	$T_A = 85°C$ Power rating
X	2.5 W	25 mW/°C	1.375 W	1 W

1.4 Recommended operating conditions. 4/

Supply voltage at VIN, VINA (V_{CC}) ..... 3.1 V to 17 V
Maximum voltage at power good, LBO, EN, SYNC ..... 17.0 V
Operating junction temperature (T_J) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Long term high temperature storage and/or extended used at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer for additional information about enhanced plastic packaging.
3/ Based on a thermal resistance of 40 K/W soldered onto a high K board.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Supply current						
Input voltage range 3/	V_I		All	3.1	17	V
Operating quiescent current	$I_{(Q)}$	I_O = 0 mA, SYNC = GND, 4/ V_I = 7.2 V, T_A = 25°C	All	20 typical		µA
		I_O = 0 mA, SYNC = GND, 4/ V_I = 17 V	01, 02, 03		29	
Shutdown current	$I_{(SD)}$	EN = GND	All		5	µA
		EN = GND, V_I = 7.2 V, T_A = 25°C			3	
Enable						
EN high level input voltage	V_{IH}		All	1.3		V
EN low level input voltage	V_{IL}		All		0.3	V
EN trip point hysteresis			All	170 typical		mV
EN input leakage current	I_{IKG}	EN = GND or V_I, V_I = 17 V	All		0.2	µA
EN input current	$I_{(EN)}$	0.6 V ≤ $V_{(EN)}$ ≤ 4 V	All	10 typical		µA
Undervoltage lockout threshold	$V_{(UVLO)}$	Input voltage falling	All	2.8	3.1	V
Undervoltage lockout hysteresis			All	250 typical		mV
Power switch						
P-channel MOSFET on resistance	$r_{DS(ON)}$	V_I ≥ 5.4, I_O = 350 mA	All		250	mΩ
		V_I = 3.5 V, I_O = 200 mA		340 typical		
		V_I = 3 V, I_O = 100 mA		490 typical		
P-channel MOSFET leakage current		V_{DS} = 17 V	All		1	µA
P-channel MOSFET current limit		V_I = 7.2 V, V_O = 3.3 V	All	2400 typical		mA
N-channel MOSFET on resistance	$r_{DS(ON)}$	V_I ≥ 5.4, I_O = 350 mA	All		200	mΩ
		V_I = 3.5 V, I_O = 200 mA		170 typical		
		V_I = 3 V, I_O = 100 mA		200 typical		
N-channel MOSFET leakage current		V_{DS} = 17 V	All		3	µA
Power good output low battery input (LBI), low battery output (LBO)						
PG trip voltage	$V_{(PG)}$		All	V_O – 1.6% typical		V
PG delay time		V_O ramping positive	All	50 typical		µs
		V_O ramping negative		200 typical		
PG, LBO output low voltage	V_{OL}	V_{FB} = 1.1 x V_O nominal, I_{OL} = 1 mA	All		0.3	V

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Power good output LBI, LBO – continued.						
PG, LBO sink current	I_{OL}		All	1 typical		mA
PG, LBO output leakage current		V_{FB} = V_O nominal	All		0.25	µA
Minimum supply voltage for valid PG, LBI, LBO signal			All	3 typical		V
LBI trip voltage	V_{LBI}	Input voltage falling	All	1.256 typical		V
LBI input leakage current	I_{LBI}		All		100	nA
LBI trip point accuracy			All	1.5%		
LBI hysteresis	$V_{LBI,HYS}$		All	25 typical		mV
Oscillator						
Oscillator frequency	f_S		All	900	1100	kHz
Synchronization range	$f_{(SYNC)}$	CMOS logic clock signal on SYNC pin	All	800	1400	kHz
SYNC high level input voltage	V_{IH}		All	1.5		V
SYNC low level input voltage	V_{IL}		All		0.3	V
SYNC input leakage current	I_{lkg}	SYNC = gnd or V_{IN}	All		0.2	µA
SYNC trip point hysteresis			All	170 typical		mV
SYNC input current		0.6 V ≤ $V_{(SYNC)}$ ≤ 4 V	All		20	µA
Duty cycle of external clock signal			All	30%	90%	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output						
Adjustable output voltage range 3/	V_O		01	1.153	16	V
FB voltage	V_{FB}		01	1.153 typical		V
FB leakage current			01		100	nA
FB voltage tolerance 4/		V_I = 3.1 V to 17 V, 0 mA < I_O < 1500 mA 5/	01	-6	6	%
Fixed output voltage tolerance 6/		V_I = 3.8 V to 17 V, 0 mA < I_O < 1500 mA 5/	02	-7	7	
		V_I = 5.5 V to 17 V, 0 mA < I_O < 1500 mA 5/	03	-7	7	
Maximum output current	I_O	$V_I \geq 3$ V (once undervoltage lockout voltage exceeded)	All	100 typical		mA
		$V_I \geq 3.5$ V		500 typical		
		$V_I \geq 4.3$ V		1200 typical		
		$V_I \geq 6$ V		1500 typical		
Current into internal voltage divider for fixed voltage versions			All	5 typical		µA
Efficiency	η	$V_I \geq 7.2$ V, V_O = 3.3 V, I_O = 600 mA	All	92% typical		
		$V_I \geq 12$ V, V_O = 5 V, I_O = 600 mA				
Duty cycle range for main switches		At 1 MHz	All	10%	100%	
Minimum t_{on} time for main switch			All	100 typical		ns
Shutdown temperature			All	145 typical		°C
Startup time		I_O = 800 mA, V_I = 12 V, V_O = 3.3 V	All	1 typical		ms

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_I = 12 V, V_O = 3.3 V, I_O = 600 mA, EN = V_I, T_A = T_J = -55°C to 125°C.

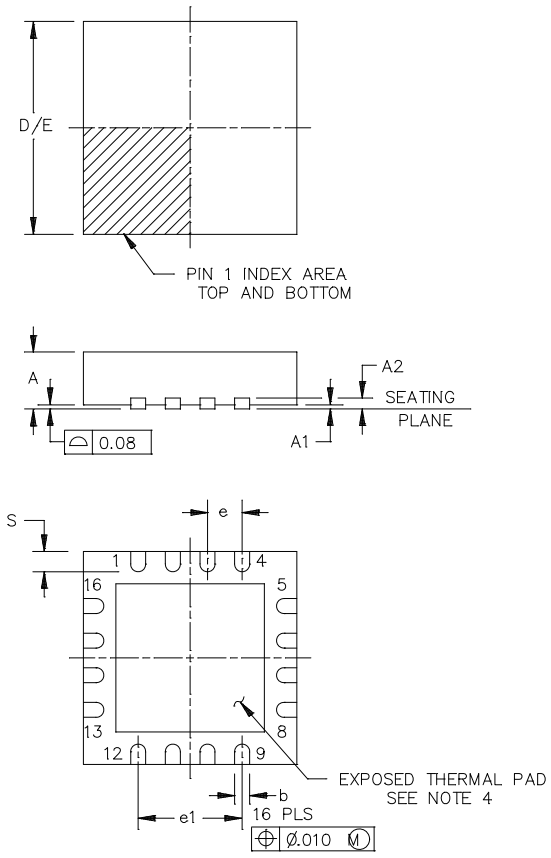
3/ Not production tested.

4/ Device is not switching.

5/ The maximum output current depends on the input voltage.

6/ The output voltage accuracy includes line and load regulation over the full temperature range T_A = -55°C to 125°C. See the section for no-load operation in the manufacturer data.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	3.85	4.15
A1	0.00	0.05	e	0.65 BSC	
A2	0.20 REF		e1	1.95 BSC	
b	0.23	0.38	S	0.30	0.50

Notes:
1. All liner dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Quad flatpack, no leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance. See manufacturer data for details regarding the exposed thermal pad dimensions.
5. Falls within JEDEC MO-220.

FIGURE 1. Case outline.

Device types	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	PGND	I	Power ground. Connect all power grounds to this pin.
2	VIN	I	Supply voltage input (power stage).
3	VIN	I	Supply voltage input (power stage).
4	EN	I	Enable. A logic high enables the converter; logic low forces the device into shutdown mode reducing the supply current to less than 2 µA.
5	SYNC	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = HIGH: Low-noise mode enabled, fixed frequency PWM operation is forced SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled
6	LBO	O	Open-drain, low-battery output. This pin is pulled low if LBI is below its threshold.
7	LBI	I	Low-battery input.
8	VINA	I	Supply voltage input (support circuits).
9	AGND	I	Analog ground, connect to GND and PGND.
10	FB	I	Feedback pin for the fixed output voltage option. For the adjustable version, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
11	GND	I	Ground.
12	GND	I	Ground.
13	PG	O	Power good comparator output. This is an open-drain output. A pullup resistor should be connected between PG and VOUT. The output goes active high when the output voltage is greater than 98.4% of the nominal value.
14	SW	O	Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
15	SW	O	Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
16	PGND	I	Power ground. Connect all power grounds to this pin.
Thermal pad			Connect to AGND.

FIGURE 2. Terminal connections.

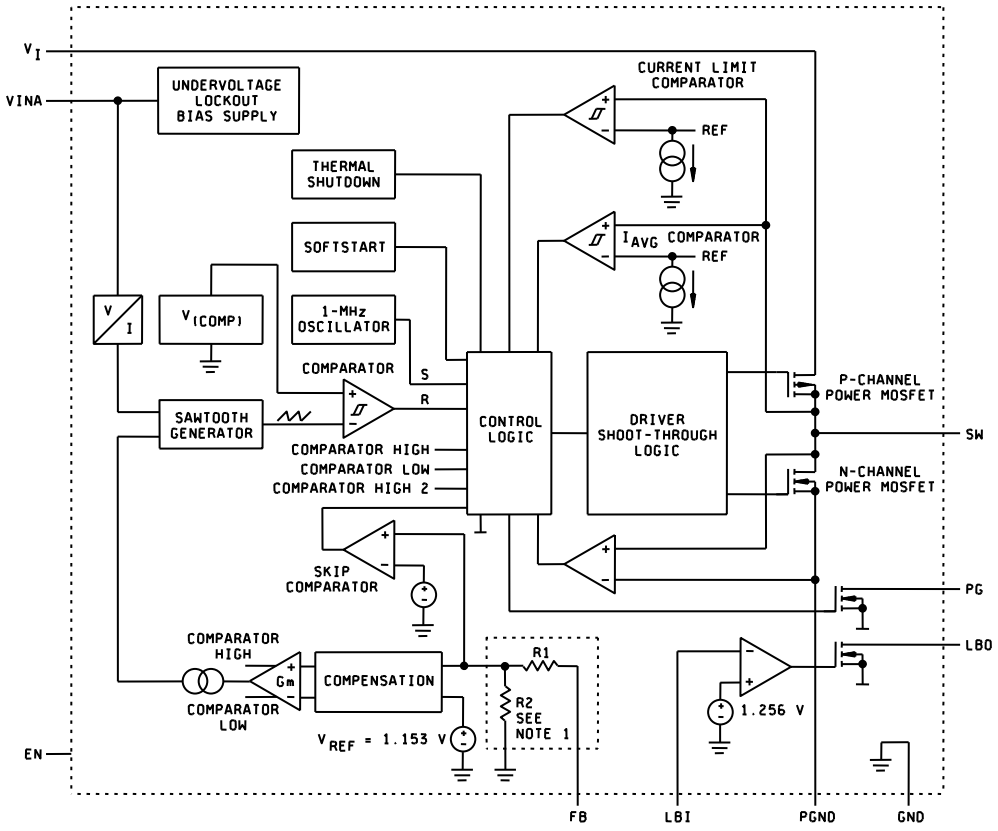


FIGURE 3. Functional block diagram.

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		REV D	PAGE 10

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/07622-01XE	01295	TPS62110-EP	TPS62110MRSAREP
V62/07622-02XE	01295	TPS62111-EP	TPS62111MRSAREP
V62/07622-03XE	01295	TPS62112-EP	TPS62112MRSAREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243