REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	19-07-10	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	REV			A	A	A	A	A	A	A	A	A	A									
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PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime
Original date of drawing YY-MM-DD 13-07-10	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, LINEAR, HEX INVERTERS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A CODE IDENT. NO. 16236	DWG NO. V62/07619
	REV A	PAGE 1 OF 10

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V046-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Hex inverters microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AHCU04 -EP	Hex Inverters

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7.0 V
Input voltage range (V_I)	-0.5 V to 7.0 V 2/
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V 2/
Input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O = 0$ to V_{CC})	±20 mA
Continuous output current (I_O) ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance (θ_{JA})	113°C/W 3/
Storage temperature range (T_{STG})	-60°C to 150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	2.0 V to 5.5 V
Minimum high level input voltage (V_{IH}):	
V_{CC} = 2.0 V	1.7 V
V_{CC} = 3.0 V	2.4 V
V_{CC} = 5.5 V	4.4 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 2.0 V	0.3 V
V_{CC} = 3.0 V	0.6 V
V_{CC} = 5.5 V	1.1 V
Input voltage (V_I)	0.0 V to V_{CC}
Output voltage (V_O)	0.0 V to V_{CC}
Maximum high level output current (I_{OH}):	
V_{CC} = 2.0 V	-50 µA
V_{CC} = 3.3 ±0.3 V	-4 mA
V_{CC} = 5.0 ±0.5 V	-8 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 2.0 V	50 µA
V_{CC} = 3.3 ±0.3 V	4 mA
V_{CC} = 5.0 ±0.5 V	8 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and voltage waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA	2.0 V	25°C, -55°C to 125°C	All	1.8		V
			3.0 V			2.7		
			4.5 V			4.0		
		I_{OH} = -4 mA	3.0 V	25°C		2.58		
				-55°C to 125°C		2.3		
		I_{OH} = -8 mA	4.5 V	25°C		3.94		
				-55°C to 125°C		3.5		
Low level output voltage	V_{OL}	I_{OL} = 50 μA	2.0 V	25°C	All		0.1	V
				-55°C to 125°C			0.2	
			3.0 V	25°C			0.1	
				-55°C to 125°C			0.3	
			4.5 V	25°C			0.1	
				-55°C to 125°C			0.5	
		I_{OL} = 4 mA	3.0 V	25°C			0.26	
				-55°C to 125°C			0.5	
		I_{OL} = 8 mA	4.5 V	25°C			0.26	
				-55°C to 125°C			0.5	
Input current	I_I	V_I = V_{CC} or GND	0 to 5.5 V	25°C	All		±0.1	μA
				-55°C to 125°C			±1.0	
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	5.5 V	25°C	All		2.0	μA
				-55°C to 125°C			20.0	
Input capacitance	C_I	V_I = V_{CC} or GND	5 V	25°C, -55°C to 125°C	All		10	pF
Power dissipation capacitance	C_{pd}	No load, f = 1 MHz		25°C	All	7.3 typical		pF
Switching characteristics								
Propagation delay time, A to Y	t_{PLH}	C_L = 50 pF, See figure 5	3.3 ±0.3 V	25°C	All	1	10.6	ns
				-55°C to 125°C		1	14	
			5 ±0.5 V	25°C		1	7	
				-55°C to 125°C		1	11	
	t_{PHL}	C_L = 50 pF, See figure 5	3.3 ±0.3 V	25°C	All	1	10.6	ns
				-55°C to 125°C		1	14	
			5 ±0.5 V	25°C		1	7	
				-55°C to 125°C		1	11	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 3/	Limits			Unit
			Min	Typical	Max	
Noise characteristics 4/						
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$			0.5		V
Quiet output, minimum dynamic $V_{OL(V)}$	$V_{OL(V)}$			-0.5		V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$			4.3		V
High level dynamic input voltage $V_{IH(D)}$	$V_{IH(D)}$		4			V
Low level dynamic input voltage $V_{IH(D)}$	$V_{IL(D)}$				1	V

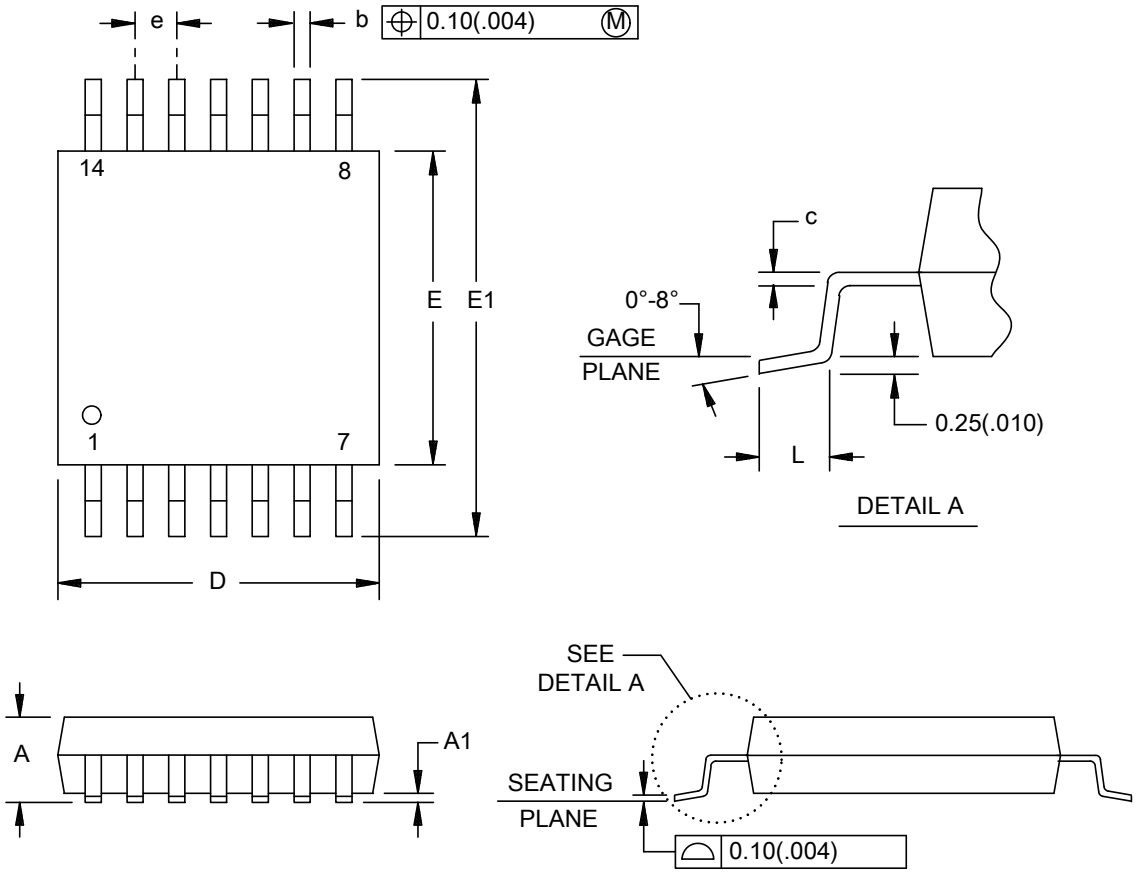
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating temperature range (unless otherwise noted).

3/ V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C.

4/ Characteristics are for surface mount packages only.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. This drawing is subject to change without notice.
3. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
4. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
5. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

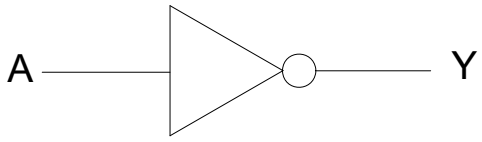
Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	14	V_{CC}
2	1Y	13	6A
3	2A	12	6Y
4	2Y	11	5A
5	3A	10	5Y
6	3Y	9	4A
7	GND	8	4Y

FIGURE 2. Terminal connections.

(Each Inverter)

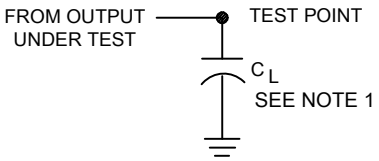
Input A	Output Y
H	L
L	H

FIGURE 3. Function table.

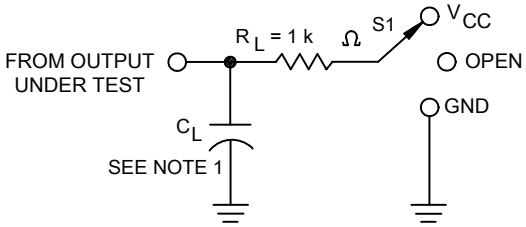


Positive logic

FIGURE 4. Logic diagram.

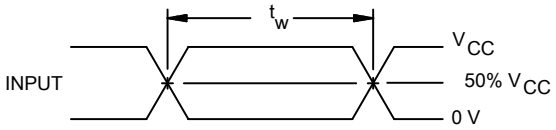


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

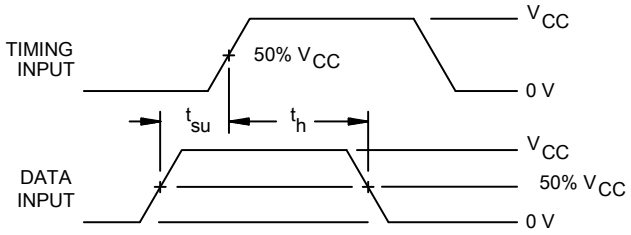


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

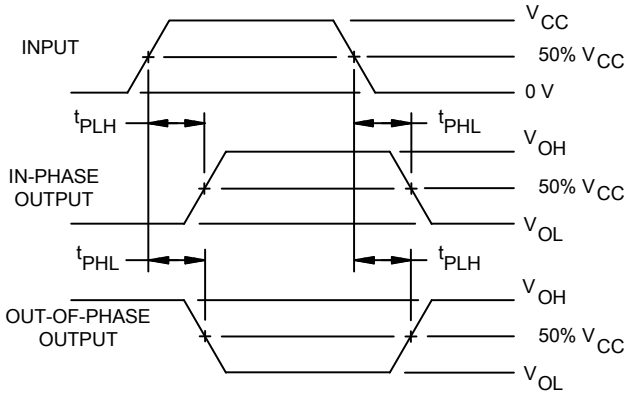
TEST	S1
t_{PLH} /t_{PHL}	OPEN
t_{PLZ} /t_{PZL}	V_{CC}
t_{PHZ} /t_{PZH}	GND
OPEN DRAIN	V_{CC}



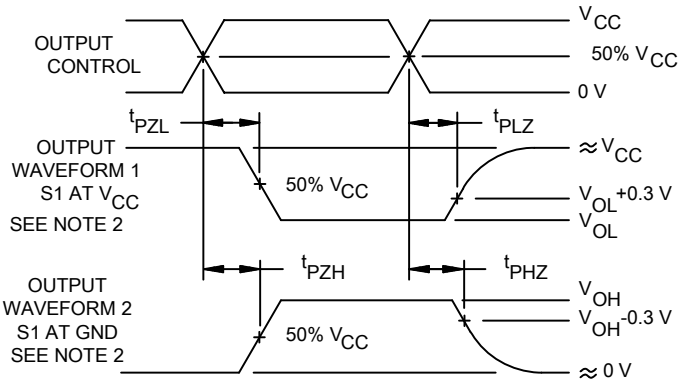
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
4. The output are measured one at a time, with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms..

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/07619-01XE	01295	AHCU04M	SN74AHCU04MPWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243