

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct title in front page and remove footnote 1 in section 1.2.1. - PHN	07-05-02	Thomas M. Hess
B	Make correction to note 5 under figure 1 by deleting MO-187-AA and replacing with MO-153. Updating document paragraphs to current requirements. - ro	14-10-08	Charles F. Saffle

CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

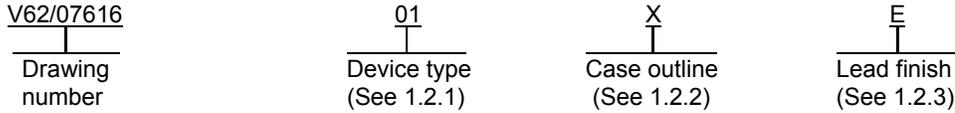
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PMIC N/A	PREPARED BY Phu H. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO
Original date of drawing YY-MM-DD  07-03-12	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, LINEAR, 4.5 V TO 20 V INPUT, 3-A OUTPUT SYNCHRONOUS PWM SWITCHES WITH INTEGRATED, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A	CODE IDENT. NO. 16236
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4.5 V to 20 V input, 3-A output synchronous pulse width modulator (PWM) switches with integrated FET microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device</u>	<u>Generic</u>	<u>Output voltage</u>	<u>Circuit function</u>
01	TPS54352-EP	1.2 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET
02	TPS54353-EP	1.5 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET
03	TPS54354-EP	1.8 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET
04	TPS54355-EP	2.5 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET
05	TPS54356-EP	3.3 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET
06	TPS54357-EP	5.0 V	4.5 V to 20 V input, 3-A output synchronous PWM switches with integrated FET

1.2.2 Case outline(s). The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage range:

(VIN).....	-0.3 V to +21.5 V
(VSENSE) .....	-0.3 V to +8.0 V
(UVLO) .....	-0.3 V to +8.0 V
(SYNC) .....	-0.3 V to +4.0 V
(ENA) .....	-0.3 V to +4.0 V
(BOOT) .....	VI(PH) +8.0 V

Output voltage range, (VO):

(VBIAS) .....	-0.3 V to +8.5 V
(LSG) .....	-0.3 V to +8.5 V
(SYNC) .....	-0.3 V to +4.0 V
(RT) .....	-0.3 V to +4.0 V
(PWRGD) .....	-0.3 V to +6.0 V
(COMP) .....	-0.3 V to +4.0 V
(PH) .....	-1.5 V to +22.0 V

Source current, (I<sub>O</sub>):

(PH) .....	Internally limited (A)
(LSG (steady state current)) .....	10 mA
(COMP, VBIAS) .....	3 mA

Sink current, (I<sub>S</sub>):

(SYNC) .....	5 mA
(LSG (steady state current)) .....	100 mA
(PH (steady state current)) .....	500 mA
(COMP) .....	3 mA
(ENA, PWRGD) .....	10 mA

Voltage differential (AGND to PGND) ..... ±0.3 V

Operating virtual junction temperature range (T<sub>J</sub>) ..... -55°C to +150°C

Storage temperature range (T<sub>STG</sub>)..... -65°C to +150°C

Lead temperature 1.6 mm (1/16 in) from case for 10 s ..... 260°C

Human-Body Model (HBM) ..... 600 V

Charged-Device Model (CDM) ..... 1.5 kV

1.4 Recommended operating conditions.

Input voltage range, (V<sub>I</sub>):

Device type 01 – 05 .....	+4.5 V to +20.0 V
Device type 06 .....	6.65 V to +20.0 V

Operating junction temperature (T<sub>J</sub>) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Schematic diagram. The schematic diagram shall be as specified on figure 3.

3.5.4 Functional Block diagram. The functional block diagram shall be as specified on figure 4.

3.5.5 Falling edge delay time. The falling edge delay time diagram shall be as specified on figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 4.5 V ≤ V <sub>IN</sub> ≤ 20.0 V -55°C ≤ T <sub>J</sub> ≤ 125°C unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Supply current						
Quiescent current	I <sub>Q</sub>	Operating current, PH pin open, no external low side MOSFET, RT = Hi-Z	All	5 typical		mA
		Shutdwon, ENA = 0 V		1 typical		
Start threshold voltage	V <sub>IN</sub>		01-05		4.48	V
			06		6.65	
Stop threshold voltage			01-05	3.69		
			06	5.45		
Hysteresis			01-05	350 typical		mV
			06	600 typical		
Output voltage						
Output voltage	V <sub>O</sub>	T <sub>J</sub> = 25°C, I <sub>O</sub> = 100 mA to 3 A	01	1.88	1.212	V
		I <sub>O</sub> = 100 mA to 3 A		1.176	1.224	
		T <sub>J</sub> = 25°C, I <sub>O</sub> = 100 mA to 3 A	02	1.485	1.515	
		I <sub>O</sub> = 100 mA to 3 A		1.47	1.53	
		T <sub>J</sub> = 25°C, I <sub>O</sub> = 100 mA to 3 A	03	1.782	1.818	
		I <sub>O</sub> = 100 mA to 3 A		1.764	1.836	
		T <sub>J</sub> = 25°C, I <sub>O</sub> = 100 mA to 3 A	04	2.475	2.525	
		I <sub>O</sub> = 100 mA to 3 A		2.45	2.55	
		T <sub>J</sub> = 25°C, V <sub>IN</sub> = 5.5 V to 20 V, I <sub>O</sub> = 100 mA to 3 A	05	3.267	3.333	
		V <sub>IN</sub> = 5.5 V to 20 V, I <sub>O</sub> = 100 mA to 3 A		3.234	3.366	
		T <sub>J</sub> = 25°C, V <sub>IN</sub> = 7.5 V to 20 V, I <sub>O</sub> = 100 mA to 3 A	06	4.95	5.05	
		V <sub>IN</sub> = 7.5 V to 20 V, I <sub>O</sub> = 100 mA to 3 A		4.9	5.1	
Under Voltage Lockout (UVLO)						
Start threshold voltage	UVLO		All		1.25	V
Stop threshold voltage			All	1.02		V
Hysteresis			All	100 typical		mV
Bias voltage (VBIAS)						
Output voltage	VBIAS	I <sub>VBIAS</sub> = 5 mA, V <sub>IN</sub> ≥ 12 V	All	7.5	8.0	V
		I <sub>VBIAS</sub> = 5 mA, V <sub>IN</sub> = 4.5 V		4.4	4.5	
Oscillator (RT)						
Internally set PWM switching frequency		RT grounded	All	200	300	kHz
		RT open		400	600	
Externally set PWM switching frequency			All	425	575	kHz

See footnote at end of table.

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TABLE I. Electrical performance characteristics – Continued.. 1/

Test	Symbol	Test conditions 4.5 V ≤ V <sub>IN</sub> ≤ 20.0 V -55°C ≤ T <sub>J</sub> ≤ 125°C unless otherwise specified	Device type	Limits		Unit
				Min	Max	
<b>Falling-Edge-Triggered Bidirectional Sync System (SYNC)</b>						
SYNC out low to high rise time (10%/90%) <u>2/</u>		25 pf to ground	All		500	ns
SYNC out high to low fall time (10%/90%) <u>2/</u>		25 pf to ground	All		10	ns
Falling edge delay time <u>2/</u>		Delay from rising edge to rising edge of PH pins, see figure 5	All	180 typical		Degree
Minimum input pulse width <u>2/</u>		RT = 100 kΩ	All	100 typical		ns
Delay (falling edge SYNC to rising edge PH) <u>2/</u>		RT = 100 kΩ	All	360 typical		ns
SYNC out high level voltage		50 kΩ resistor to ground, no pullup resistor	All	2.5		V
SYNC out low level voltage			All		0.6	V
SYNC in low level threshold			All	0.8		V
SYNC in high level threshold			All		2.3	V
SYNC in frequency range <u>2/</u>		Percentage of programmed frequency	All	-10%	10%	
				225	770	kHz
<b>Feed Forward Modulator (Internal Signal)</b>						
Modulator gain		V <sub>IN</sub> = 12 V, T <sub>J</sub> = 25°C	All	8		
Modulator gain variation			All	±25%		
Minimum controllable ON time <u>2/</u>			All	180		ns
Maximum duty factor <u>2/</u>		V <sub>IN</sub> = 4.5 V	All	80%		
<b>VSENSE</b>						
Input bias current, Enable (ENA)	VSENSE		All	1 typical		μA
Disable low level input voltage			All		0.5	V
Internal slow-start time (10% to 90%)		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	01	3.2 typical		ms
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		1.6 typical		
		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	02	4 typical		
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		2 typical		
		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	03	4.6 typical		
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		2.3 typical		
		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	04	4.4 typical		
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		2.2 typical		
		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	05	5.9 typical		
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		2.9 typical		
		f <sub>s</sub> = 250 kHz, RT = ground <u>2/</u>	06	5.4 typical		
		f <sub>s</sub> = 500 kHz, RT = Hi-Z <u>2/</u>		2.7 typical		

See footnote at end of table.

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TABLE I. Electrical performance characteristics – Continued.. 1/

Test	Symbol	Test conditions 4.5 V ≤ V <sub>IN</sub> ≤ 20.0 V -55°C ≤ T <sub>J</sub> ≤ 125°C unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Enable (ENA) – continued.						
Pullup current source			All	1.8	10	μA
Pulldown MOSFET		I <sub>I(ENA)</sub> = 1 mA	All	0.1		V
Power Good (PWRGD)						
Power good threshold		Rising voltage	All	97%		
Rising edge delay 2/		f <sub>s</sub> = 250 kHz	All	4 typical		ms
		f <sub>s</sub> = 500 kHz		2 typical		
Output saturation voltage	PWRGD	I <sub>sink</sub> = 1 mA, V <sub>IN</sub> > 4.5 V	All	0.05 typical		V
Output saturation voltage		I <sub>sink</sub> = 100 μA, V <sub>IN</sub> = 0 V	All	0.76 typical		V
Open drain leakage current		Voltage on PWRGD = 6 V	All		3	μA
Current limit						
Current limit		V <sub>IN</sub> = 12 V	All	3.3	6.5	A
Current limit hiccup time 2/		f <sub>s</sub> = 500 kHz	All	4.5 typical		ms
Thermal shutdown						
Thermal shutdown trip point 2/			All	165 typical		°C
Thermal shutdown hysteresis 2/			All	7 typical		°C
Low side MOSFET driver (LSG)						
Turn on rise time, (10%,90%) 2/		V <sub>IN</sub> = 4.5 V, capacitive load = 1000 pF	All	15 typical		ns
Deadtime		V <sub>IN</sub> = 12 V	All	60 typical		ns
Drive ON resistance		V <sub>IN</sub> = 4.5 V sink/source	All	7.5 typical		Ω
		V <sub>IN</sub> = 12 V sink/source		5 typical		
Output power MOSFET (PH)						
Phase node voltage when disabled		DC conditions and no load, ENA = 0 V	All	0.5 typical		V
Voltage drop, low-side FET and diode		V <sub>IN</sub> = 4.5 V, I <sub>dc</sub> = 100 mA	All		1.42	V
		V <sub>IN</sub> = 12 V, I <sub>dc</sub> = 100 mA			1.38	
High side power MOSFET 3/ switch	r <sub>DS(ON)</sub>	V <sub>IN</sub> = 4.5 V, BOOT-PH = 4.5 V, I <sub>O</sub> = 0.5 A	All		300	mΩ
		V <sub>IN</sub> = 12 V, BOOT-PH = 8 V, I <sub>O</sub> = 0.5 A			200	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Specified by design, not production tested.

3/ Resistance from V<sub>IN</sub> to PH pins.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V <sub>IN</sub>	9	VSENSE
2	V <sub>IN</sub>	10	AGND
3	UVLO	11	PGND
4	PWRGD	12	VBIAS
5	RT	13	LSG
6	SYNC	14	PH
7	ENA	15	PH
8	COMP	16	BOOT

FIGURE 2. Terminal connections.

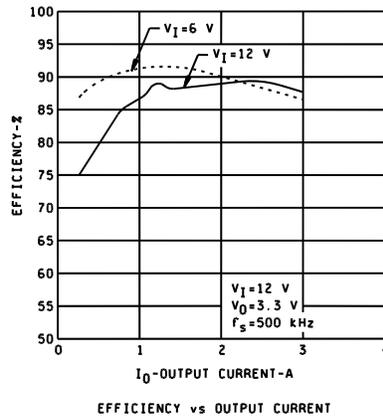
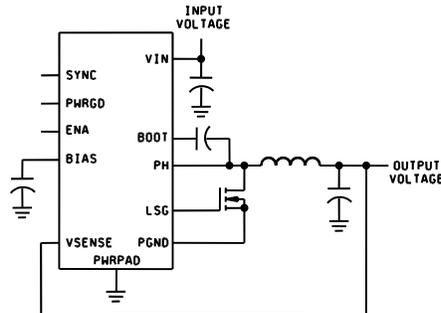


FIGURE 3. Schematic diagram.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07616</b>
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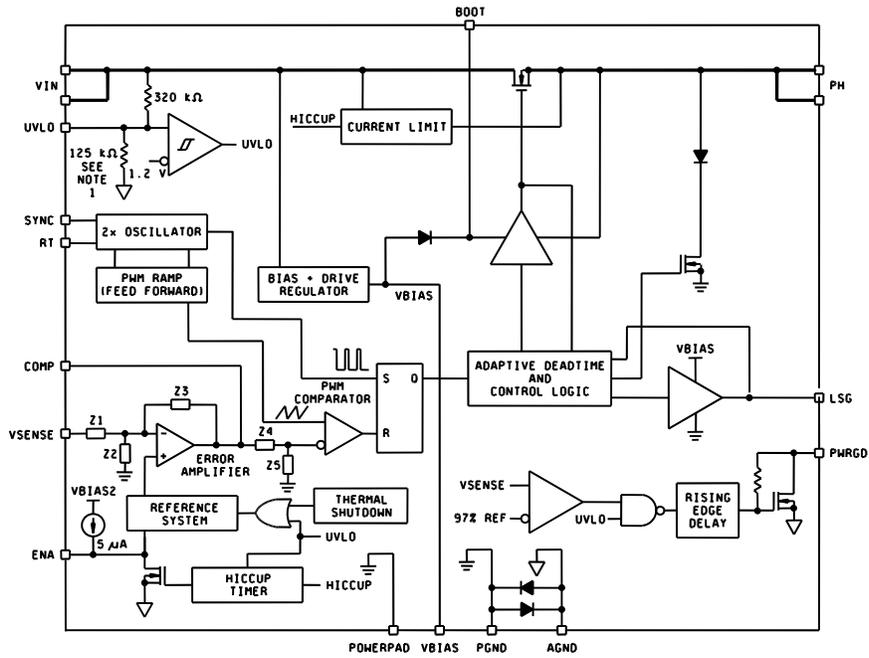


FIGURE 4. Functional block diagram.

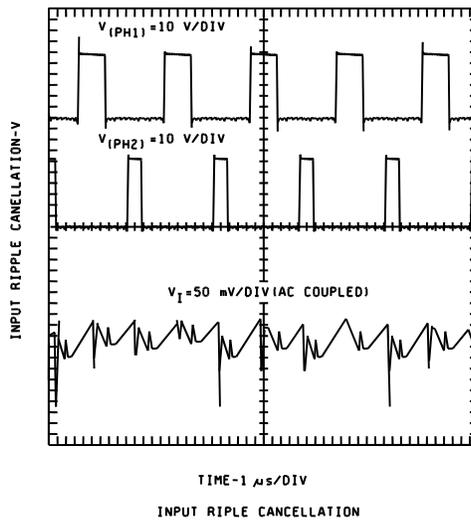


FIGURE 5. Falling edge delay time.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Package marking
V62/07616-01XE	<u>2/</u>	TPS54352MPWPREP	TBD
V62/07616-02XE	<u>2/</u>	TPS54353MPWPREP	TBD
V62/07616-03XE	01295	TPS54354MPWPREP	PMDM
V62/07616-04XE	<u>2/</u>	TPS54355MPWPREP	TBD
V62/07616-05XE	01295	TPS54356MPWPREP	PMEM
V62/07616-06XE	<u>2/</u>	TPS54357MPWPREP	TBD

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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