REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Delete the Dissipation rating table and add paragraph 1.4 Thermal characteristics. Add ASME reference to section 2. Update document paragraphs to current requirements. - ro	14-11-05	C. SAFFLE
B	Add terminal symbol descriptions to Figure 2. Update document paragraphs to current requirements. - ro	19-12-05	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE																						
REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B								
	PAGE			1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 07-02-14	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, TRIPLE-SUPPLY POWER MANAGEMENT IC FOR POWERING FPGAs AND DSPs, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07614**
	REV **B**	**PAGE** 1 **OF** 11

AMSC N/A

5962-V114-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance triple-supply power management integrated circuit (IC) for powering field programmable gate arrays (FPGAs) and digital signal processors (DSPs) microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device	Generic	Output voltage	Circuit function
01	TPS75003-EP	Adjustable	Triple-supply power Management IC for powering FPGAs and DSPs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	Package style
X	20	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

V_{INX} range (IN1, IN2, IN3): ..... -0.3 V to +7.0 V
V_{ENX} range (EN1, EN2, EN3) ..... -0.3 V to V_{INX} + 0.3 V
V_{SWX} range (SW1, SW2, SW3) ..... -0.3 V to V_{INX} + 0.3 V
V_{ISX} range (IS1, IS2, IS3) ..... -0.3 V to V_{INX} + 0.3 V
VOUT3 range ..... -0.3 V to 7.0 V
V_{SSX} range (SS1, SS2, SS3) ..... -0.3 V to V_{INX} + 0.3 V
V_{FBX} range (FB1, FB2, FB3) ..... -0.3 V to +3.3 V
Peak LDO output current (I_{OUT3}) ..... Internally limited
Continuous total power dissipation ..... See paragraph 1.4
Junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
ESD rating, (HBM) ..... 1 kV
ESD rating, CDM ..... 500 V

1.4 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	42.6	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	51.8	°C/W
Thermal resistance, junction-to-board	θ_{JB}	39.5	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.6	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	14.2	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	2.8	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. APPLICABLE DOCUMENTS

AMERICAN SOCIETY OF MECHANICAL ENGINEERS (ASME)

ASME Y14.5 M - Dimensioning and Tolerancing. (DoD adopted)

(Copies of these documents are available from https://www.asme.org.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Typical application for powering. The typical application for powering shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Supply and logic					
Input voltage range (IN1, IN2, IN3) 3/	V_{INX}		2.2	6.5	V
Quiescent current, $I_Q = I_{DGND} + I_{AGND}$	I_Q	$I_{OUT1} = I_{OUT2} = I_{OUT3} = 0$ mA		150	µA
Shutdown supply current	I_{SHDN}	$V_{EN1} = V_{EN2} = V_{EN3} = 0$ V		3	µA
Enable high, enabled (EN1, EN2)	$V_{IH1, 2}$	$T_A = 25°C$	1.40		V
		T_A = Full range	1.45		
Enable high, enabled (EN3)	V_{IH3}	$T_A = 25°C$	1.14		V
		T_A = Full range	1.20		
Enable low, shutdown (EN1, EN2, EN3)	V_{ILX}		0	0.3	V
Enable pin current (EN1, EN2, EN3)	I_{ENX}			0.5	µA
Buck controllers 1 and 2					
Adjustable output voltage range 4/	$V_{OUT1, 2}$		V_{FBX}	V_{INX}	V
Feed back voltage (FB1, FB2)	$V_{FB1, 2}$		1.22 typical		V
Feed back voltage accuracy 3/ (FB1, FB2)			±2% typical		
Current into FB1, FB2 pins	$I_{FB1, 2}$			0.5	µA
Reference voltage for current sense	$V_{IS1, 2}$	$T_A = 25°C$	80	120	mV
		T_A = Full range	75	125	
Current into IS1, IS2 pins	$I_{IS1, 2}$			0.5	µA
Line regulation 3/	$\Delta V_{OUT}\%/\Delta V_{IN}$	Measured with the circuit in figure 4, $V_{OUT} + 0.5\ V \le V_{IN} \le 6.5\ V$	0.1 typical		% / V
Load regulation	$\Delta V_{OUT}\%/\Delta I_{OUT}$	Measured with the circuit in figure 4, $30\ mA \le I_{OUT} \le 2\ A$	0.6 typical		% / A
Efficiency 5/	$n_{1, 2}$	Measured with the circuit in figure 4, $I_{OUT} = 1$ A	94% typical		
Startup time 5/	$t_{STR1, 2}$	Measured with the circuit in figure 4, $R_L = 6\ \Omega$, $C_{OUT} = 100\ \mu F$, $C_{SS} = 2.2$ nF	5 typical		ms
Gate driver P-channel and N-channel MOSFET on-resistance	$R_{DS,ON1, 2}$	$V_{IN1, 2} > 2.5$ V	4 typical		Ω
		$V_{IN1, 2} = 2.2$ V	6 typical		
Gate driver P-channel and N-channel MOSFET drive current	$I_{SW1, 2}$		100 typical		mA
Minimum on time	t_{ON}		1.36	1.84	µs
Minimum off time	t_{OFF}		0.44	0.86	µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
LDO					
Output voltage range 4/	V_{OUT3}		1	6.5 - V_{DO}	V
Feed back pin voltage	V_{FB3}		0.507 typical		V
Feed back pin accuracy 3/		2.95 V ≤ V_{IN} ≤ 6.5 V, 1 mA ≤ I_{OUT3} ≤ 300 mA	±4%		
Line regulation 3/	$\Delta V_{OUT}\%/\Delta V_{IN}$	V_{OUT3} + 0.5 V ≤ V_{IN3} ≤ 6.5 V	0.075 typical		% / V
Load regulation	$\Delta V_{OUT}\%/\Delta I_{OUT}$	10 mA ≤ I_{OUT3} ≤ 2 A	0.01 typical		% / mA
Drop out voltage (V_{IN} = $V_{OUT(NOM)}$ – 0.1) 6/	V_{DO}	I_{OUT3} = 300 mA		350	mV
Current limit	I_{CL3}	V_{OUT} = 0.9 $V_{OUT(NOM)}$	375	1000	mA
Current into FB3 pin	I_{FB3}			0.1	µA
Output noise	V_n	BW = 100 Hz – 100 kHz, I_{OUT3} = 300 mA	400 typical		μV_{RMS}
Thermal shutdown temperature for LDO	t_{SD}	Shutdown, temperature increasing	175 typical		ºC
		Reset. temperature decreasing	160 typical		ºC
Under voltage lockout threshold	UVLO	V_{IN} rising	1.8 typical		V
Under voltage lockout hysteresis		V_{IN} falling	100 typical		mV

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{EN1} = V_{IN1}, V_{EN2} =V_{IN2}, V_{EN3} = V_{IN3}, V_{IN1} = V_{IN2} = 2.2 V, V_{IN3} = 3.0 V, V_{OUT3} = 2.5 V, C_{OUT1} = C_{OUT2} = 47 µF, C_{OUT2} = 47 µF, T_A = -55°C to +125°C. Typical values are at T_A = 25°C.

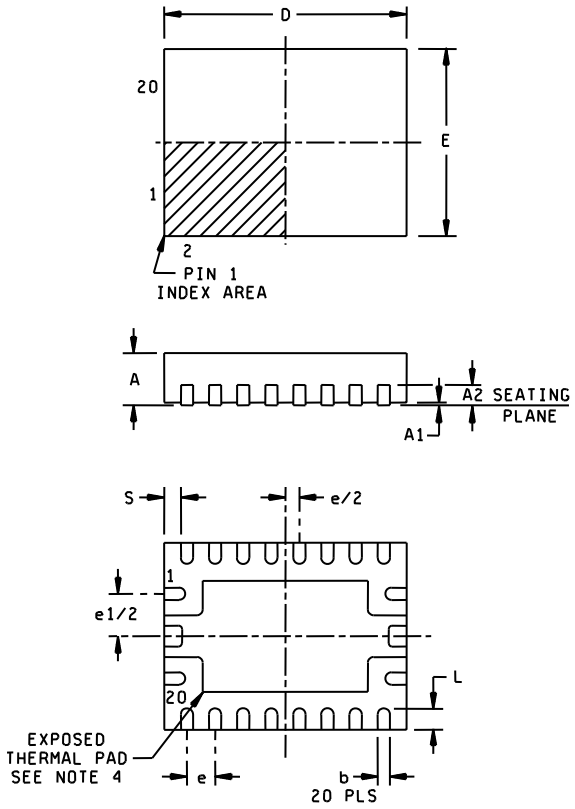
3/ To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum V_{IN3} = V_{OUT3} + V_{DO} or 2.2 V, whichever is greater.

4/ Maximum V_{OUT} is dependent on external components and will be less than V_{IN}. Parameter is not production tested.

5/ Depends on external components.

6/ V_{DO} does not apply when V_{OUT} + V_{DO} < 2.2 V.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	e	0.50 BSC	
A1	0.00	0.05	e/2	0.25 BSC	
A2	0.20 REF		e1/2	0.75 BSC	
b	0.18	0.30	L	0.30	0.50
D	4.35	4.65	S	0.325 typical	
E	3.35	3.65			

Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M – 1994.
2. This drawing is subject to change without notice.
3. QFN (Quad Flatpack No-Lead) package configuration.
4. the package thermal pad must be soldered to the board for thermal and mechanical performance. See manufacturer data sheet for details regarding the exposed thermal pad dimensions.

FIGURE 1. Case outline.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUT3	Regulated LDO output. A small ceramic capacitor (≥ 2.2 μF) is needed from this pin to ground to ensure stability.
2	FB3	Same as FB1, but for LDO.
3	EN3	Same as EN1 but for LDO.
4	EN2	Same as EN1 but for BUCK2 controller
5	SS2	Same as SS1 but for BUCK2 regulator.
6	DGND	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the manufacturer's data sheet.
7	SW2	Same as SW1, but for BUCK2 controller.
8	IN2	Input supply to BUCK2.
9	IS2	Same as IS1, but compared to IN2 and used for BUCK2 controller.
10	FB2	Same as FB1, but for BUCK2 controller.
11	FB1	Feedback pin. Used to set the output voltage of BUCK1 regulator.
12	IS1	Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required.
13	IN1	Input supply to BUCK1.
14	SW1	Gate drive pin for external BUCK1 P-channel MOSFET.
15	DGND	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the PCB layout section of this data sheet.
16	SS1	Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important.
17	EN1	Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.
18	AGND	Ground connection for LDO.
19	SS3	Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, thereby slowing output voltage ramp-up.
20	IN3	Input supply to LDO.

FIGURE 2. Terminal connections.

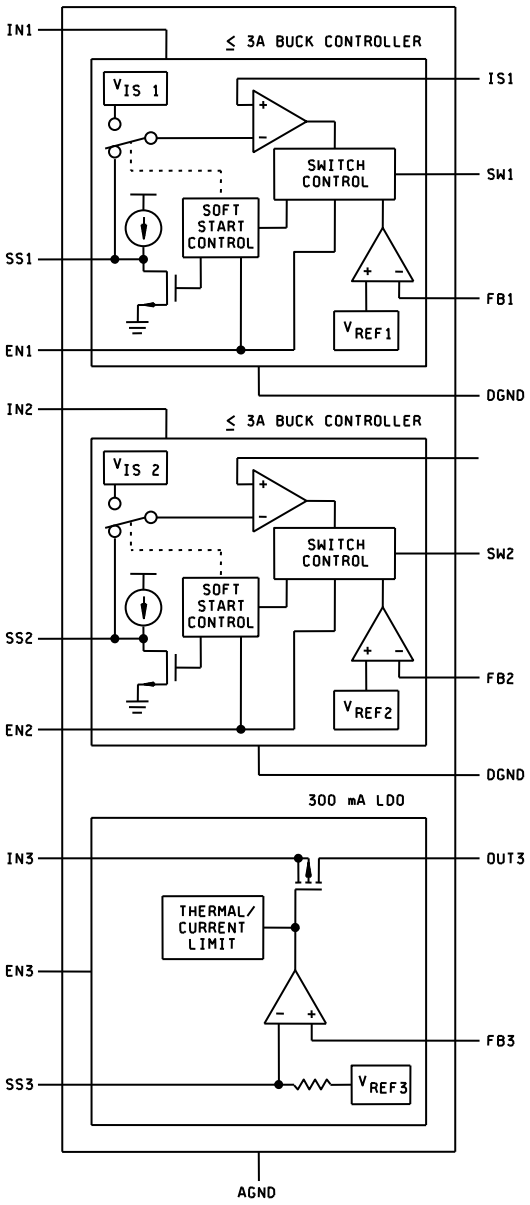


FIGURE 3. Functional block diagram.

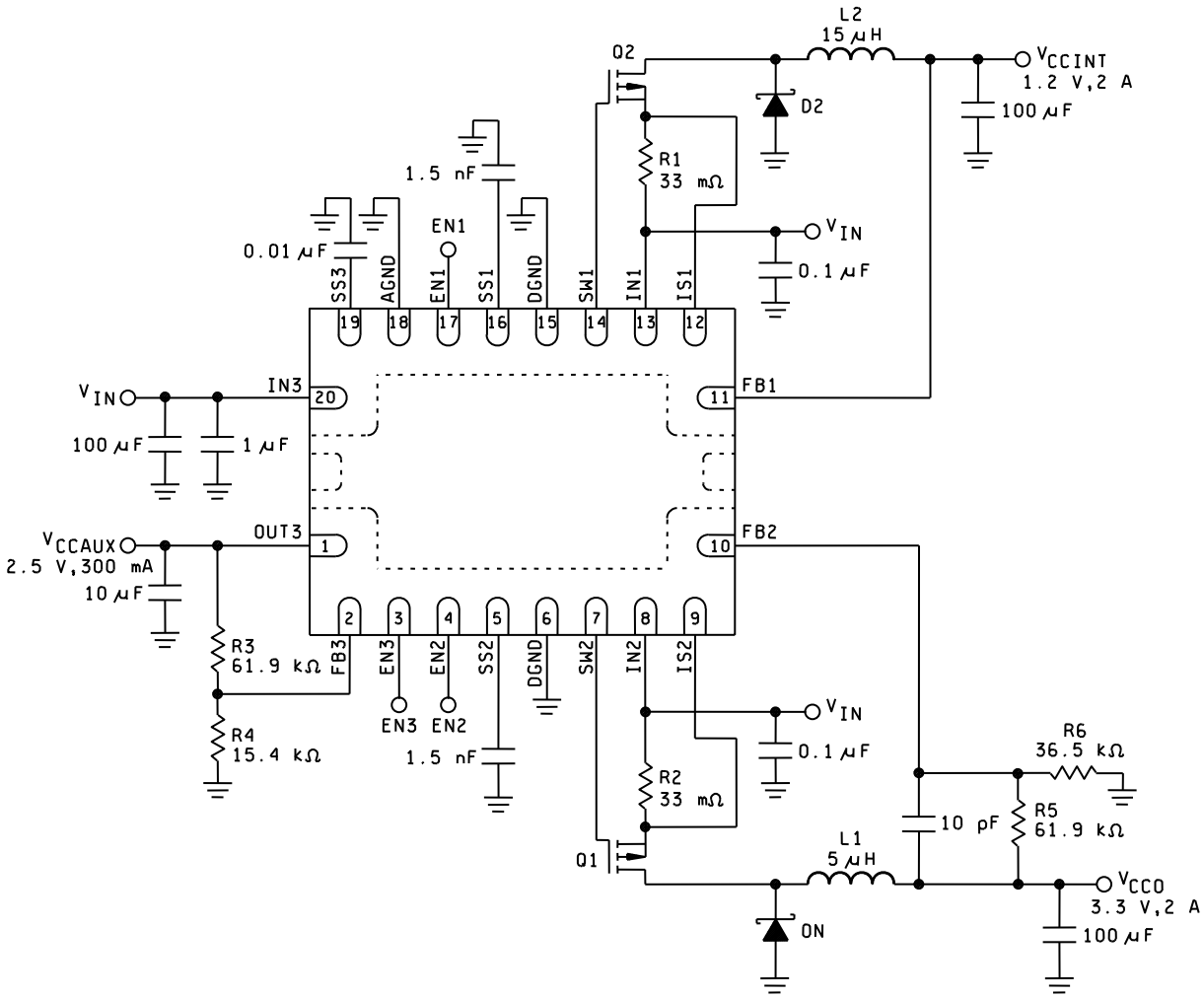


FIGURE 4. Typical application for powering.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/07614-01XE	01295	TPS75003MRHLREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243