



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 2-A wide-input-range step-down converter microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/07613</u>   Drawing number	-	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>E</u>   Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device</u>	<u>Generic</u>	<u>Output voltage</u>	<u>Circuit function</u>
01	TPS5420-EP	Adjustable to 1.22 V	2-A wide-input-range step-down converter

1.2.2 Case outline(s). The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	JEDEC MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		REV    A	PAGE    2

1.3 Absolute maximum ratings. 1/ 2/

Input voltage range:	
(VIN) .....	-0.3 V to +38.0 V <u>3/</u>
(BOOT) .....	-0.3 V to +50.0 V
(PH(steady state)) .....	-0.6 V to +38.0 V <u>3/</u>
(EN) .....	-0.3 V to +7.0 V
(VSENSE) .....	-0.3 V to +3.0 V
(BOOT-PH) .....	+10.0 V
(PH(transient < 10 ns)) .....	-1.2 V
Source current, (I <sub>O</sub> ) (PH) .....	Internally limited
Leak current, (I <sub>lkg</sub> ) (PH) .....	10 μA
Operating virtual junction temperature range (T <sub>J</sub> ) .....	-55°C to +150°C
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to +150°C
ESD rating, (HBM) .....	2 kV
Dissipation rating: <u>4/</u> <u>5/</u>	

Case outline	Thermal impedance junction-to-ambient
X <u>6/</u>	75°C/W

1.4 Recommended operating conditions. 7/

Input voltage range, V <sub>IN</sub> (V <sub>I</sub> ) .....	+5.5 V to +35.0 V
Operating virtual junction temperature range (T <sub>J</sub> ) .....	-55°C to +125°C

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
  - 2/ All voltage values are with respect to network ground terminal.
  - 3/ Approaching the absolute maximum rating for the V<sub>IN</sub> pin may cause the voltage on the PH pin to exceed the absolute maximum rating.
  - 4/ Maximum power dissipation may be limited by over current protection.
  - 5/ Power rating at a specific ambient temperature T<sub>A</sub> should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final printed circuit board (PCB) should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See manufacturer for more information.
  - 6/ Test board conditions:
    - a. 3 inch x 3 inch, two layers, thickness: 0.062 inch.
    - b. 2 ounces copper traces located on the top and bottom of the PCB.
  - 7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		REV    A	PAGE    3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Schematic diagram. The schematic diagram shall be as shown in figure 3.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		<b>REV     A</b>	<b>PAGE    4</b>

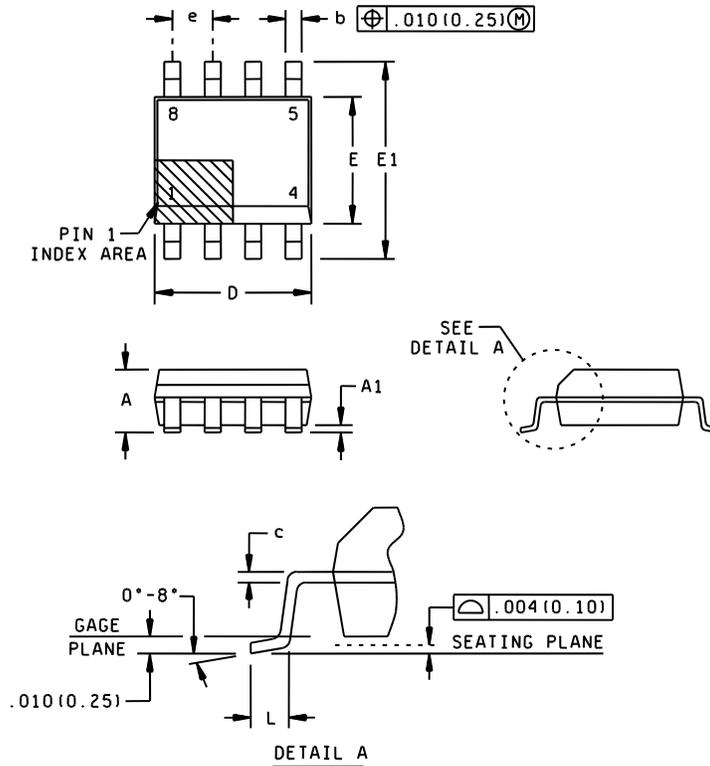
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 5.5 V ≤ VIN ≤ 35.0 V -55°C ≤ TJ ≤ 125°C unless otherwise specified	Limits		Unit
			Min	Max	
Supply voltage (VIN pin)					
Quiescent current	IQ	VSENSE = 2.0 V, not switching, PH pin open		4.4	mA
		Shutdown, ENA = 0 V		50.0	μA
Undervoltage Lockout (UVLO)					
Start threshold voltage, UVLO				5.5	V
Hysteresis voltage, UVLO			330 typical		mV
Voltage reference					
Voltage reference accuracy		TJ = 25°C	1.202	1.239	V
		IQ = 0 A to 2 A	1.196	1.245	
Oscillator					
Internally set free-running frequency		TJ = 25°C	400	600	kHz
		TJ = -55°C to 125°C	375	600	
Minimum controllable on time				200	ns
Maximum duty cycle			87%		
Enable (ENA pin)					
Start threshold voltage, ENA				1.3	V
Stop threshold voltage, ENA			0.5		V
Hysteresis voltage, ENA			450 typical		mV
Internal slow-start time (0 – 100%)			6.6	10.6	ms
Current limit					
Current limit			3.0	5.2	A
Current limit hiccup time			13.0	22.0	ms
Thermal shutdown					
Thermal shutdown trip point			135		°C
Thermal shutdown hysteresis			14 typical		°C
Output MOSFET					
High-side power MOSFET switch	rDS(on)	VIN = 5.5 V	150 typical		mΩ
		VIN = 10.0 V to 35.0 V		230	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		<b>REV A</b>	<b>PAGE 5</b>

Case X



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.27	e	.050 BSC		1.27 BSC	
A1	.004	.010	0.10	0.25	E	.150	.157	3.80	4.00
b	.012	.020	0.31	0.51	E1	.228	.244	5.80	6.20
c	.005	.010	0.12	0.25	L	.016	.050	0.40	1.27
D	.189	.197	4.80	5.00					

Notes:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. This drawing is subject to change without notice.
3. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
4. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
5. Falls within JEDEC MS-012 with variation AA.

FIGURE 1. Case outline.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	SIZE <b>A</b>	CODE IDENT NO. <b>16236</b>	DWG NO. <b>V62/07613</b>
		REV <b>A</b>	PAGE <b>6</b>

Case X

Terminal number	Terminal symbol	Description
1	BOOT	Boost capacitor for the high-side field effect transistor (FET) gate driver. Connect 0.01 $\mu$ F low-equivalent series resistance (ESR) capacitor from BOOT to PH pin
2	NC	Not connected internally
3	NC	Not connected internally
4	VSENSE	Feedback voltage for the regulator. Connect to output voltage divider.
5	ENA	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable
6	GND	Ground
7	VIN	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality, low ESR ceramic capacitor
8	PH	Source of the high-side power metal oxide semiconductor field effect transistor (MOSFET). Connected to external inductor and diode.

FIGURE 2. Terminal connections.

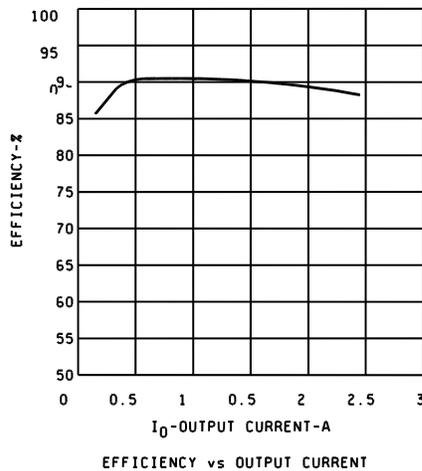
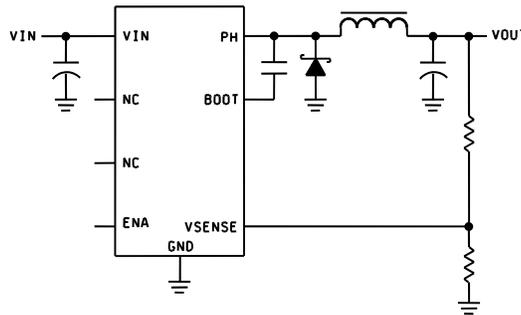


FIGURE 3. Schematic diagram.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		<b>REV     A</b>	<b>PAGE    7</b>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u> <u>2/</u>	Device manufacturer CAGE code	Vendor part number
V62/07613-01XE	01295	TPS5420MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243  
Point of contact: U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/07613</b>
		<b>REV      A</b>	<b>PAGE      8</b>