REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add MIL-STD-883 reference to section 2. Delete junction temperature reference from paragraph 1.3. Make change to footnote 3/ as specified under paragraph 6.3. Update document paragraphs to current requirements. - ro	14-10-22	C. SAFFLE
B	Add "T_A = 125°C power rating" limits under paragraph 1.5. Update document paragraphs to the current requirements. - ro	20-04-07	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B						
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32						
REV STATUS OF PAGES	**REV**				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 07-02-07	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, HIGH SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS, MONOLITHIC SILICON
	APPROVED BY JOSEPH RODENBECK	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07612**
	REV **B**	**PAGE** 1 **OF** 32

AMSC N/A

5962-V029-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high speed differential line drivers and receivers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65LVDS050	High speed differential line drivers and receivers
02	SN65LVDS051	High speed differential line drivers and receivers
03	SN65LVDS179	High speed differential line drivers and receivers
04	SN65LVDS180	High speed differential line drivers and receivers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
N	8	MO-187-AA	Plastic surface mount
T	8	MS-012-AA	Plastic surface mount
U	14	MO-153	Plastic surface mount
X	14	MS-012-AB	Plastic surface mount
Y	16	MO-153	Plastic surface mount
Z	16	MS-012-AC	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 4 V 2/
Voltage range:
D, R, DE, and $\overline{RE}$ pins ..... -0.5 V to 6 V
Y, Z, A, and B pins ..... -0.5 V to 4 V
Electrostatic discharge (ESD):
Y, Z, A, B, and GND pins ..... Class 3, A: 12 kV, B: 600 V 3/
All pins ..... Class 3, A: 7 kV, B: 500 V
Power dissipation (P_D) ..... See 1.5, dissipation ratings table
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 250°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC}) ..... 3 V to 3.6 V
High level input voltage (V_{IH}) ..... 2 V minimum
Low level input voltage (V_{IL}) ..... 0.8 V maximum
Magnitude of differential input voltage $|V_{ID}|$ ..... 0.1 V to 0.6 V
Magnitude of differential output voltage with disabled driver $|V_{OD(dis)}|$ ..... 520 mV maximum
Driver output voltage (V_{OY} or V_{OZ}) ..... 0 V to 2.4 V
Common mode input voltage (V_{IC}) (see figure 5) ..... $|V_{ID}|$ / 2 V to 2.4 – ($|V_{ID}|$ / 2 V)
V_{CC} – 0.8 V maximum
Operating free-air temperature range (T_A) ..... -55°C to +125°C 5/

1.5 Dissipation ratings table.

Package	$T_A \leq 25°C$ power rating	Derating factor above $T_A = 25°C$ 6/	$T_A = 85°C$ power rating	$T_A = 125°C$ power rating
N	424 mW	3.4 mW/°C	220 mW	84 mW
T	635 mW	5.1 mW/°C	330 mW	125 mW
U	736 mW	5.9 mW/°C	383 mW	146 mW
X	987 mW	7.9 mW/°C	513 mW	197 mW
Y	839 mW	6.7 mW/°C	437 mW	169 mW
Z	1110 mW	8.9 mW/°C	577 mW	220 mW

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
3/ Tested in accordance with MIL-STD-883C method 3015.7.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer for additional information on enhanced plastic packaging.
6/ This is the inverse of the junction to ambient thermal resistance when board mounted and with no air flow.

2. APPLICABLE DOCUMENTS

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth tables. The truth tables shall be as shown in figure 3.

3.5.4 Logic diagrams. The logic diagrams shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Device electrical characteristics section							
Supply current	I_{CC}	Drivers and receivers enabled, no receiver loads, driver R_L = 100 Ω	-55°C to +125°C	01		20	mA
		Drivers enabled, receivers disabled, R_L = 100 Ω				16	
		Drivers disabled, receivers enabled, no loads				6	
		Disabled				1	
		Drivers enabled, no receiver loads, driver R_L = 100 Ω		02		20	
		Drivers disabled, no loads				6	
		No receiver loads, driver R_L = 100 Ω		03		12	
		Driver and receiver enabled, no receiver load, driver R_L = 100 Ω		04		12	
		Driver enabled, receiver disabled, R_L = 100 Ω				7	
		Driver disabled, receiver enabled, no load				2	
		Disabled				1	
Driver electrical characteristics section							
Differential output voltage magnitude	$\|V_{OD}\|$	See figures 6 and 7, R_L = 100 Ω	-55°C to +125°C	All	247	454	mV
Change in differential output voltage magnitude between logic states	$\Delta\|V_{OD}\|$	See figures 6 and 7, R_L = 100 Ω	-55°C to +125°C	All	-50	50	mV
Steady state common mode output voltage	$V_{OC(SS)}$	See figure 8	-55°C to +125°C	All	1.125	1.375	V
Change in steady state common mode output voltage between logic states	$\Delta V_{OC(SS)}$	See figure 8	-55°C to +125°C	All	-50	50	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section - continued							
Peak to peak common output voltage	$V_{OC(PP)}$	See figure 8	-55°C to +125°C	All		150	mV
High level input current	I_{IH}	DE pin, V_{IH} = 5 V	-55°C to +125°C	All		-20	µA
		D pin, V_{IH} = 5 V				20	
Low level input current	I_{IL}	DE pin, V_{IL} = 0.8 V	-55°C to +125°C	All		-10	µA
		D pin, V_{IL} = 0.8 V				10	
Short circuit output current	I_{OS}	V_{OY} or V_{OZ} = 0 V	-55°C to +125°C	All		10	mA
		V_{OD} = 0 V				10	
Off state output current	$I_{O(OFF)}$	DE = 0 V, V_{OY} or V_{OZ} = 0 V	-55°C to +125°C	All	-1	1	µA
		DE = V_{CC}, V_{OY} or V_{OZ} = 0 V, V_{CC} < 1.5 V			-1	1	
Input capacitance	C_{IN}		-55°C to +125°C	All	3 typical		pF
Receiver electrical characteristics section							
Positive going differential input voltage threshold	V_{IT+}	See figure 5 and Table II	-55°C to +125°C	All		100	mV
Negative going differential input voltage threshold	V_{IT-}	See figure 5 and Table II	-55°C to +125°C	All	-100		mV
High level output voltage	V_{OH}	I_{OH} = -8 mA	-55°C to +125°C	All	2.4		V
		I_{OH} = -4 mA			2.8		
Low level output voltage	V_{OL}	I_{OL} = 8 mA	-55°C to +125°C	All		0.4	V
Input current (A or B inputs)	I_I	V_I = 0	-55°C to +125°C	All	-2	-20	µA
		V_I = 2.4 V			-1.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section - continued							
Power off input current (A or B inputs)	$I_{I(OFF)}$	V_{CC} = 0 V	-55°C to +125°C	All		±20	µA
High level input current (enables)	I_{IH}	V_{IH} = 5 V	-55°C to +125°C	All		±10	µA
Low level input current (enables)	I_{IL}	V_{IL} = 0.8 V	-55°C to +125°C	All		±10	µA
High impedance output current	I_{OZ}	V_O = 0 or 5 V	-55°C to +125°C	All		±10	µA
Input capacitance	C_{IN}		-55°C to +125°C	All	5 typical		pF
Driver switching characteristics section							
Propagation delay time, low to high level output	t_{PLH}	R_L = 100 Ω, C_L = 10 pF, see figure 7	-55°C to +125°C	All		4.5	ns
Propagation delay time, high to low level output	t_{PHL}	R_L = 100 Ω, C_L = 10 pF, see figure 7	-55°C to +125°C	All		4.5	ns
Differential output signal rise time	t_r	R_L = 100 Ω, C_L = 10 pF, see figure 7	-55°C to +125°C	All		1.2	ns
Differential output signal fall time	t_f	R_L = 100 Ω, C_L = 10 pF, see figure 7	-55°C to +125°C	All		1.2	ns
Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$t_{sk(p)}$	R_L = 100 Ω, C_L = 10 pF, 2/ see figure 7	+25°C	All	300 typical 3/		ps
Channel to channel output skew	$t_{sk(o)}$	R_L = 100 Ω, C_L = 10 pF, 4/ see figure 7	+25°C	All	150 typical 3/		ps
Enable time	t_{en}	See figure 9	-55°C to +125°C	All		10	ns
Disable time	t_{dis}	See figure 9	-55°C to +125°C	All		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver switching characteristics section							
Propagation delay time, low to high level output	t_{PLH}	C_L = 10 pF, see figure 10	-55°C to +125°C	All		4.5	ns
Propagation delay time, high to low level output	t_{PHL}	C_L = 10 pF, see figure 10	-55°C to +125°C	All		4.5	ns
Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	$t_{sk(p)}$	C_L = 10 pF, see figure 10 2/	+25°C	All	0.3 typical 3/		ns
Output signal rise time	t_r	C_L = 10 pF, see figure 10	-55°C to +125°C	All		1.5	ns
Output signal fall time	t_f	C_L = 10 pF, see figure 10	-55°C to +125°C	All		1.5	ns
Propagation delay time, high impedance to high leveloutput	t_{PZH}	See figure 11	+25°C	All	2.5 typical 3/		ns
Propagation delay time, high impedance to low level output	t_{PZL}	See figure 11	+25°C	All	2.5 typical 3/		ns
Propagation delay time, high level to high impedance output	t_{PHZ}	See figure 11	+25°C	All	7 typical 3/		ns
Propagation delay time, low level to high impedance output	t_{PLZ}	See figure 11	+25°C	All	4 typical 3/		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $t_{sk(p)}$ is the magnitude of the time difference between the high to low and low to high propagation delay times at an output.

3/ Typical values are at 25°C and with a 3.3 V supply.

4/ $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

TABLE II. Receiver minimum and maximum input threshold test voltages.

Applied voltages		Resulting differential input voltages	Resulting common mode input voltage
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

Case N

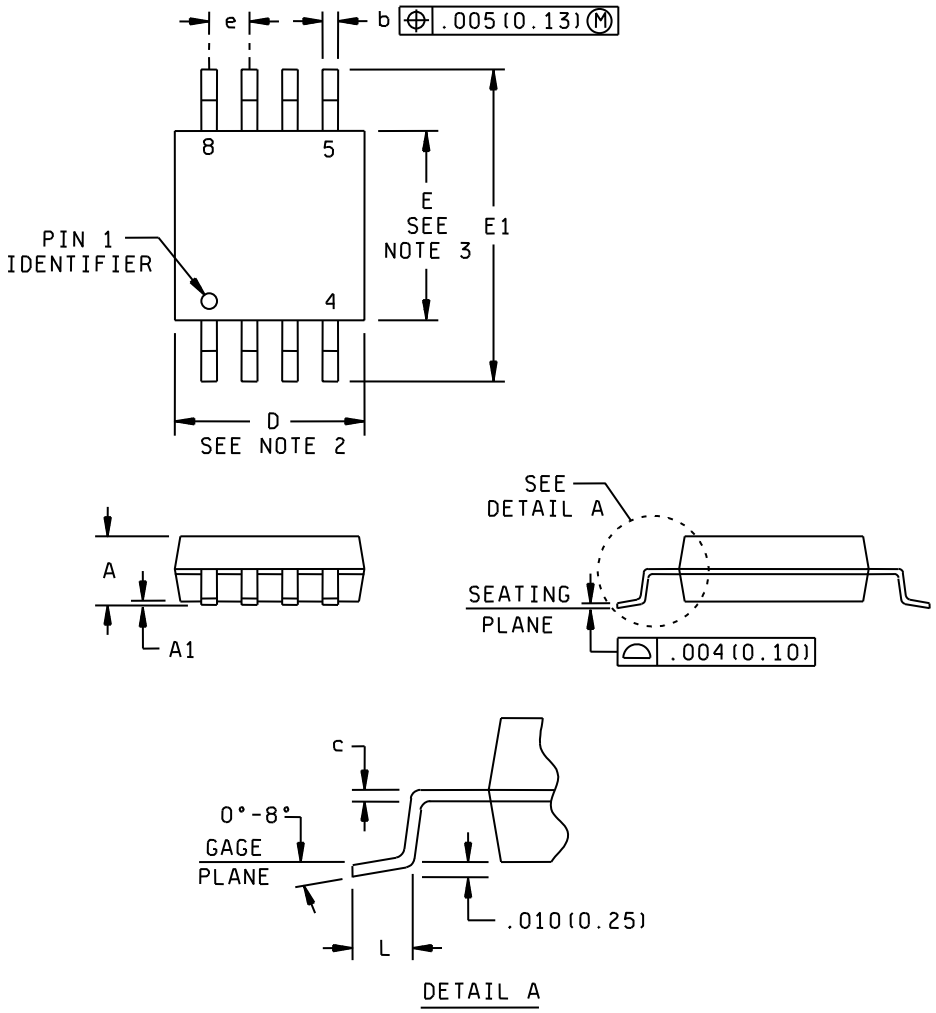


FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07612
		REV B	PAGE 10

Case N - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.043	---	1.10
A1	0.001	0.005	0.05	0.15
b	0.009	0.014	0.25	0.38
c	0.005	0.009	0.13	0.23
D	0.114	0.122	2.90	3.10
E	0.114	0.122	2.90	3.10
E1	0.187	0.198	4.75	5.05
e	0.025 BSC		0.65 BSC	
L	0.015	0.027	0.40	0.70
n	8		8	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.50 mm (0.020 inch) per side.
4. Falls with JEDEC MO-187-AA, except interlead flash.

FIGURE 1. Case outlines - Continued.

Case T

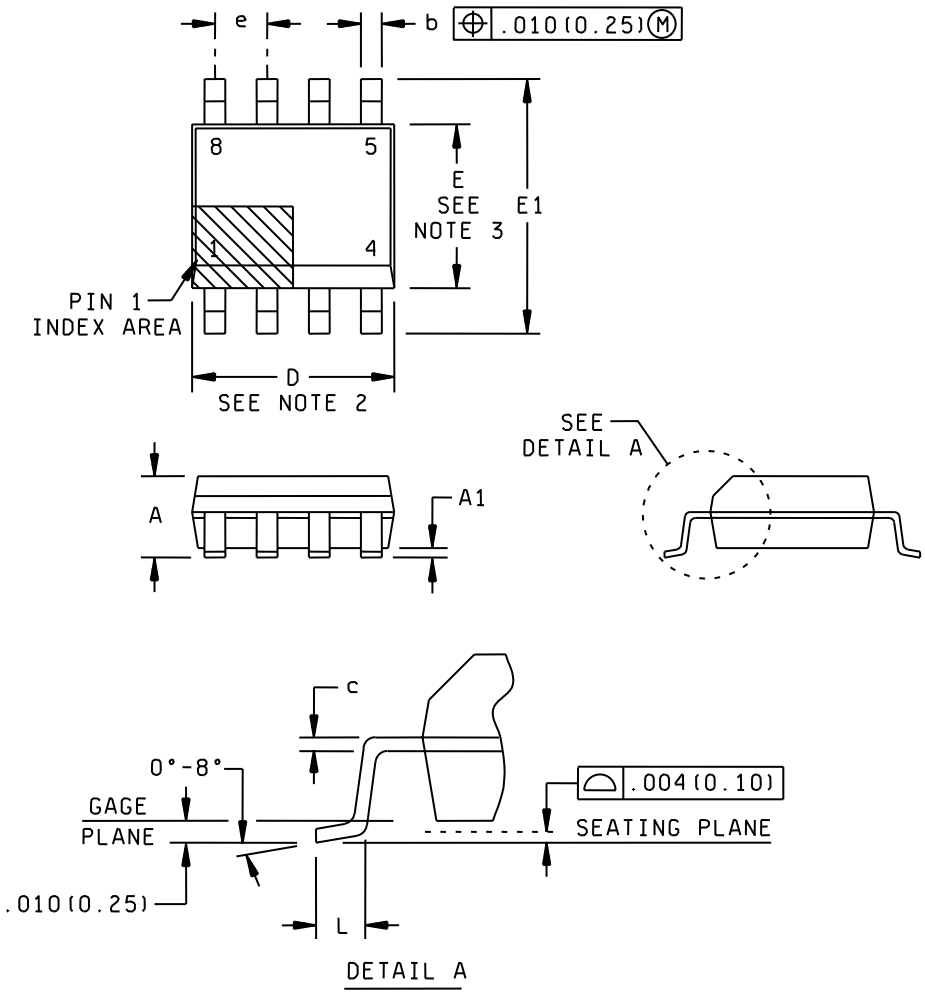


FIGURE 1. Case outlines – Continued.

Case T - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outlines - Continued.

Case U

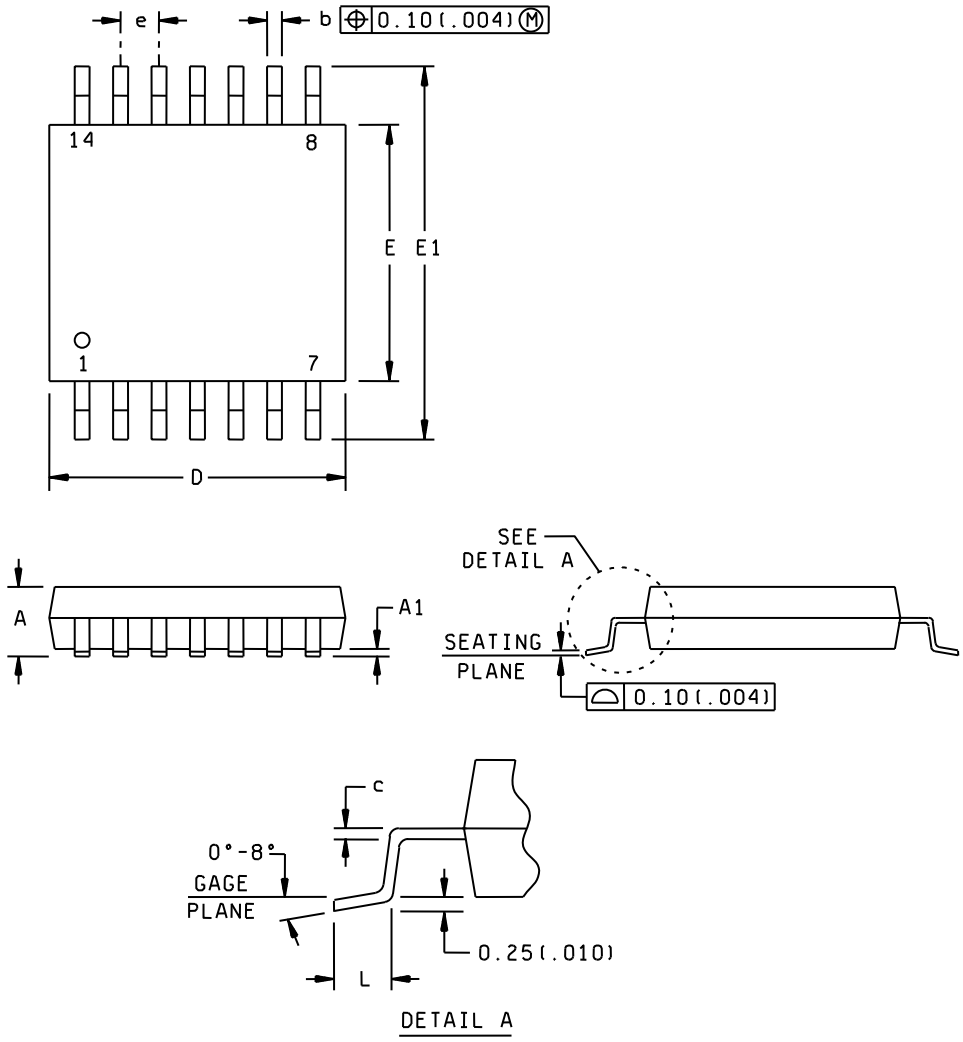


FIGURE 1. Case outlines – Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.005 NOM		0.15 NOM	
D	.192	.200	4.90	5.10
E	.169	.177	4.30	4.50
E1	.244	.259	6.20	6.60
e	.025 BSC		0.65 BSC	
L	.019	.029	0.50	0.75
n	14		14	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.009 inch) per side.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

Case X

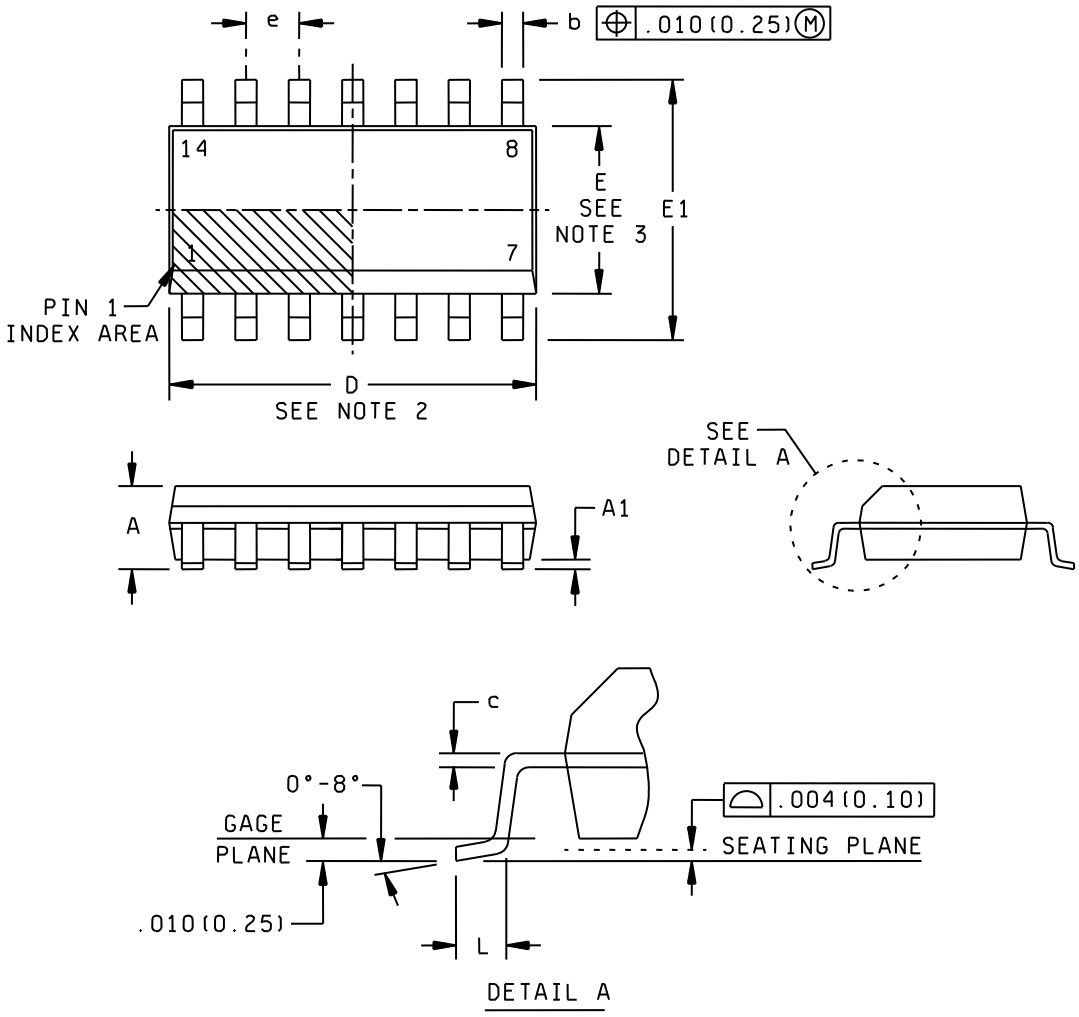


FIGURE 1. Case outlines – Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	14		14	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012-AB.

FIGURE 1. Case outlines - Continued.

Case Y

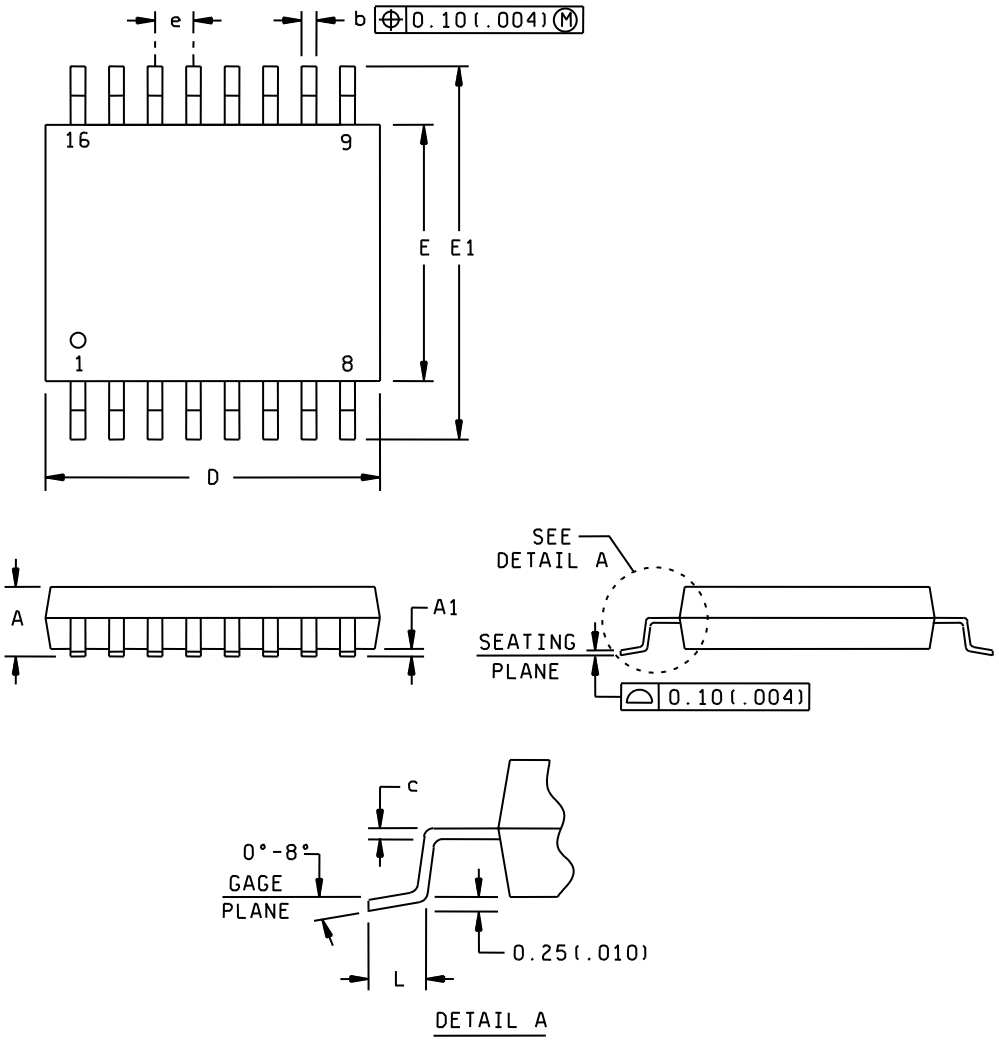


FIGURE 1. Case outlines – Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	0.005 NOM		0.15 NOM	
D	.192	.200	4.90	5.10
E	.169	.177	4.30	4.50
E1	.244	.259	6.20	6.60
e	.025 BSC		0.65 BSC	
L	.019	.029	0.50	0.75
n	16		16	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.009 inch) per side.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

Case Z

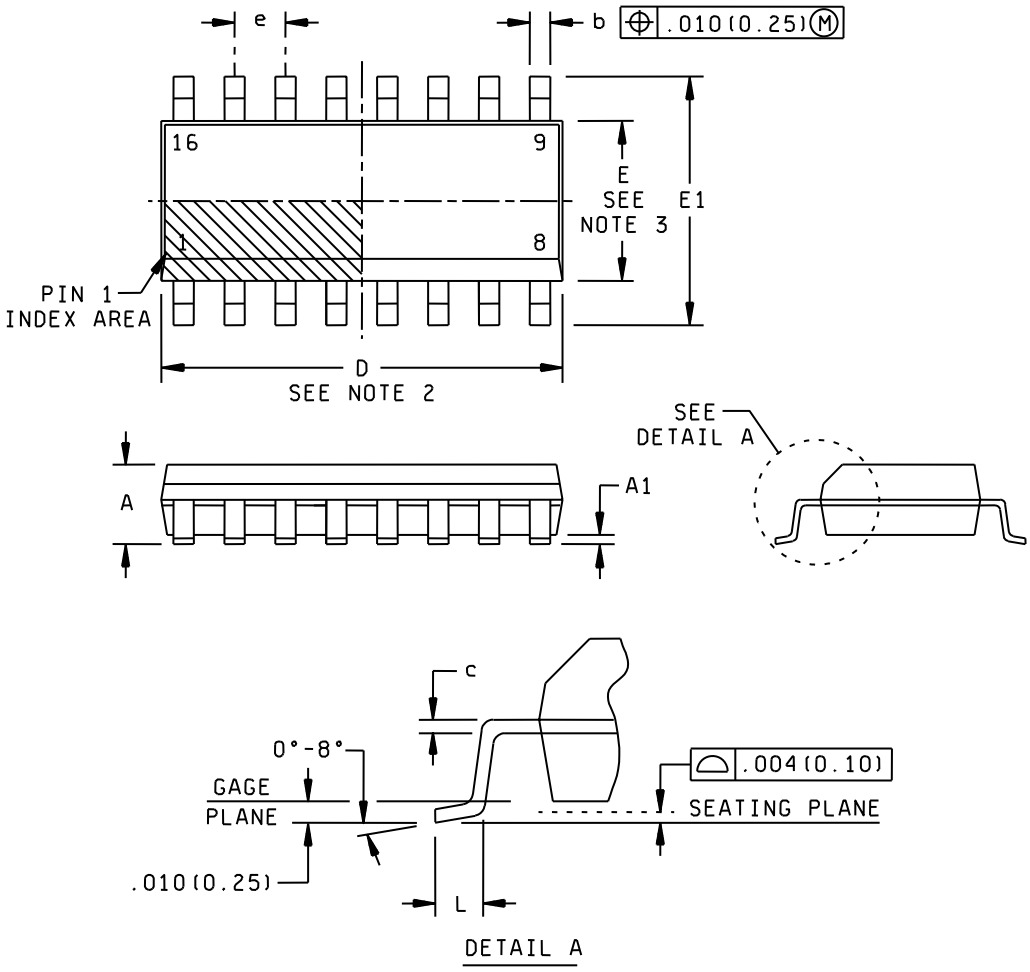


FIGURE 1. Case outlines – Continued.

Case Z - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	16		16	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012-AC.

FIGURE 1. Case outlines - Continued.

Device types	01	02	03	04
Case outlines	Y and Z	Y and Z	N and T	U and X
Terminal number	Terminal symbol			
1	1B	1B	V_{CC}	NC
2	1A	1A	R	R
3	1R	1R	D	$\overline{RE}$
4	$\overline{RE}$	1DE	GND	DE
5	2R	2R	Y	D
6	2A	2A	Z	GND
7	2B	2B	B	GND
8	GND	GND	A	NC
9	2D	2D	---	Y
10	2Y	2Y	---	Z
11	2Z	2Z	---	B
12	DE	2DE	---	A
13	1Z	1Z	---	V_{CC}
14	1Y	1Y	---	V_{CC}
15	1D	1D	---	---
16	V_{CC}	V_{CC}	---	---

Terminal symbol	Description
A	Receiver input
B	Receiver input
D	Driver input
DE	Driver input
GND	Ground
R	Receiver output
$\overline{RE}$	Receiver input
V_{CC}	Supply voltage
Y	Driver output
Z	Driver output

FIGURE 2. Terminal connections.

Device types 01, 02, 04

Receiver

Inputs		Output
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
-100 mV < V_{ID} < 100 mV	L	?
$V_{ID} \leq$ - 100 mV	L	L
Open	L	H
X	H	Z

Driver

Inputs		Outputs	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	OFF	OFF

H = High level
L = Low
Z = High impedance
X = Don't care
OFF = No output

FIGURE 3. Truth tables.

Device type 03

Receiver

Inputs	Output
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV < V_{ID} < 100 mV	?
$V_{ID} \geq$ - 100 mV	L
Open	H

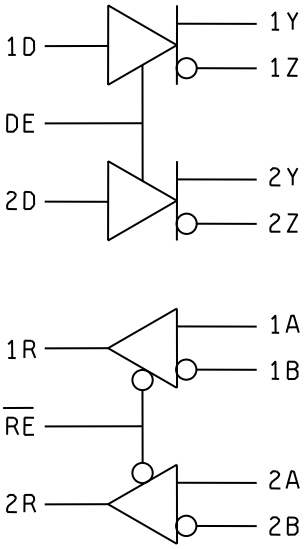
Driver

Input	Outputs	
D	Y	Z
L	L	H
H	H	L
Open	L	H

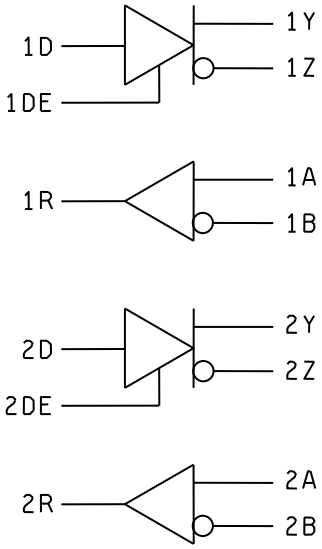
H = High level
L = Low
? = Indeterminate

FIGURE 3. Truth tables - continued.

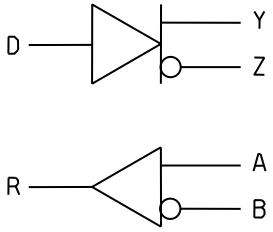
DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 03



DEVICE TYPE 04

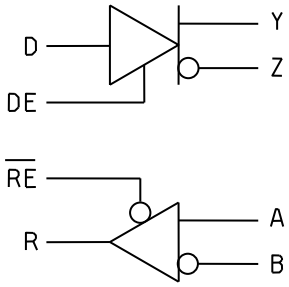


FIGURE 4. Logic diagrams.

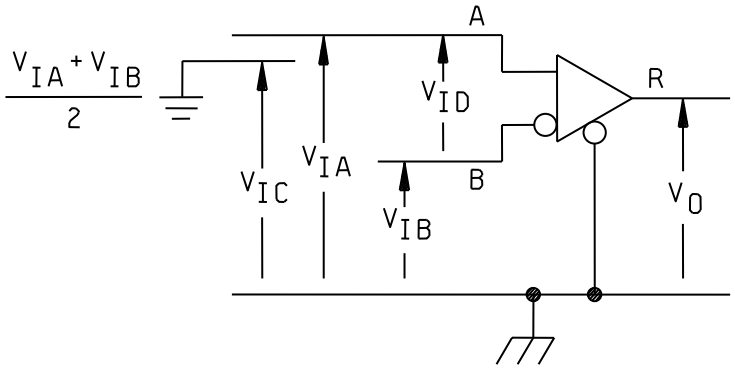


FIGURE 5. Receiver voltage definitions.

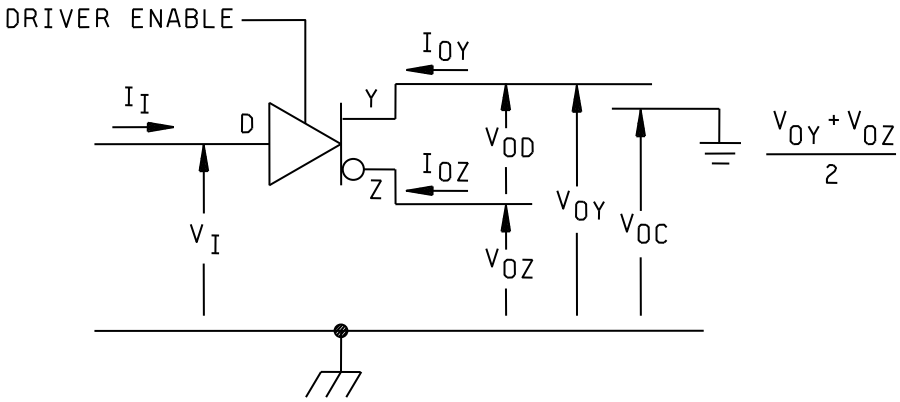
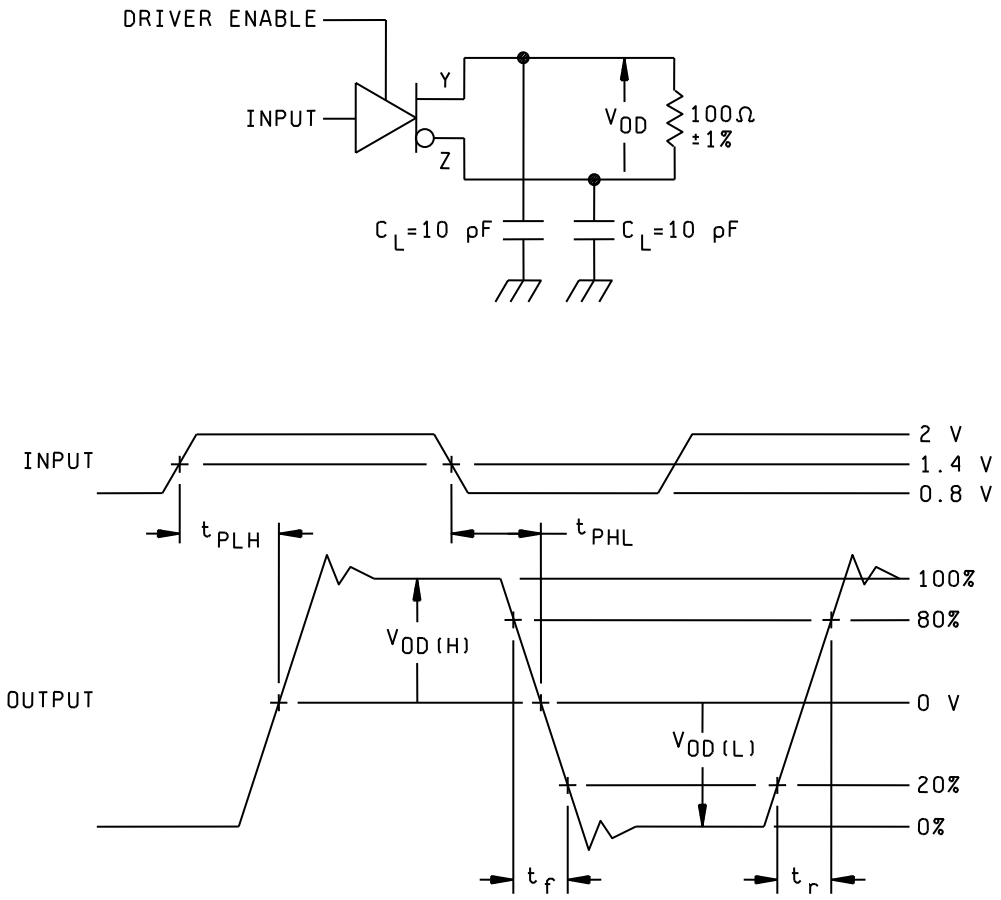
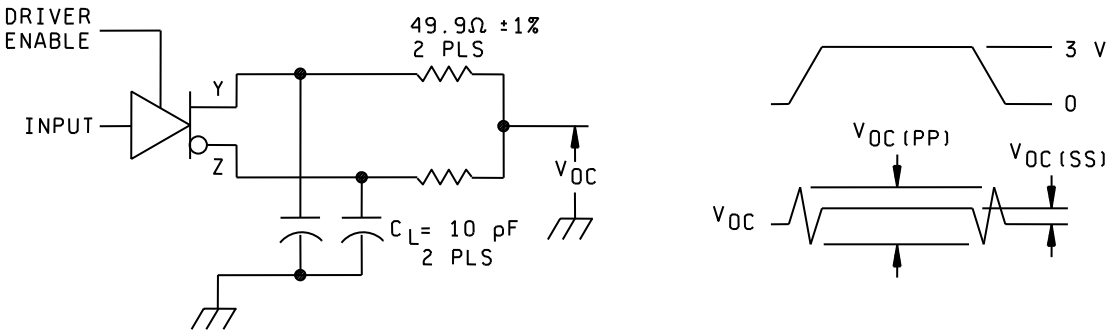


FIGURE 6. Driver voltage and current definitions.



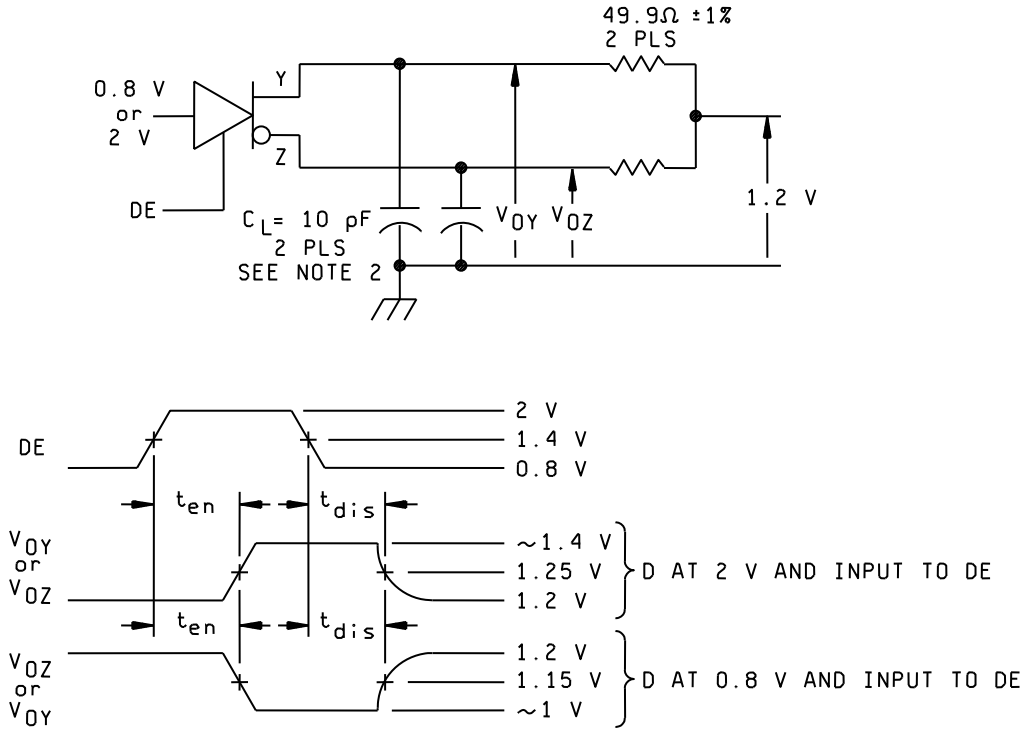
NOTE: All input pulses are supplied by a generator having the following characteristics:
t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 million pulses per second (Mpps), pulse width = 10 ±0.2 ns.
C_L includes instrumentation and fixture capacitance with 0.06 mm of the device under test.

FIGURE 7. Test circuit, timing, and voltage definitions for the differential output signal.



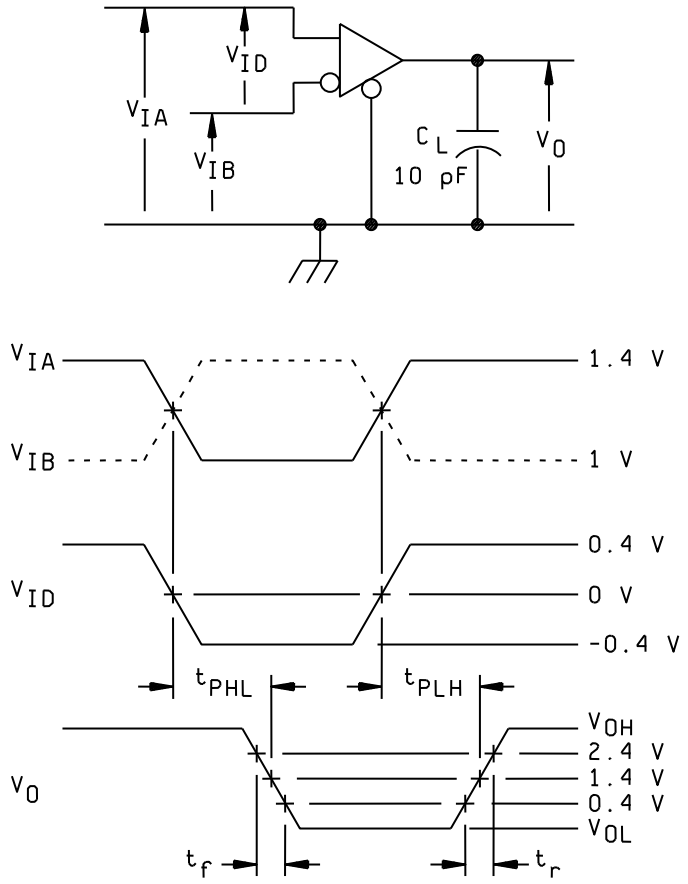
NOTE: All input pulses are supplied by a generator having the following characteristics:
t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.
C_L includes instrumentation and fixture capacitance with 0.06 mm of the device under test.
The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

FIGURE 8. Test circuit and definitions for the driver common mode output voltage.



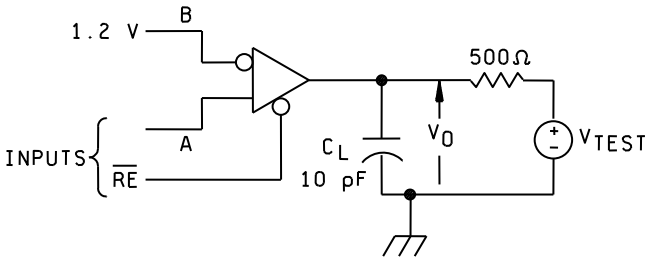
NOTE: All input pulses are supplied by a generator having the following characteristics:
t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns.
C_L includes instrumentation and fixture capacitance with 0.06 mm of the device under test.

FIGURE 9. Enable and disable time circuit and definitions.



NOTE: All input pulses are supplied by a generator having the following characteristics:
t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.
C_L includes instrumentation and fixture capacitance with 0.06 mm of the device under test.

FIGURE 10. Timing test circuit and waveforms.



NOTE: All input pulses are supplied by a generator having the following characteristics:
t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns.
C_L includes instrumentation and fixture capacitance with 0.06 mm of the device under test.

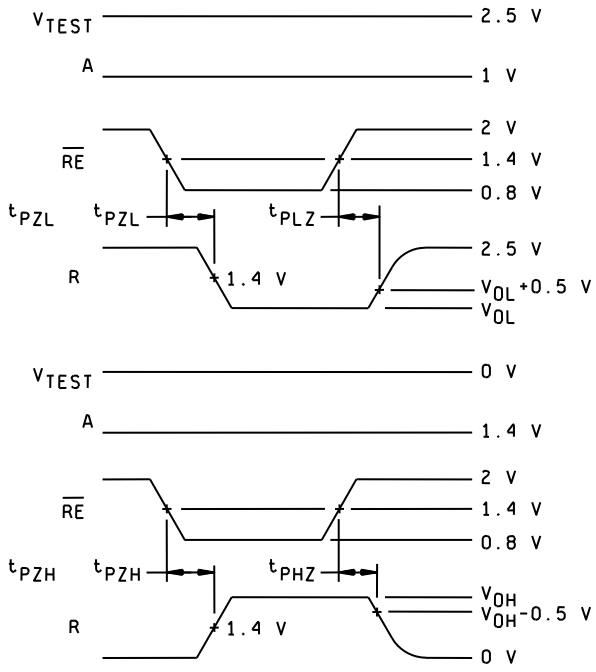


FIGURE 11. Enable / disable time test circuit and waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Vendor part number
V62/07612-01YE	3/	SN65LVDS050MPWREP
V62/07612-01ZE	3/	SN65LVDS050MDREP
V62/07612-02YE	3/	SN65LVDS051MPWREP
V62/07612-02ZE	3/	SN65LVDS051MDREP
V62/07612-03NE	01295	SN65LVDS179MDGKREP
V62/07612-03TE	3/	SN65LVDS179MDREP
V62/07612-04UE	3/	SN65LVDS180MPWREP
V62/07612-04XE	3/	SN65LVDS180MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current packaging and ordering information, see package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available from the manufacturer.
3/ Not available from an approved source.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243