REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add AIN, $\overline{AIN}$, CLK and $\overline{CLK}$ parameters to paragraph 1.3. Update document paragraphs to reflect current requirements. - ro	14-09-10	C. SAFFLE
B	Make clarification to Voltage difference limits as specified under paragraph 1.3. Update document paragraphs to current requirements. - ro	20-05-27	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B																		
PAGE	18	19	20																		

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-12-22	**CHECKED BY** TOM HESS **APPROVED BY** RAYMOND MONNIN	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT, 500 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07607**
	REV **B**	**PAGE** 1 **OF** 20

AMSC N/A

5962-V022-20

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12-bit, 500 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADS5463-EP	12 bit, 500 MSPS, analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	80	MS-026	Plastic quad flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage :
- AV_{DD5} to GND ..... 6 V
- AV_{DD3} to GND ..... 5 V
- DV_{DD3} to GND ..... 5 V

Voltage difference between pin and ground:
- AIN, $\overline{AIN}$ to GND: 2/
  - AC signal ..... -0.3 V to (AV_{DD5} + 0.3 V)
  - DC signal, T_J = 105°C ..... 0.4 V to 4.4 V
  - DC signal, T_J = 125°C ..... 1.0 V to 3.8 V

Voltage difference between these pins:
- AIN to $\overline{AIN}$: 2/
  - AC signal ..... -5.2 V to 5.2 V
  - DC signal, T_J = 105°C ..... -4 V to 4 V
  - DC signal, T_J = 125°C ..... -2.8 V to 2.8 V

Voltage difference between pin and ground:
- CLK, $\overline{CLK}$ to GND: 2/
  - AC signal ..... -0.3 V to (AV_{DD5} + 0.3 V)
  - DC signal, T_J = 105°C ..... 0.1 V to 4.7 V
  - DC signal, T_J = 125°C ..... 1.1 V to 3.7 V

Voltage difference between these pins:
- CLK to $\overline{CLK}$: 2/
  - AC signal ..... -3.3 V to 3.3 V
  - DC signal, T_J = 105°C ..... -3.3 V to 3.3 V
  - DC signal, T_J = 125°C ..... -2.6 V to 2.6 V

Digital data output to GND ..... -0.3 V to DV_{DD3} + 0.3 V

Maximum junction temperature (T_J) ..... +150°C

Storage temperature range (T_{STG}) ..... -65°C to 150°C

Electrostatic discharge (ESD) human body model (HBM) ..... 2 kV

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Valid when supplies are within recommended operating range.

1.4 Recommended operating conditions. 3/

Supplies:
- Analog supply voltage (AV_{DD5}) ..... 4.75 V to 5.25 V
- Analog supply voltage (AV_{DD3}) ..... 3 V to 3.6 V
- Output driver supply voltage (DV_{DD3}) ..... 3 V to 3.6 V

Analog input:
- Differential input range ..... 2.2 V_{PP} typical
- Input common mode voltage (V_{CM}) ..... 2.4 V typical

Digital output: (DRY, DATA, OVR)
- Maximum differential output load ..... 10 pF typical

Clock input:
- CLK input sample rate (sine wave) ..... 20 MSPS to 500 MSPS
- Clock amplitude, differential sine wave ..... 3 V_{PP} typical
- Clock duty cycle ..... 50 % typical

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. 4/

Parameter	Test conditions	Typical limits
$R_{\theta JA}$ 5/	Soldered thermal pad, no airflow	23.7°C/W
$R_{\theta JA}$ 5/	Soldered thermal pad, 150 LFM airflow	17.8°C/W
$R_{\theta JA}$ 5/	Soldered thermal pad, 250 LFM airflow	16.4°C/W
$R_{\theta JP}$ 6/	Bottom of package (thermal pad)	2.99°C/W

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ Using 36 thermal vias (6 x 6 array).

5/ $R_{\theta JA}$ is the thermal resistance from junction to ambient.

6/ $R_{\theta JP}$ is the thermal resistance from junction to the thermal pad.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			+25°C	01	12 typical		Bits
Analog inputs section							
Differential input range			+25°C	01	2.2 typical		V_{PP}
Input common mode	V_{CM}		+25°C	01	2.4 typical		V
Input resistance (dc)		Each input to ground	+25°C	01	500 typical		Ω
Input capacitance		Each input to ground	+25°C	01	2.5 typical		pF
Analog input bandwidth (-3 dB)		Dependent on source impedance	+25°C	01	2 typical		GHz
Common mode rejection ratio	CMRR	Common mode signal = 10 MHz	+25°C	01	80 typical		dB
Internal reference voltage section							
Reference voltage	V_{REF}		+25°C	01	2.4 typical		V
Dynamic accuracy section							
No missing codes					Assured		
Differential linearity error	DNL	f_{IN} = 10 MHz	-55°C to +125°C	01	-0.95	0.95	LSB
Integral linearity error	INL	f_{IN} = 10 MHz	-55°C to +125°C	01	-2.5	2.5	LSB
Offset error			-55°C to +125°C	01	-11	11	mV
Offset temperature coefficient			+25°C	01	0.0005 typical		mV/°C
Gain error			-55°C to +125°C	01	-5.2	5.2	%FS
Gain temperature coefficient			+25°C	01	-0.02 typical		Δ%/°C
Power supply rejection ratio	PSRR	100 kHz supply noise, see figure 5	+25°C	01	85 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
5 V analog supply current	I_{AVDD5}	V_{IN} = full scale, f_{IN} = 10 MHz, f_S = 500 MSPS	-55°C to +125°C	01		365	mA
3.3 V analog supply current	I_{AVDD3}	V_{IN} = full scale, f_{IN} = 10 MHz, f_S = 500 MSPS	-55°C to +125°C	01		145	mA
3.3 V digital supply current	I_{DVDD3}	V_{IN} = full scale, f_{IN} = 10 MHz, f_S = 500 MSPS	-55°C to +125°C	01		92	mA
Total power dissipation	P_D		-55°C to +125°C	01		2.575	W
Power up time			+25°C	01	200 typical		µs
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f_{IN} = 10 MHz	+25°C	01	65.3 typical		dBFS
		f_{IN} = 70 MHz	+25°C		65.4 typical		
		f_{IN} = 100 MHz	+25°C		63.5		
			-55°C to +125°C		63		
		f_{IN} = 230 MHz	+25°C		65.1 typical		
		f_{IN} = 300 MHz	+25°C		63.25		
			-55°C to +125°C		61.75		
		f_{IN} = 450 MHz	+25°C		64.6 typical		
		f_{IN} = 650 MHz	+25°C		63.9 typical		
		f_{IN} = 900 MHz	+25°C		62.6 typical		
		f_{IN} = 1.3 GHz	+25°C		59.3 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Spurious free dynamic range	SFDR	f_{IN} = 10 MHz	+25°C	01	85 typical		dBc
		f_{IN} = 70 MHz	+25°C		82 typical		
		f_{IN} = 100 MHz	+25°C		70		
			-55°C to +125°C		67		
		f_{IN} = 230 MHz	+25°C		78 typical		
		f_{IN} = 300 MHz	+25°C		64		
			-55°C to +125°C		62		
		f_{IN} = 450 MHz	+25°C		75 typical		
		f_{IN} = 650 MHz	+25°C		65 typical		
		f_{IN} = 900 MHz	+25°C		56 typical		
		f_{IN} = 1.3 GHz	+25°C		45 typical		
Second harmonic	HD2	f_{IN} = 10 MHz	+25°C	01	87 typical		dBc
		f_{IN} = 70 MHz	+25°C		82 typical		
		f_{IN} = 100 MHz	-55°C to +125°C		67		
		f_{IN} = 230 MHz	+25°C		81 typical		
		f_{IN} = 300 MHz	-55°C to +125°C		62.5		
		f_{IN} = 450 MHz	+25°C		80 typical		
		f_{IN} = 650 MHz	+25°C		77 typical		
		f_{IN} = 900 MHz	+25°C		66 typical		
		f_{IN} = 1.3 GHz	+25°C		50 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Third harmonic	HD3	f_{IN} = 10 MHz	+25°C	01	85 typical		dBc
		f_{IN} = 70 MHz	+25°C		90 typical		
		f_{IN} = 100 MHz	-55°C to +125°C		67.5		
		f_{IN} = 230 MHz	+25°C		90 typical		
		f_{IN} = 300 MHz	-55°C to +125°C		63		
		f_{IN} = 450 MHz	+25°C		75 typical		
		f_{IN} = 650 MHz	+25°C		65 typical		
		f_{IN} = 900 MHz	+25°C		56 typical		
		f_{IN} = 1.3 GHz	+25°C		45 typical		
Worst harmonic/spur (other than HD2 and HD3)	HD3	f_{IN} = 10 MHz	+25°C	01	86 typical		dBc
		f_{IN} = 70 MHz	+25°C		86 typical		
		f_{IN} = 100 MHz	+25°C		86 typical		
		f_{IN} = 230 MHz	+25°C		77 typical		
		f_{IN} = 300 MHz	+25°C		81 typical		
		f_{IN} = 450 MHz	+25°C		86 typical		
		f_{IN} = 650 MHz	+25°C		85 typical		
		f_{IN} = 900 MHz	+25°C		78 typical		
		f_{IN} = 1.3 GHz	+25°C		67 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Total harmonic distortion	THD	f_{IN} = 10 MHz	+25°C	01	80 typical		dBc
		f_{IN} = 70 MHz	+25°C		79 typical		
		f_{IN} = 100 MHz	+25°C		77 typical		
		f_{IN} = 230 MHz	+25°C		75 typical		
		f_{IN} = 300 MHz	+25°C		73 typical		
		f_{IN} = 450 MHz	+25°C		73 typical		
		f_{IN} = 650 MHz	+25°C		64 typical		
		f_{IN} = 900 MHz	+25°C		55 typical		
		f_{IN} = 1.3 GHz	+25°C		44 typical		
Signal-to-noise and distortion	SINAD	f_{IN} = 10 MHz	+25°C	01	65.2 typical		dBc
		f_{IN} = 70 MHz	+25°C		65.2 typical		
		f_{IN} = 100 MHz	-55°C to +125°C		62		
		f_{IN} = 230 MHz	+25°C		64.7 typical		
		f_{IN} = 300 MHz	-55°C to +125°C		58.75		
		f_{IN} = 450 MHz	+25°C		64.1 typical		
		f_{IN} = 650 MHz	+25°C		61.5 typical		
		f_{IN} = 900 MHz	+25°C		55.4 typical		
		f_{IN} = 1.3 GHz	+25°C		45.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section – continued.							
Two-tone SFDR		f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, each tone at -7 dBFS	+25°C	01	90 typical		dBc
		f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, each tone at -16 dBFS	+25°C		89 typical		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, each tone at -7 dBFS	+25°C		82 typical		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, each tone at -16 dBFS	+25°C		89 typical		
Effective number of bits	ENOB	f_{IN} = 100 MHz	-55°C to +125°C	01	9.9		Bits
		f_{IN} = 300 MHz	+25°C		10.4 typical		
RMS idle channel noise		Inputs tied to common mode	+25°C	01	0.7 typical		LSB
Low voltage differential signaling (LVDS) digital outputs characteristics section							
Differential output voltage (±)	V_{OD}		+25°C	01	247	454	mV
Common mode output voltage	V_{OC}		-55°C to +125°C	01	1.125	1.375	V
Timing characteristics section		3/					
Aperture delay	t_A		+25°C	01	200 typical		ps
Aperture jitter, rms			+25°C	01	160 typical		fs
Latency			+25°C	01	3.5 typical		Cycles
Clock period	t_{CLK}		-55°C to +125°C	01	2		ns
Clock pulse duration, high	t_{CLKH}		-55°C to +125°C	01	1		ns
Clock pulse duration, low	t_{CLKL}		-55°C to +125°C	01	1		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics section – continued. 3/							
CLK to DRY delay 4/	t_{DRY}	Zero crossing, 7 pF differential loading	+25°C	01	1100 typical		ps
CLK to DATA/OVR 4/ delay	t_{DATA}	Zero crossing, 7 pF differential loading	+25°C	01	1100 typical		ps
DRY to DATA skew	t_{SKEW}	t_{DATA} - t_{DRY}, 7 pF differential loading	+25°C	01	0 typical		ps
DRY/DATA/OVR rise time	t_{RISE}	7 pF differential loading	+25°C	01	500 typical		ps
DRY/DATA/OVR fall time	t_{FALL}	7 pF differential loading	+25°C	01	500 typical		ps

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, sampling rate = 500 MSPS, 50 % clock duty cycle, AV_{DD5} = 5 V, AV_{DD3} = 3.3 V, DV_{DD3} = 3.3 V, -1 dbFS differential input, and 3 V_{PP} differential clock.

3/ Timing parameters assured by design or characterization, but not production tested.

4/ DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the data propagation delay.

Case X

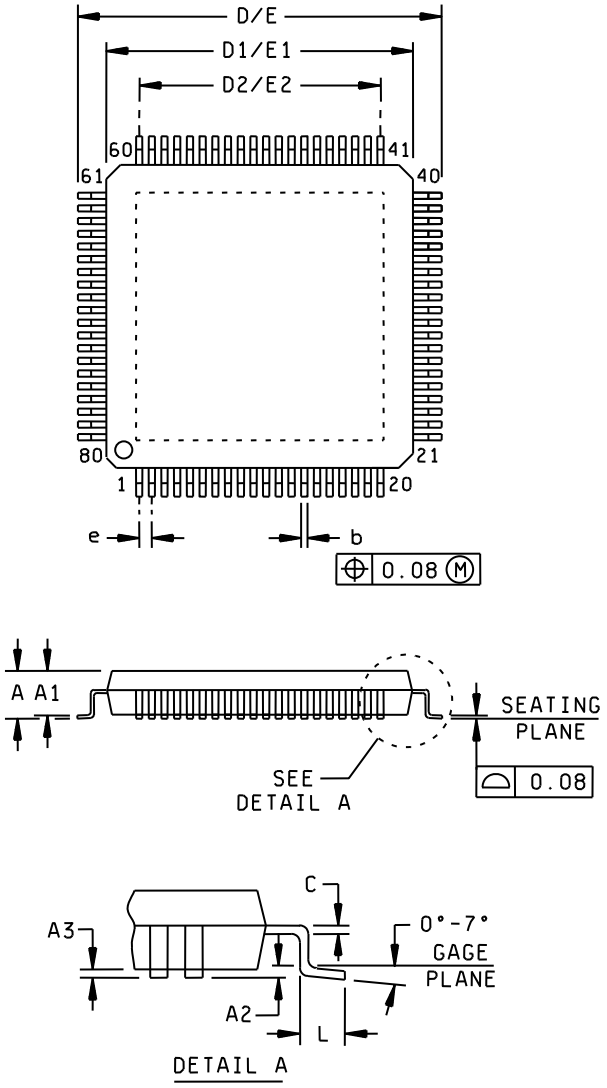

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.037	0.041	0.95	1.05
A2	0.009	---	0.25	---
A3	0.001	0.005	0.05	0.15
b	0.006	0.010	0.17	0.27
c	0.005 nominal		0.13 nominal	
D	0.543	0.559	13.80	14.20
D1	0.464	0.480	11.80	12.20
D2	0.037	---	0.95	---
e	0.019 BSC		0.50 BSC	
E	0.543	0.559	13.80	14.20
E1	0.464	0.480	11.80	12.20
E2	0.037	---	0.95	---
L	0.017	0.029	0.45	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout. The vendor datasheet is available from the manufacturer.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outline – continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DV_{DD3}	21	AV_{DD5}	41	$\overline{OVR}$	61	$\overline{D4}$
2	GND	22	GND	42	OVR	62	D4
3	AV_{DD5}	23	AV_{DD5}	43	NC	63	$\overline{D5}$
4	NC	24	GND	44	NC	64	D5
5	NC	25	AV_{DD5}	45	NC	65	GND
6	V_{REF}	26	GND	46	NC	66	DV_{DD3}
7	GND	27	AV_{DD5}	47	NC	67	$\overline{D6}$
8	AV_{DD5}	28	GND	48	NC	68	D6
9	GND	29	RESERVED	49	NC	69	$\overline{D7}$
10	CLK	30	GND	50	NC	70	D7
11	$\overline{CLK}$	31	AV_{DD5}	51	DV_{DD3}	71	$\overline{D8}$
12	GND	32	GND	52	GND	72	D8
13	AV_{DD5}	33	RESERVED	53	$\overline{D0}$	73	$\overline{D9}$
14	AV_{DD5}	34	GND	54	D0	74	D9
15	GND	35	AV_{DD3}	55	$\overline{D1}$	75	$\overline{D10}$
16	AIN	36	GND	56	D1	76	D10
17	$\overline{AIN}$	37	AV_{DD3}	57	$\overline{D2}$	77	$\overline{D11}$ (MSB)
18	GND	38	GND	58	D2	78	D11 (MSB)
19	AV_{DD5}	39	AV_{DD3}	59	$\overline{D3}$	79	$\overline{DRY}$
20	GND	40	GND	60	D3	80	DRY

NC = No connection

FIGURE 2. Terminal connections.

Terminal symbol	Description
AIN	Differential input signal (positive).
$\overline{\text{AIN}}$	Differential input signal (negative).
AV_{DD5}	Analog power supply (5 V).
AV_{DD3}	Analog power supply (3.3 V). (Suggestion for ≤ 250 MSPS: leave option to connect to 5 V for ADS5440/4 compatibility).
DV_{DD}	Output driver power supply (3.3 V).
GND	Ground.
CLK	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	Differential input clock (negative).
D0, $\overline{\text{D0}}$	LVDS digital output pair, least-significant bit (LSB).
D1 – D10, $\overline{\text{D1}}$ - $\overline{\text{D10}}$	LVDS digital output pairs.
D11, $\overline{\text{D11}}$	LVDS digital output pair, most significant bit (MSB).
DRY, $\overline{\text{DRY}}$	Data ready LVDS output pair.
NC	No connect. Pins 4 and 5 should be left floating, pins 43 – 50 are possible future bit additions for this pin out and therefore can be connected to a digital bus or left floating.
OVR, $\overline{\text{OVR}}$	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
RESERVED	Pin 29 reserved for possible future V_{CM} output for this pinout; pin 33 is reserved for possible future power down control pin for this pinout.
V_{REF}	Reference voltage.

FIGURE 2. Terminal connections – continued.

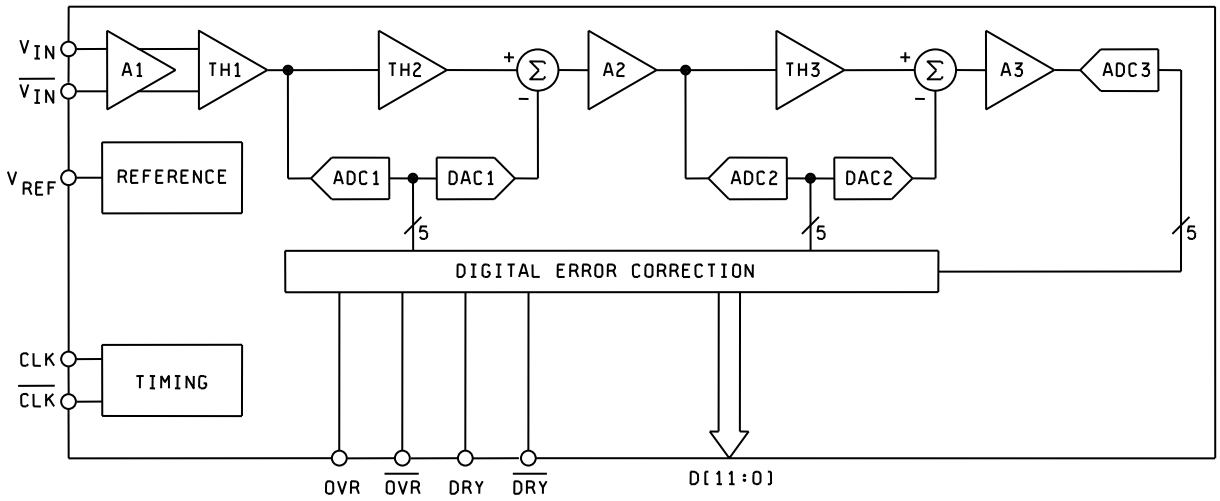

FIGURE 3. Block diagram.

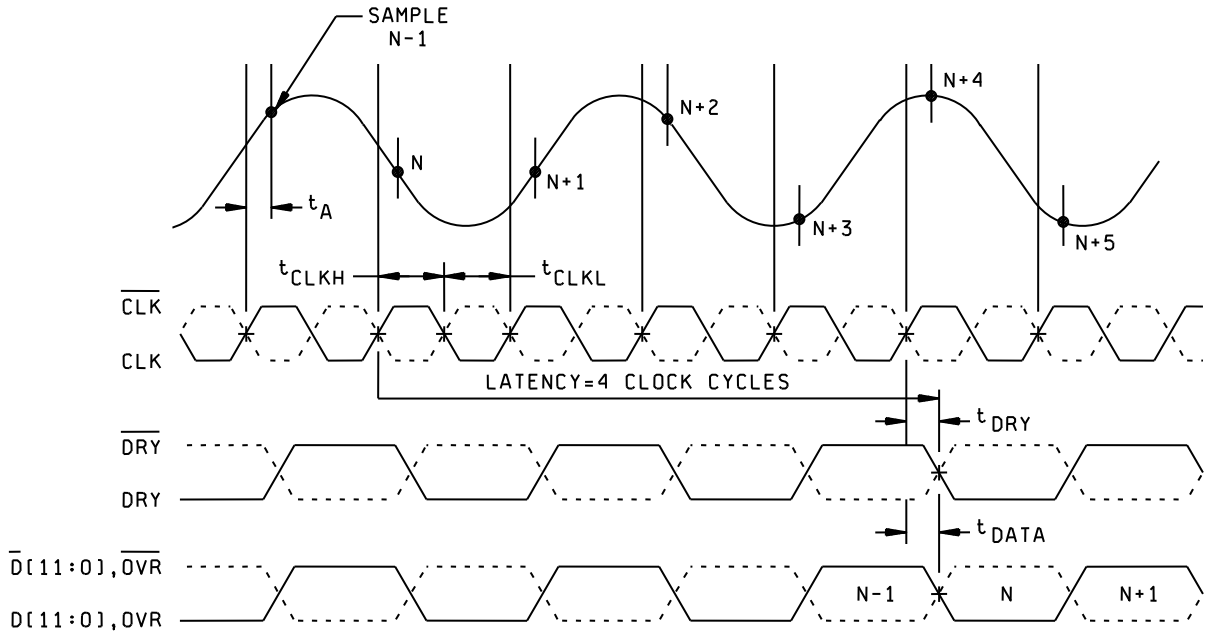

FIGURE 4. Timing waveforms.

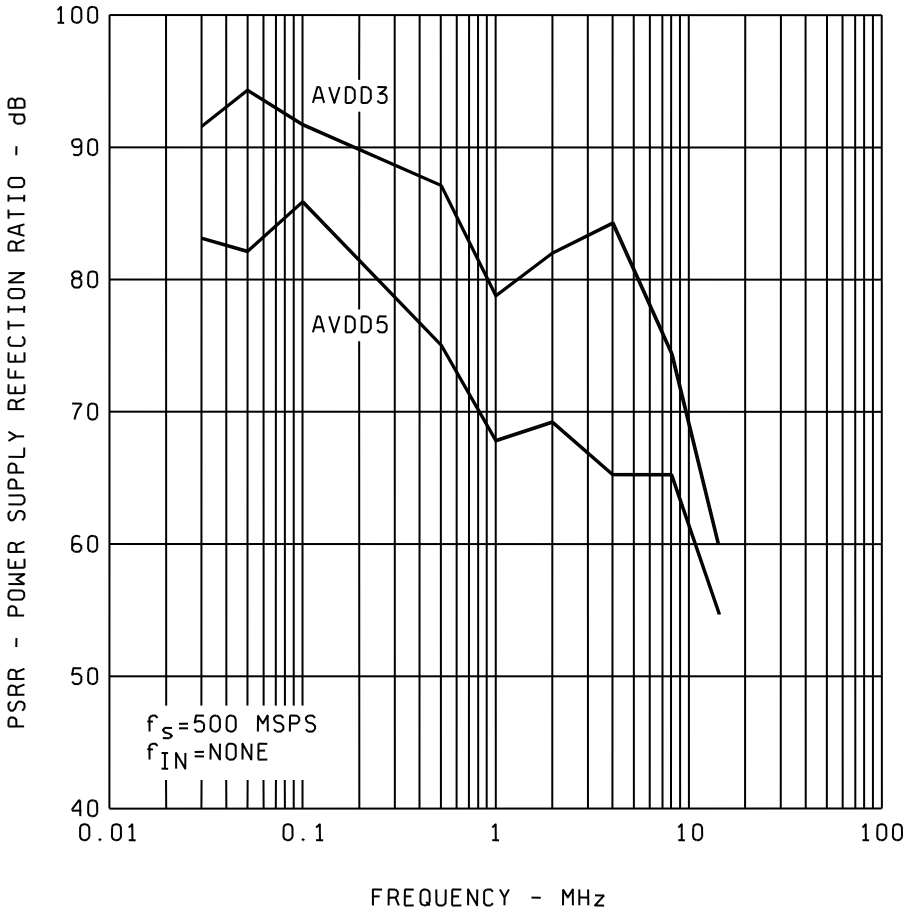

FIGURE 5. PSRR versus supply injected frequency.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/ lead	Mode of transportation and quantity	Package marking	Vendor part number
V62/07607-01XE	01295	HTQFP-80 (thermal pad)	Tray, 96	ADS5463MEP	ADS5463MPFPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Thermal pad size: 9.5 mm x 9.5 mm (0.374 inch) minimum, 10 mm x 10 mm (0.393 inch) maximum.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243