

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add reference information to section 2. Make change to notes specified under figure 1. Update boilerplate paragraphs to current requirements. - ro	11-12-01	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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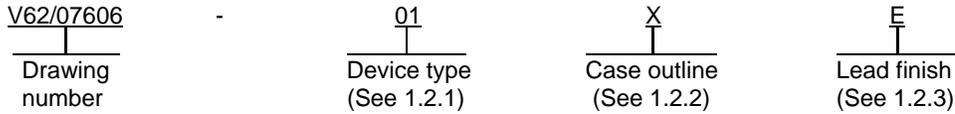
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	PREPARED BY RICK OFFICER					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990													
Original date of drawing YY-MM-DD 06-11-15	CHECKED BY TOM HESS					TITLE MICROCIRCUIT, LINEAR, DUAL, HIGH SPEED, LOW NOISE, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON													
	APPROVED BY RAYMOND MONNIN																		
	SIZE A	CODE IDENT. NO. 16236				DWG NO. V62/07606													
	REV A					PAGE 1 OF 10													

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, high speed, low noise, operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	MC33078-EP	Dual, high speed, low noise, operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 2

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V _{CC+})	+18 V maximum	2/
Negative supply voltage (V _{CC-})	-18 V maximum	2/
Supply voltage (V _{CC-} to V _{CC+})	36 V maximum	
Input voltage, either input	V _{CC-} to V _{CC+} maximum	2/ 3/
Input current	±10 mA maximum	4/
Duration of output short circuit	Unlimited	5/
Package thermal impedance (θ _{JA})	97°C/W	6/ 7/
Operating virtual junction temperature (T _J)	+150°C	
Storage temperature range (T _{STG})	-65°C to +150°C	8/

1.4 Recommended operating conditions. 9/

Positive supply voltage range (V _{CC+})	+5 V to +18 V
Negative supply voltage range (V _{CC-})	-5 V to -18 V
Operating free-air temperature range (T _A)	-55°C to +125°C

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 2/ All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
 - 3/ The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
 - 4/ Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
 - 5/ The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
 - 6/ Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 7/ The package thermal impedance is calculated in accordance with JESD 51-7.
 - 8/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer’s website for additional information on enhanced plastic packaging.
 - 9/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/07606</p>
		<p>REV A</p>	<p>PAGE 4</p>

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_{CC-} = -15\text{ V}$, $V_{CC+} = +15\text{ V}$ unless otherwise specified	Temperature, T_A	Device type	Limits		Unit		
					Min	Max			
Input offset voltage	V_{IO}	$V_O = 0$, $R_S = 10\ \Omega$, $V_{CM} = 0$	+25°C	01		2	mV		
			-55°C to +125°C			3			
Input offset voltage temperature coefficient	αV_{IO}	$V_O = 0$, $R_S = 10\ \Omega$, $V_{CM} = 0$	-55°C to +125°C	01	2 typical		$\mu\text{V}/^\circ\text{C}$		
Input bias current	I_{IB}	$V_O = 0$, $V_{CM} = 0$	+25°C	01		750	nA		
			-55°C to +125°C			800			
Input offset current	I_{IO}	$V_O = 0$, $V_{CM} = 0$	+25°C	01		150	nA		
			-55°C to +125°C			175			
Common mode input voltage range	V_{ICR}	$\Delta V_{IO} = 5\text{ mV}$, $V_O = 0$	-55°C to +125°C	01	± 13		V		
Large signal differential voltage amplification	A_{VD}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	+25°C	01	90		dB		
			-55°C to +125°C		80				
Maximum output voltage swing	V_{OM+}	$V_{ID} = \pm 1\text{ V}$, $R_L = 600\ \Omega$	+25°C	01	10.7 typical		V		
	V_{OM-}				-11.9 typical				
	V_{OM+}	$V_{ID} = \pm 1\text{ V}$, $R_L = 2\text{ k}\Omega$	+25°C		13.2				
	V_{OM-}				-13.2				
	V_{OM+}				$V_{ID} = \pm 1\text{ V}$, $R_L = 10\text{ k}\Omega$	+25°C		13.5	
	V_{OM-}							-14	
Common mode rejection ratio	CMRR	$V_{IN} = \pm 13\text{ V}$	+25°C	01	80		dB		
Supply voltage <u>2/</u> rejection ratio	k_{SVR}	$V_{CC+} = +5\text{ V}$ to +15 V, $V_{CC-} = -5\text{ V}$ to -15 V	+25°C	01	80		dB		
Output short circuit current	I_{OS}	$ V_{ID} = 1\text{ V}$, output to GND, source current	+25°C	01	15		mA		
		$ V_{ID} = 1\text{ V}$, output to GND, sink current			-20				

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_{CC-} = -15\text{ V}$, $V_{CC+} = +15\text{ V}$ unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current (per channel)	I _{CC}	$V_O = 0$	+25°C	01		2.5	mA
			-55°C to +125°C			3.5	
Slew rate at unity gain	SR	$A_{VD} = 1$, $V_{IN} = -10\text{ V to }10\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	+25°C	01	5		V/ μ s
Gain bandwidth product	GBW	$f = 100\text{ kHz}$	+25°C	01	16 typical		MHz
Unity gain frequency	B ₁	Open loop	+25°C	01	9 typical		MHz
Gain margin		$R_L = 2\text{ k}\Omega$, $C_L = 0\text{ pF}$	+25°C	01	-11 typical		dB
		$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$			-6 typical		
Phase margin	ϕ_m	$R_L = 2\text{ k}\Omega$, $C_L = 0\text{ pF}$	+25°C	01	55 typical		°
		$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$			40 typical		
Amplifier-to-amplifier isolation		$f = 20\text{ Hz to }20\text{ kHz}$	+25°C	01	-120 typical		dB
Power bandwidth		$V_O = 27\text{ V}_{(PP)}$, $R_L = 2\text{ k}\Omega$, THD $\leq 1\%$	+25°C	01	120 typical		kHz
Total harmonic distortion	THD	$V_O = 3\text{ V}_{rms}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $f = 20\text{ Hz to }20\text{ kHz}$	+25°C	01	0.002 typical		%
Open loop output impedance	z _O	$V_O = 0$, $f = 9\text{ MHz}$	+25°C	01	37 typical		Ω
Differential input resistance	r _{id}	$V_{CM} = 0$	+25°C	01	175 typical		k Ω
Differential input capacitance	C _{id}	$V_{CM} = 0$	+25°C	01	12 typical		pF
Equivalent input noise voltage	V _n	$f = 1\text{ kHz}$, $R_S = 100\ \Omega$	+25°C	01	4.5 typical		nV / $\sqrt{\text{Hz}}$
Equivalent input noise current	I _n	$f = 1\text{ kHz}$	+25°C	01	0.5 typical		pA / $\sqrt{\text{Hz}}$

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Measured with $V_{CC\pm}$ differentially varied at the same time.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 6

Case X

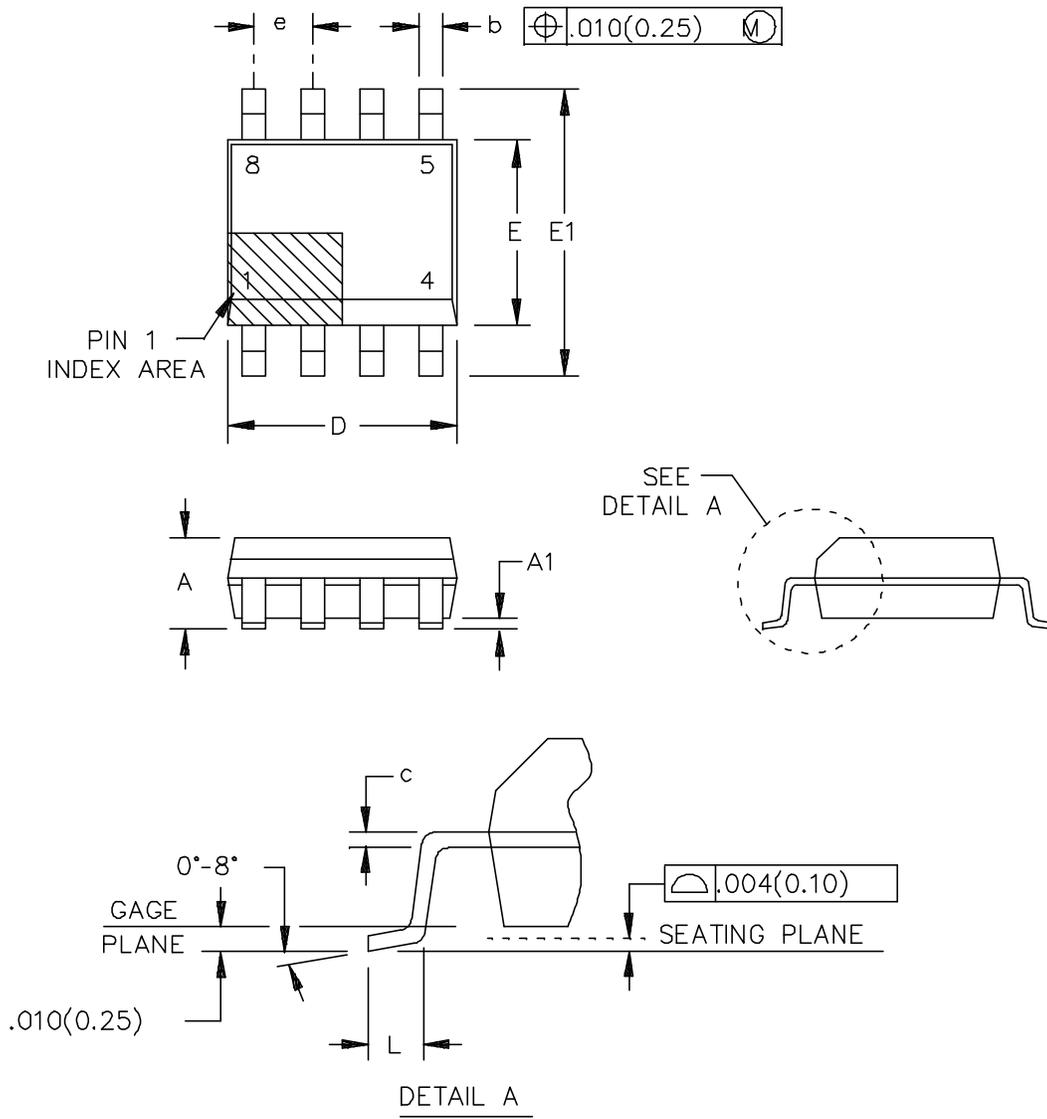


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/07606</p>
		<p>REV A</p>	<p>PAGE 7</p>

Case X - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012 variation AA.

FIGURE 1. Case outline – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 8

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT1
2	IN1-
3	IN1+
4	VCC-
5	IN2+
6	IN2-
7	OUT2
8	VCC+

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 9

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package	Top side marking	Vendor part number
V62/07606-01XE	01295	Reel of 2500	33078M	MC33078MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available from manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Ln.
 PO Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07606
		REV A	PAGE 10