REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-08-25	Thomas M. Hess
B	Update document paragraphs to current requirements. - ro	21-07-08	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B	B																	
PAGE	18	19	20	21																	

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-11-01	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 10 MHz TO 66 MHz, 10:1 LVDS SERIALIZER/DESERIALIZER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06677**
	REV B	**PAGE** 1 **OF** 21

AMSC N/A

5962-V047-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 10 MHz to 66 MHz, 10:1 LVDS serializer/deserializer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06677	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65LV1023A-EP	10 MHz to 66 MHz, 10:1 LVDS serializer
02	SN65LV1224B-EP	10 MHz to 66 MHz, 10:1 LVDS deserializer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	28	MO-187	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC} to GND)	-0.3 V to 4.0 V
LVTTL input voltage	-0.3 V to V_{CC} + 0.3 V
LVTTL output voltage	-0.3 V to V_{CC} + 0.3 V
LVDS receiver input voltage	-0.3 V to 3.9 V
LVDS driver output voltage	-0.3 V to 3.9 V
LVDS output short circuit duration	10 ms
Electrostatic discharge:	
Human body model (HBM)	up to 6 kV
Machine model (MM)	up to 200 V
Junction temperature	150°C
Storage temperature	-65°C to 150°C 2/
Lead temperature (soldering, 4 seconds)	260°C
Maximum package power dissipation (T_A = 25°C)	1.27 W
Package derating	10.8 mW/°C above 25°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	3.0 V to 3.6 V 3/
Receiver input voltage range	0 V to 2.4 V
Receiver input common mode range	$\frac{V_{ID}}{2}$ to 2.4 - $\left(\frac{V_{ID}}{2}\right)$ V
Maximum supply noise voltage	100 mVp-p
Operating free air temperature	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Long term high temperature storage and/or extended use at maximum operating conditions may result in a reduction of overall device life.

3/ By design, DV_{CC} and AV_{CC} are separated internally and does not matter what the difference is for $|DV_{CC}-AV_{CC}|$, as long as both are within 3 V to 3.6 V.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Deserializer truth table. The deserializer truth table shall be as shown in figure 3.

3.5.4 Block diagrams. The block diagrams shall be as shown in figure 4.

3.5.5 Timing diagrams and test circuits. The timing diagrams and test circuits shall be as shown in figures 5 through 23.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ Device type: All Unless otherwise specified	Limits		Unit
			Min	Max	
Serializer LVCMOS/LVTTL DC specifications 2/					
High level input voltage	V_{IH}		2	V_{CC}	V
Low level input voltage	V_{IL}		GND	0.8	V
Input clamp voltage	V_{CL}	I_{CL} = -18 mA		-1.5	V
Input current 3/	I_{IN}	V_{IN} = 0 V to 3.6 V	-200	200	µA
Deserializer LVCMOS/LVTTL DC specifications					
High level input voltage	V_{IH}		2	V_{CC}	V
Low level input voltage	V_{IL}		GND	0.8	V
Input clamp voltage	V_{CL}	I_{CL} = -18 mA		-1.5	V
Input current (pull-up and pull-down resistors on inputs)	I_{IN}	V_{IN} = 0 V to 3.6 V	-200	200	µA
High level output voltage	V_{OH}	I_{OH} = -5 mA	2.2	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 5 mA	GND	0.5	V
Output short circuit current	I_{OS}	V_{OUT} = 0 V		-85	mA
High impedance output current	I_{OZ}	$\overline{PWRDN}$ or REN = 0.8 V, V_{OUT} = 0 V or V_{CC}	-10	10	µA
Serializer LVDS DC specifications (Apply to pins DO+ and DO–)					
Output differential voltage (DO+)-(DO-)	V_{OD}	R_L = 27 Ω, See figure 22	350		mV
Output differential voltage unbalance	ΔV_{OD}			35	mV
Offset voltage	V_{OS}		1.1	1.3	V
Offset voltage unbalance	ΔV_{OS}			35	mV
Output short circuit current	I_{OS}	D0 = 0 V, D_{INx} = high, $\overline{PWRDN}$ and DEN = 2.4 V		-90	mA
High impedance output current	I_{OZ}	$\overline{PWRDN}$ or DEN = 0.8 V, D0 = 0 V or V_{CC}	-10	10	µA
Power off output current	I_{OX}	V_{CC} = 0 V, DO = 0 V or 3.6 V	-20	25	µA
Output single ended capacitance	C_O		1 typical		pF
Deserializer LVDS DC specifications (Apply to pins RI+ and RI–)					
Differential threshold high voltage	V_{TH}	V_{CM} = 1.1 V		50	mV
Differential threshold low voltage	V_{TL}		-50		mV
Input current	I_{IN}	V_{IN} = 2.4 V, V_{CC} = 3.6 V or 0 V	-10	15	µA
		V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V	-10	10	
Input single ended capacitance	C_I		0.5 typical		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ Device type: All Unless otherwise specified		Limits		Unit
				Min	Max	
Serializer supply current (applies to pins DV_{CC} and AV_{CC})						
Serializer supply current worst case	I_{CCD}	R_L = 27 Ω, See figure 7	f = 10 MHz		25	mA
			f = 66 MHz		70	
Serializer supply current	I_{CCXD}	$\overline{PWRDN}$ = 0.8 V			500	µA
Deserializer supply current (applies to pins DV_{CC} and AV_{CC})						
Deserializer supply current worst case	I_{CCR}	C_L = 15 pF, See figure 7	f = 10 MHz		35	mA
			f = 66 MHz		95	
Deserializer supply current, power down	I_{CCXR}	$\overline{PWRDN}$ = 0.8 V, REN = 0.8 V			1	mA
Serializer timing requirement for TCLK						
Transmit clock period	t_{TCP}			15.15	100	ns
Transmit clock high time	t_{TCIH}			0.4T	0.6T	ns
Transmit clock low time	t_{TCIL}			0.4T	0.6T	ns
TCLK input transition time	$T_{t(CLK)}$				6	ns
TCLK input jitter	t_{JIT}	See figure 21			150	ps (RMS)
Frequency tolerance				-100	+100	ppm
Serializer switching characteristics						
LVDS low to high transition time	$t_{TLH(L)}$	R_L = 27 Ω, C_L = 10 pF to GND, See figure 8		0.2 typical		ns
LVDS high to low transition time	$t_{THL(L)}$			0.25 typical		ns
DIN0-DIN9 setup to TCLK	$t_{su(DI)}$	R_L = 27 Ω, C_L = 10 pF to GND, See figure 11		0.5		ns
DIN0-DIN9 hold from TCLK	$t_{h(DI)}$			4		
DO± high to high impedance state delay	$t_{d(HZ)}$	R_L = 27 Ω, C_L = 10 pF to GND, See figure 12		2.5 typical		ns
DO± low to high impedance state delay	$t_{d(LZ)}$			2.5 typical		ns
DO± high to high impedance state to high delay	$t_{d(ZH)}$			5 typical		ns
DO± high to high impedance state to low delay	$t_{d(ZL)}$			6.5 typical		ns
SYNC pulse duration	$t_{w(SPW)}$	R_L = 27 Ω, See figure 14		6xt_{TCP}		ns
Serializer PLL lock time	$t_{(PLD)}$			1026xt_{TCP}		ns
Serializer delay	$t_{d(S)}$	R_L = 27 Ω, See figure 15		t_{TCP}	t_{TCP}+3	ns
Deterministic jitter	t_{DJIT}	R_L = 27 Ω, C_L = 10 pF to GND		230 typical		ps
				150 typical		
Random jitter	t_{RJIT}	R_L = 27 Ω, C_L = 10 pF to GND		10 typical		ps (RMS)

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ Device type: All Unless otherwise specified		Limits		Unit
				Min	Max	
Deserializer timing requirement for REFCLK						
REFCLK period	t_{RFCP}			15.15	100	ns
REFCLK duty cycle	t_{RFDC}			30%	70%	
REFCLK transition time	$t_{t(RF)}$				6	ns
Frequency tolerance				-100	+100	ppm
Deserializer switching characteristics						
Receiver out clock period	$t_{(RCP)}$	$t_{(RCP)} = t_{(TCP)}$, See figure 15	RCLK	15.15	100	ns
CMOS/TTL low to high transition time	$t_{TLH(C)}$	C_L = 15 pF, See figure 9	R_{OUT0}-R_{OUT9}, $\overline{LOCK}$, RCLK	1.2 typical		ns
CMOS/TTL high to low transition time	$t_{THL(C)}$			1.1 typical		ns
Deserializer delay	$t_{d(D)}$ 5/	T_A = 25°C, 3.3 V See figure 16	10 MHz	$1.75xt_{(RCP)}+4.2$	$1.75xt_{(RCP)}+12.6$	ns
			66 MHz	$1.75xt_{(RCP)}+7.4$	$1.75xt_{(RCP)}+9.7$	
R_{OUTx} data valid before RCLK	$t_{(ROS)}$	See figure 17	RCLK 10 MHz	$0.4xt_{(RCP)}$		ns
			RCLK 66 MHz	$0.4xt_{(RCP)}$		
R_{OUTx} data valid after RCLK	$t_{(ROH)}$		10 MHz	$-0.4xt_{(RCP)}$		ns
			66 MHz	$-0.4xt_{(RCP)}$		
RCLK duty cycle	$t_{(RDC)}$			40%	60%	ns
High to high impedance state delay	$t_{d(HZ)}$	See figure 18	R_{OUT0}-R_{OUT9}	6.5 typical		ns
Low to high impedance state delay	$t_{d(LZ)}$			4.7 typical		ns
High impedance state to high delay	$t_{d(HR)}$			5.3 typical		ns
High impedance state to low delay	$t_{d(ZL)}$			4.7 typical		ns
Deserilaizer PLL lock time from $\overline{PWRDN}$ (with SYNCPAT)	$t_{(DRS1)}$	See figure 19 and 20 6/	10 MHz		$850xt_{RFCP}$	µs
			66 MHz		$850xt_{RFCP}$	
Deserilaizer PLL lock time from SYNCPAT	$t_{(DRS2)}$		10 MHz		2	µs
			66 MHz		0.303	
High impedance state to high delay (power up)	$t_{d(ZHLK)}$		$\overline{LOCK}$		3	ns
Deserializer noise margin	t_{RNM}	See figure 21 7/	10 MHz	3680 typical		ps
			66 MHz	540 typical		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Apply to D_{IN0}-D_{IN9}, TCLK, $\overline{PWRDN}$, TCLK_R/$\overline{F}$, SYNC1, SYNC2, and DEN.

3/ High I_{IN} values are due to pullup and pulldown resistors on the inputs.

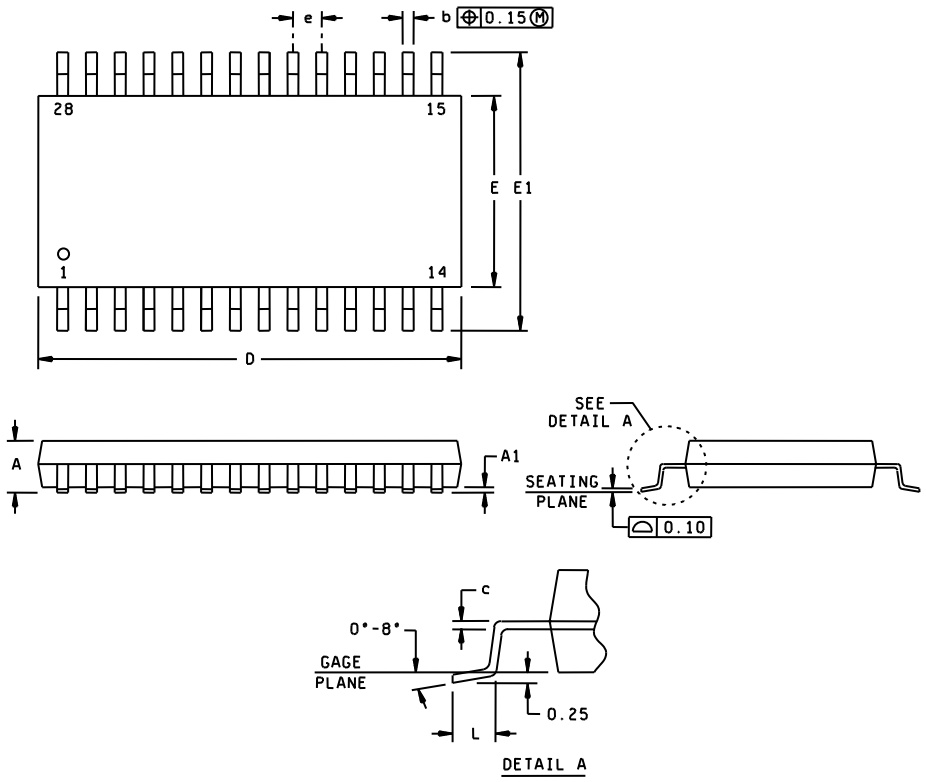
4/ Apply to pins $\overline{PWRDN}$, RCLK_R/$\overline{F}$, REN, and REFCLK = inputs; apply to pins R_{OUTx}, RCLK, and $\overline{LOCK}$ = outputs (see deserializer truth table)

5/ The deserializer delay time for all frequencies does not exceed two serial bit times.

6/ $t_{(DSR1)}$ represents the time required for the deserialzer to register that a lock has occurred upon power up or when leaving the power down mode. $t_{(DSR2)}$ represents the time required to register that a lock has occurred for power up and enabled deserializer when the input (RI±) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). In order to specify deserializer PLL performance, $t_{(DSR1)}$ and $t_{(DSR2)}$ are specified with REFCLK active and stable and specific conditions of SYNCPATs.

7/ t_{RNM} represents the phase noise or jitter that the deserializer can withstand in the incoming data stream before bit errors occur.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		2.00	E	5.00	5.60
A1	0.05		E1	7.40	8.20
b	0.22	0.38	e	0.65 BSC	
c	0.09	0.25	L	0.55	0.95
D	9.90	10.50			

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion.
3. Falls within JEDEC MO-187 variation DA.

FIGURE 1. Case outline.

Case X

Device type 01			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	SYNC1	15	DGND
2	SYNC2	16	DGND
3	D_{IN0}	17	AV_{CC}
4	D_{IN1}	18	AGND
5	D_{IN2}	19	DEN
6	D_{IN3}	20	AGND
7	D_{IN4}	21	DO-
8	D_{IN5}	22	DO+
9	D_{IN6}	23	AGND
10	D_{IN7}	24	$\overline{PWRDN}$
11	D_{IN8}	25	AGND
12	D_{IN9}	26	AV_{CC}
13	TCLK_R/$\overline{F}$	27	DV_{CC}
14	TCLK	28	DV_{CC}

Device type 02			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	15	R_{OUT9}
2	RCLK_R/$\overline{F}$	16	R_{OUT8}
3	REFCLK	17	R_{OUT7}
4	AV_{CC}	18	R_{OUT6}
5	$R_{I}+$	19	R_{OUT5}
6	$R_{I}–$	20	DGND
7	$\overline{PWRDN}$	21	DV_{CC}
8	REN	22	DGND
9	RCLK	23	DV_{CC}
10	$\overline{LOCK}$	24	R_{OUT4}
11	AV_{CC}	25	R_{OUT3}
12	AGND	26	R_{OUT2}
13	AGND	27	R_{OUT1}
14	DGND	28	R_{OUT0}

FIGURE 2. Terminal connections.

Inputs		Outputs		
$\overline{PWRDN}$	REN	ROUT(0:9) 1/.	$\overline{LOCK}$ 2/	RCLK 1/ 3/
H	H	Z	H	Z
H	H	Active	L	Active
L	X	Z	Z	Z
H	L	Z	Active	Z

1/ ROUT and RCLK are 3-stated when $\overline{LOCK}$ is asserted high.

2/ $\overline{LOCK}$ output reflects the state of the deserializer with regard to the selected data stream

3/ RCLK active indicates the RCLK is running if the deserializer is locked. The timing of RCLK with respect to ROUT is determined by RCLK_R/$\overline{F}$.

FIGURE 3. Deserializer truth table.

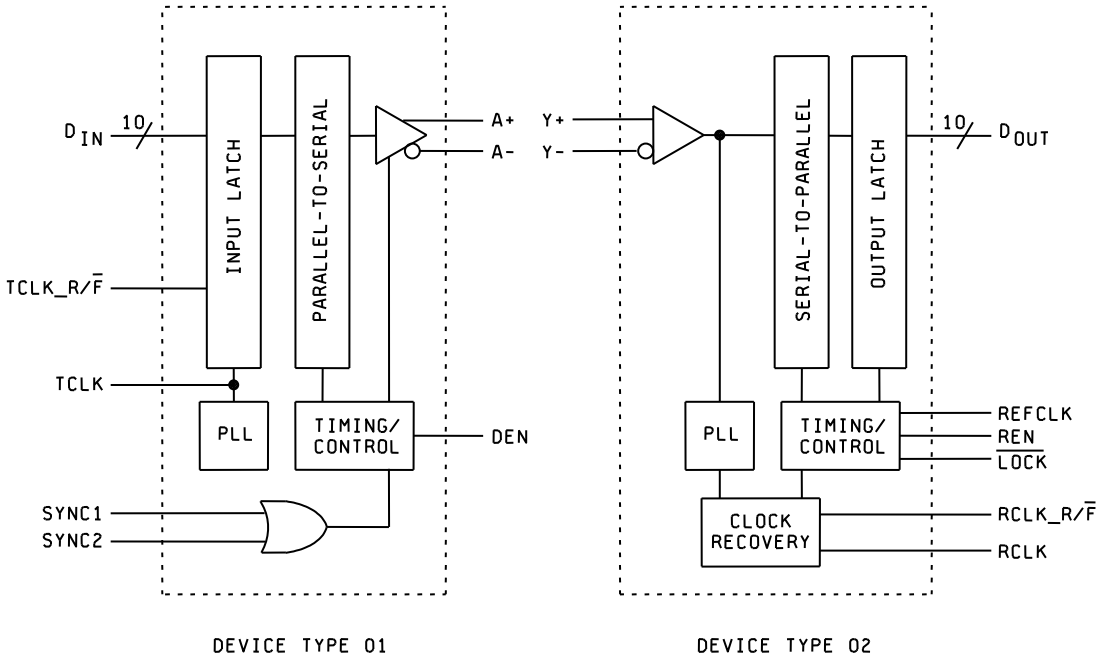


FIGURE 4. Block diagrams.

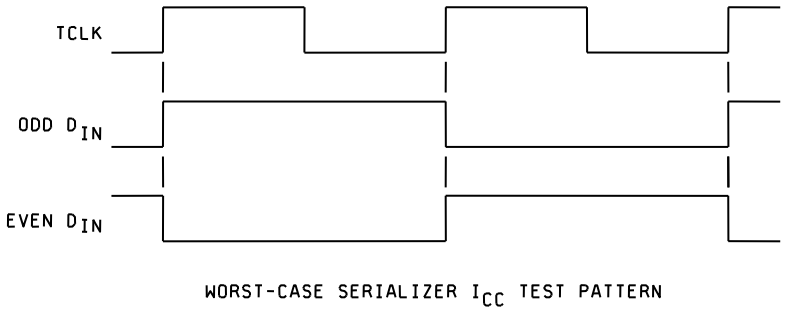
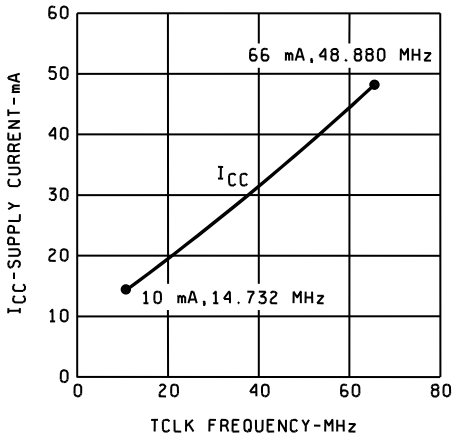
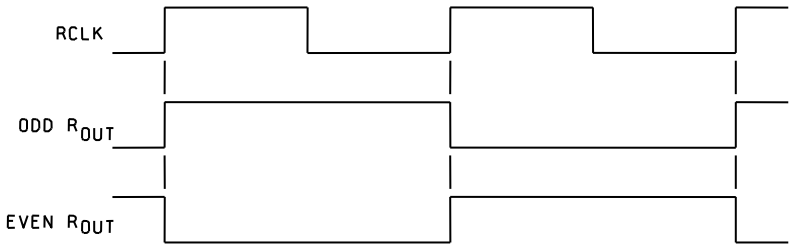


FIGURE 5. Timing diagrams and test circuits.



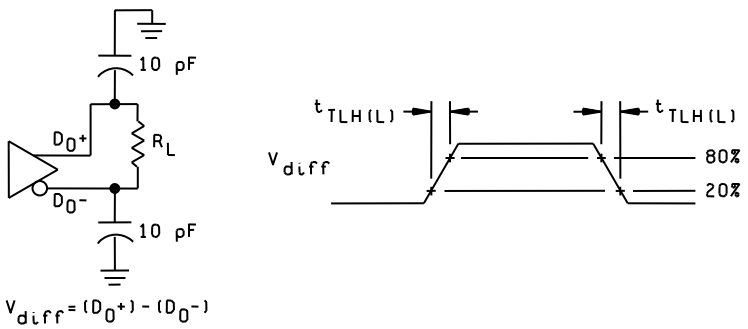
SUPPLY CURRENT
vs
TCLK FREQUENCY

FIGURE 6 Timing diagrams and test circuits.



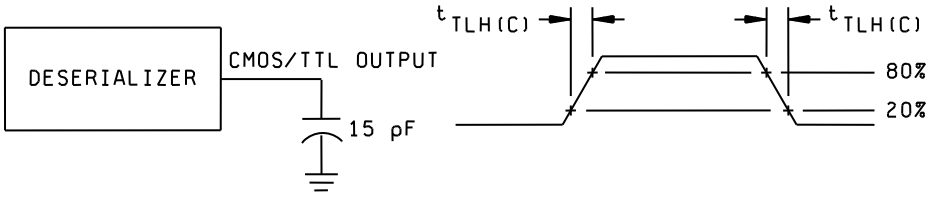
WORST-CASE DESERIALIZER I_{CC} TEST PATTERN

FIGURE 7 Timing diagrams and test circuits.



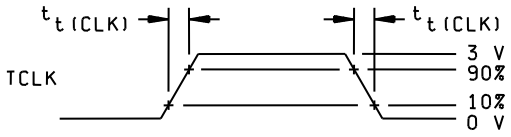
SERIALIZER LVDS OUTPUT LOAD AND TRANSITION TIMES

FIGURE 8 Timing diagrams and test circuits.



DESERIALIZER CMOS/TTL OUTPUT LOAD AND TRANSITION TIMES

FIGURE 9 Timing diagrams and test circuits.



SERIALIZER INPUT CLOCK TRANSITION TIMES

FIGURE 10 Timing diagrams and test circuits.

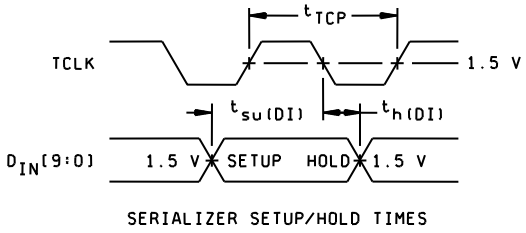


FIGURE 11 Timing diagrams and test circuits.

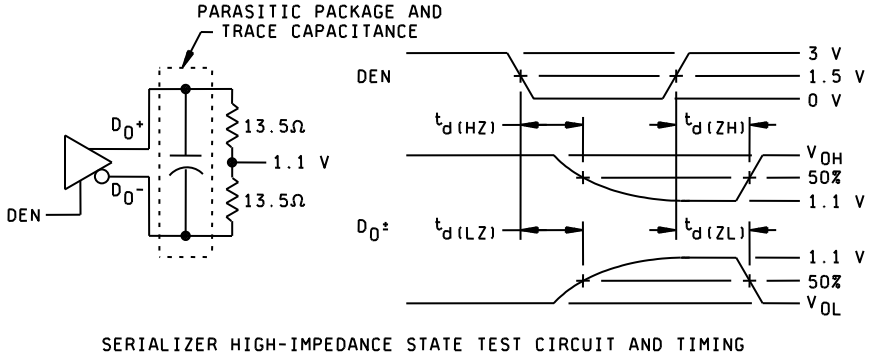


FIGURE 12 Timing diagrams and test circuits.

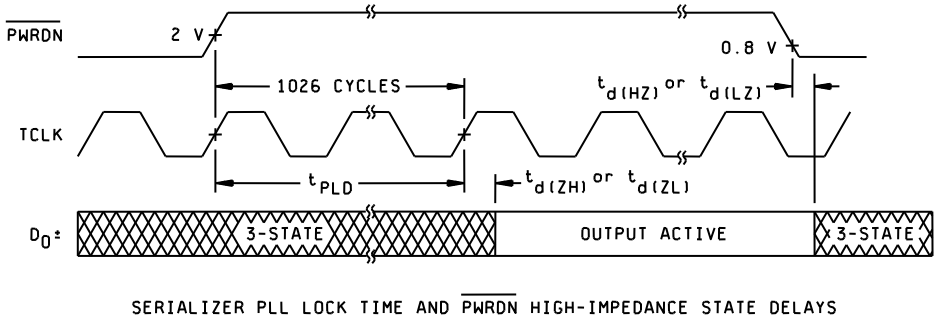


FIGURE 13 Timing diagrams and test circuits.

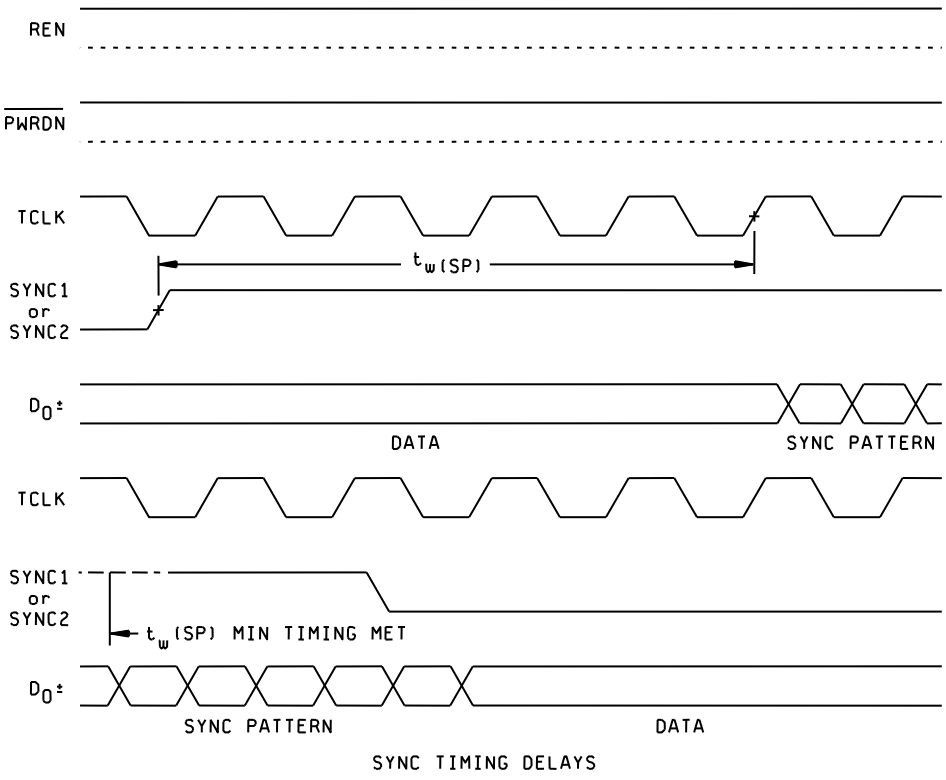


FIGURE 14 Timing diagrams and test circuits.

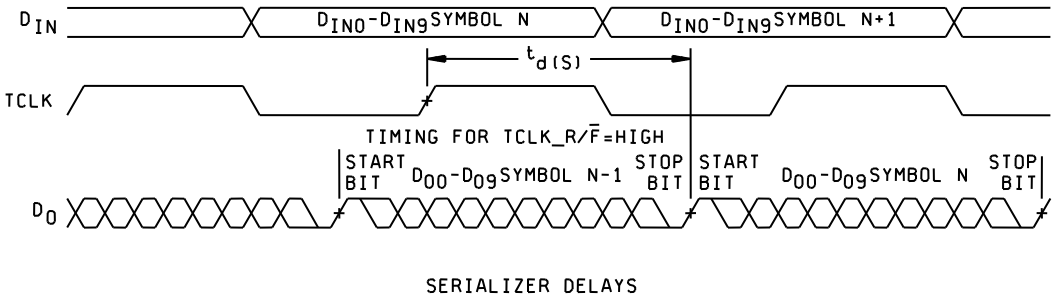


FIGURE 15 Timing diagrams and test circuits.

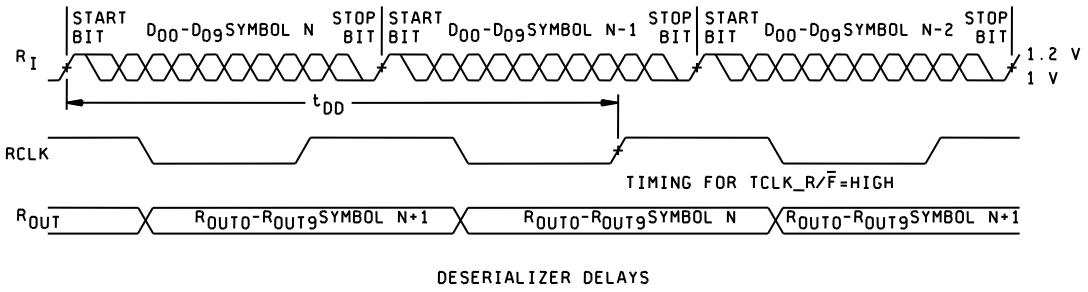


FIGURE 16 Timing diagrams and test circuits.

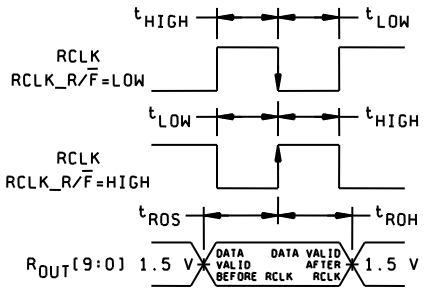
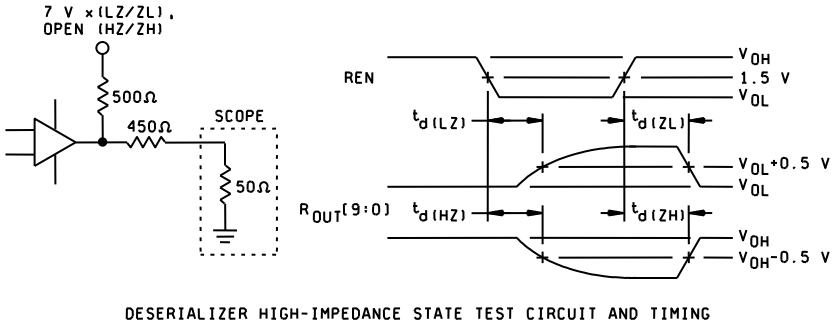
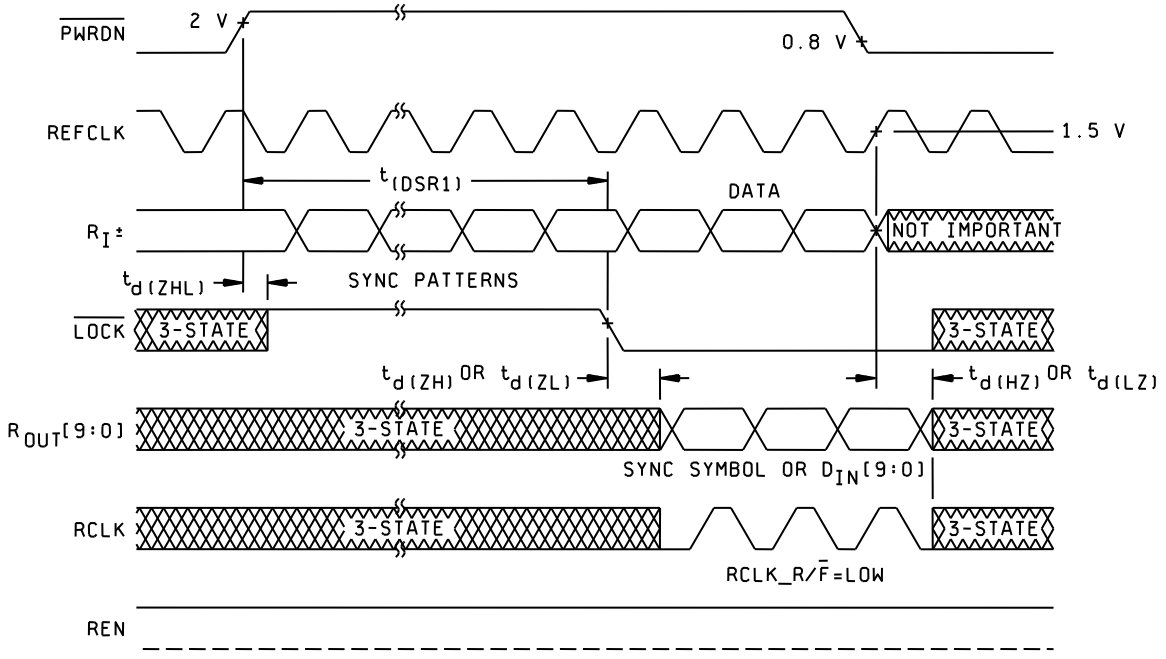


FIGURE 17 Timing diagrams and test circuits.



DESERIALIZER HIGH-IMPEDANCE STATE TEST CIRCUIT AND TIMING

FIGURE 18 Timing diagrams and test circuits.



DESERIALIZER PLL LOCK TIMES AND $\overline{\text{PWRDN}}$ 3-STATE DELAYS

FIGURE 19 Timing diagrams and test circuits.

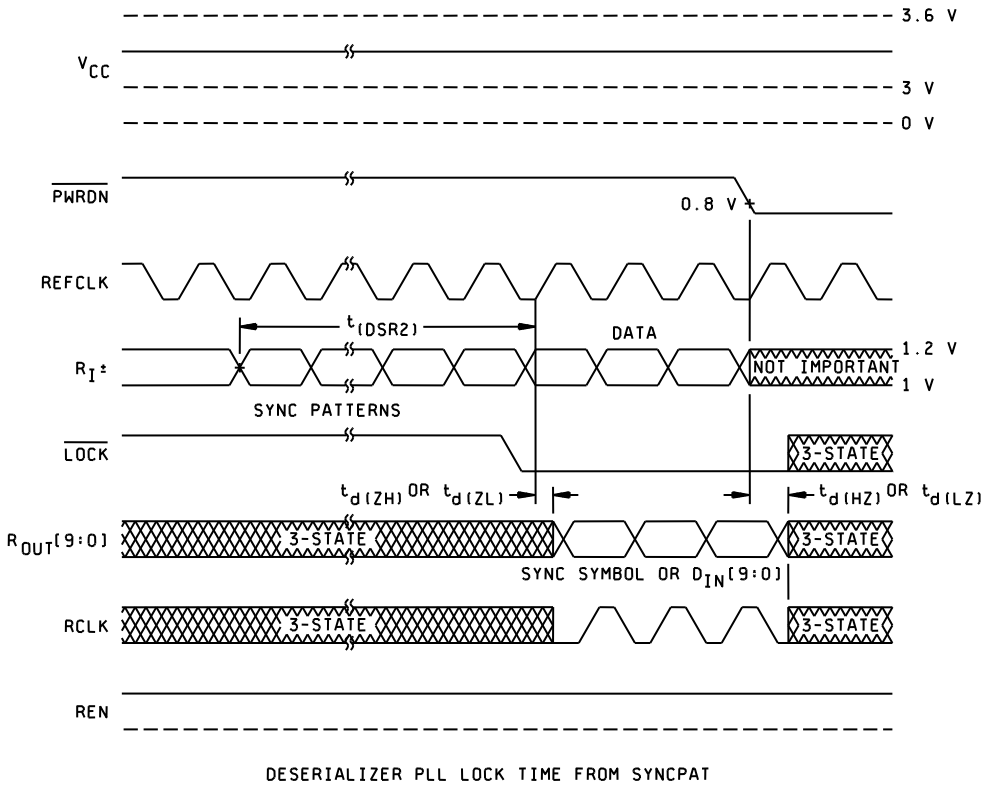
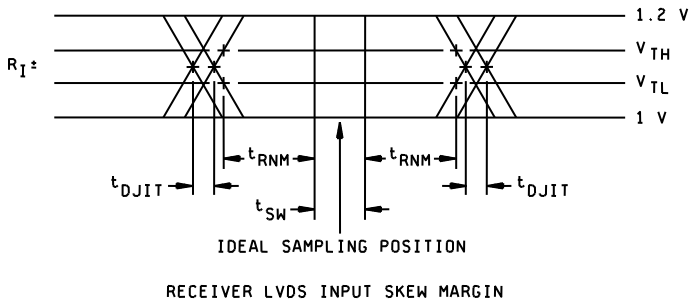


FIGURE 20 Timing diagrams and test circuits.

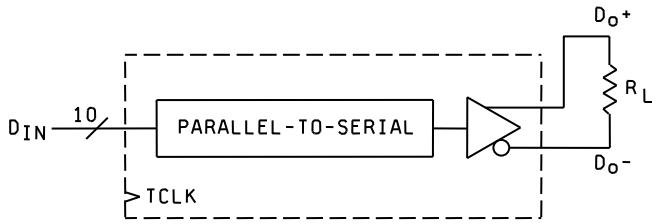


t_{SW}: Setup and hold time (Internal data sampling window)

t_{DJIT}: Serializer output bit position jitter that results from jitter on TCLK

t_{RNM}: Receiver noise margin time

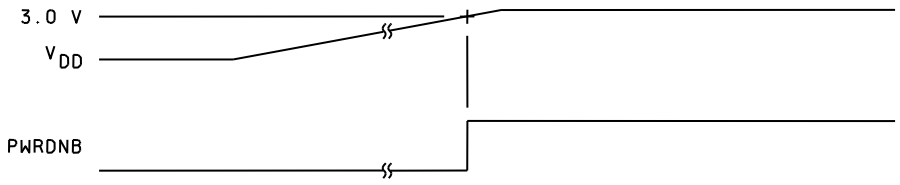
FIGURE 21 Timing diagrams and test circuits.



V_{OD} DIAGRAM

VOD = (D_O+) – (D_O-)
Differential output signal is shown as (D_O+) – (D_O-)

FIGURE 22. Timing diagrams and test circuits.



DEVICE STARTUP

FIGURE 23. Timing diagrams and test circuits.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/06677-01XE	01295	LV1023AMEP	SN65LV1023AMDBREP
V62/06677-02XE	01295	LV1224BMEP	SN65LV1224BMDBREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243