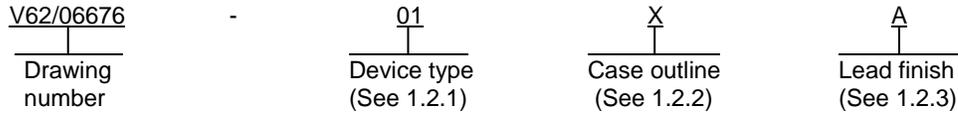


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 26-bit registered buffer with SSTL_2 inputs and LVCMOS outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74SSTV32867-EP	26-bit registered buffer with SSTL_2 inputs and LVCMOS outputs

1.2.2 Case outlines. The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	96	MO-205	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC} and V_{DDQ})	-0.5 V to 3.6 V
Input voltage range (V_I)	-0.5 V to $V_{CC} + 0.5$ V 2/
Output voltage range (V_O)	-0.5 V to $V_{DDQ} + 0.5$ V 2/ 3/
Input clamp current ($V_I < 0$) (I_{IK})	-50 mA
Output clamp current ($V_O < 0$ or $V_O > V_{DDQ}$) (I_{OK})	± 50 mA
Continuous output current ($V_O = 0$ to V_{DDQ}) (I_O)	± 50 mA
Continuous current through each V_{CC} , V_{DDQ} , or GND	± 100 mA
Package thermal impedance (θ_{JA})	40 °C/W 4/
Storage temperature range (T_{STG})	-65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	V_{DDQ} to 2.7 V
Output supply voltage range (V_{DDQ})	2.3 V to 2.7 V
Reference voltage range (V_{REF}) ($V_{REF} = V_{DDQ}/2$)	1.15 V to 1.35 V
Termination voltage range (V_{TT})	$V_{REF} - 40$ mV to $V_{REF} + 40$ mV
Input voltage range (V_{IN})	0 V to V_{CC}
Minimum AC high level input voltage (V_{IH}) (Data input)	$V_{REF} + 310$ mV
Maximum AC low level input voltage (V_{IL}) (Data input)	$V_{REF} - 310$ mV
Minimum DC high level input voltage (V_{IH}) (Data input)	$V_{REF} + 150$ mV
Maximum DC low level input voltage (V_{IL}) (Data input)	$V_{REF} - 150$ mV
Minimum high level input voltage (V_{IH}) (RESET)	1.7 V
Maximum low level input voltage (V_{IL}) (RESET)	0.7 V
Common-mode input voltage range (V_{ICR}) (CLK, \overline{CLK})	0.97 V to 1.53 V
Minimum peak-to-peak input voltage ($V_{I(PP)}$) (CLK, \overline{CLK})	360 mV
Maximum high level output current (I_{OH})	-8 mA
Maximum low level output current (I_{OL})	8 mA
Operating free-air temperature range (T_A)	-40°C to +85°C

- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3/ This value is limited to 3.6 V maximum.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ The RESET input of the device must be held at VCC or GND to ensure proper operation. The differential inputs must not be floating unless RESET is low.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IK}	I _I = -18 mA	2.3 V	25°C, -40°C to 85°C	All		-1.5	V
High level output voltage	V _{OH}	I _{OH} = -100 μA	2.3 V to 2.7 V			V _{DDQ} - 0.2		V
		I _{OH} = -8 mA	2.3 V			1.7		
Low level output voltage	V _{OL}	I _{OL} = 100 μA	2.3 V to 2.7 V				0.2	V
		I _{OL} = 8 mA	2.3 V				0.45	
Input current	I _I	All inputs. V _{IN} = V _{CC} or GND	2.7 V				±5	μA
Quiescent supply current	I _{CC}	Static standby. RESET = GND, I _O = 0 A	2.7 V				40	μA
		Static operating. RESET = V _{CC} , V _{IN} = V _{IH(AC)} or V _{IL(AC)} , I _O = 0 A					95	mA
Dynamic operating quiescent supply current, clock only	I _{CCD}	RESET = V _{CC} , V _{IN} = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching, 50% duty cycle, I _O = 0 A	2.5 V		44	μA/MHz		
Dynamic operating quiescent supply current, per each data input		RESET = V _{CC} , V _{IN} = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching, 50% duty cycle, One data input switching At one-half clock frequency, 50% duty cycle, I _O = 0 A			5	μA/clock MHz/ D input		
Input capacitance 3/	C _i	Data inputs. V _I = V _{REF} ± 310 mV	2.5 V	25°C		3.5 2/	pF	
		CLK, CLK. V _{ICR} = 1.25 V, V _{I(PP)} = 360 mV				4.5 2/		
		RESET. V _{IN} = V _{CC} or GND				5 2/		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Clock frequency	f _{clock}		2.3 V to 2.7 V	25°C, -40°C to 85°C	All		200	MHz
Pulse duration	t _w	CLK, CLK high or low C _L = 30 pF, See figure 5.				2.5		ns
Differential inputs active time <u>4/</u>	t _{act}	See figure 5.				22		ns
Differential inputs inactive time <u>5/</u>	t _{inact}	See figure 5.				22		ns
Setup time	t _{su}	Fast slew rate. <u>6/ 7/</u> Data before CLK ↑, CLK ↓ See figure 5.				1.0		ns
		Slow slew rate. <u>7/ 8/</u> Data before CLK ↑, CLK ↓ See figure 5.				1.5		
Hold time	t _h	Fast slew rate. <u>6/ 7/</u> Data after CLK ↑, CLK ↓ See figure 5.				1.0		ns
		Slow slew rate. <u>7/ 8/</u> Data after CLK ↑, CLK ↓ See figure 5.				1.5		
Maximum frequency	f _{max}	V _{REF} = V _{DDQ} /2, C _L = 30 pF, See figure 5.				200		MHz
Propagation delay time, CLK and CLK to Q	t _{pd}	V _{REF} = V _{DDQ} /2, C _L = 30 pF, See figure 5.		5.5	ns			
Propagation delay time, high to low, RESET to Q	t _{PHL}	V _{REF} = V _{DDQ} /2, C _L = 30 pF, See figure 5.		5.2	ns			

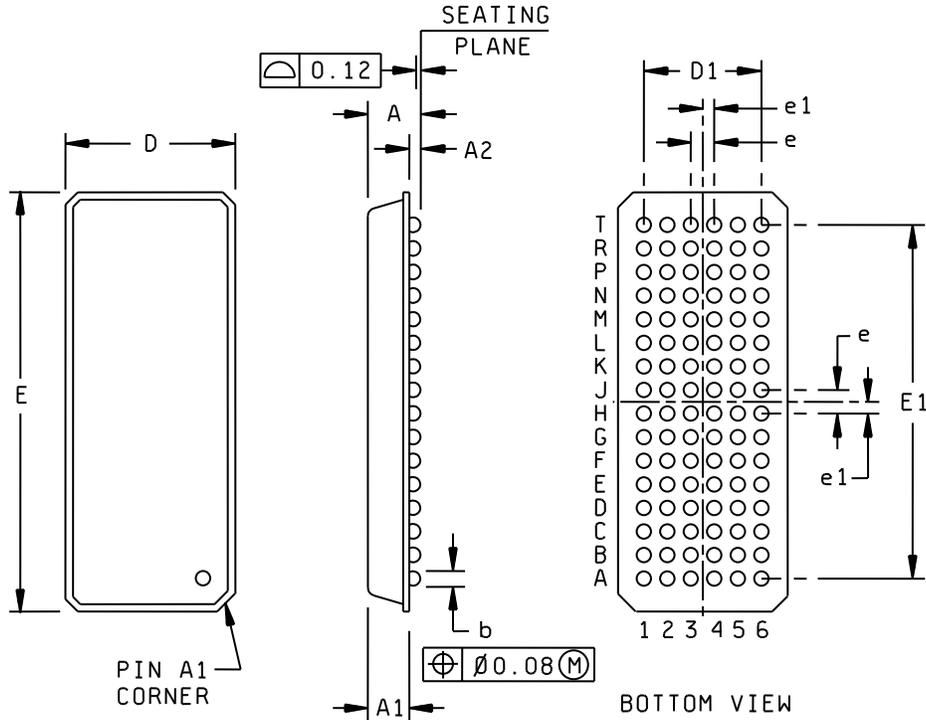
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.40	---	0.055	D1	4.00 NOM		0.157 NOM	
A1	0.85	0.95	0.033	0.037	E	13.40	13.60	0.528	0.535
A2	0.35	0.45	0.014	0.018	E1	12.00 NOM		0.472 NOM	
b	0.45	0.55	0.018	0.022	e	0.80 NOM		0.031 NOM	
D	5.40	5.60	0.213	0.220	e1	0.40 NOM		0.016 NOM	

NOTES:

1. All linear dimensions are in millimeters (inches). Inches equivalents are shown for general reference only.
2. This case outline is subject to change without notice.
3. Falls within JEDEC MO-205 variation CC.

FIGURE 1. Case outline.

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Inputs				Output
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q ₀
L	X or floating	X or floating	X or floating	L

H = High voltage level
 L = Low voltage level
 X = Immaterial
 ↑ = Rising edge of clock
 ↓ = Falling edge of clock

FIGURE 2. Function table.

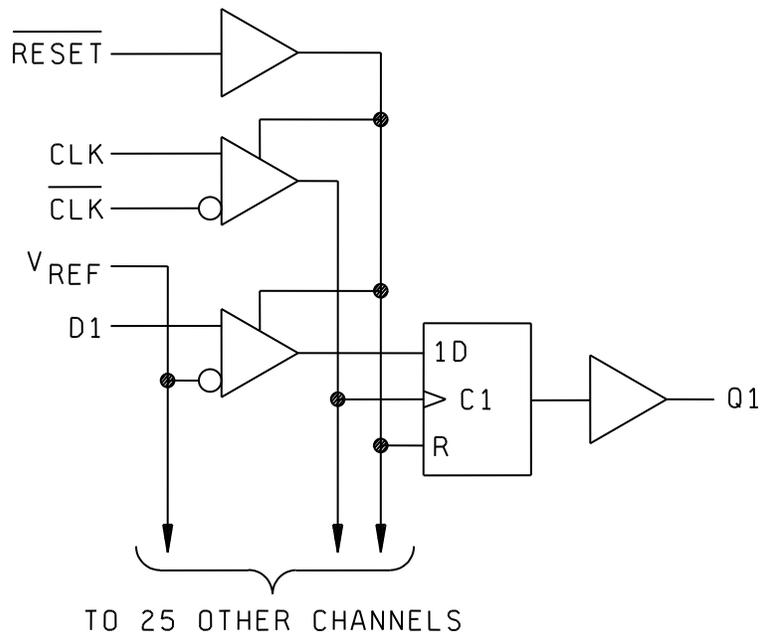
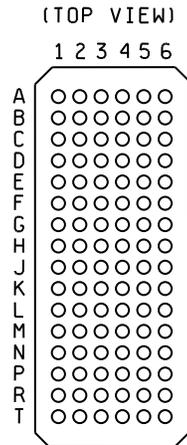


FIGURE 3. Logic diagram.

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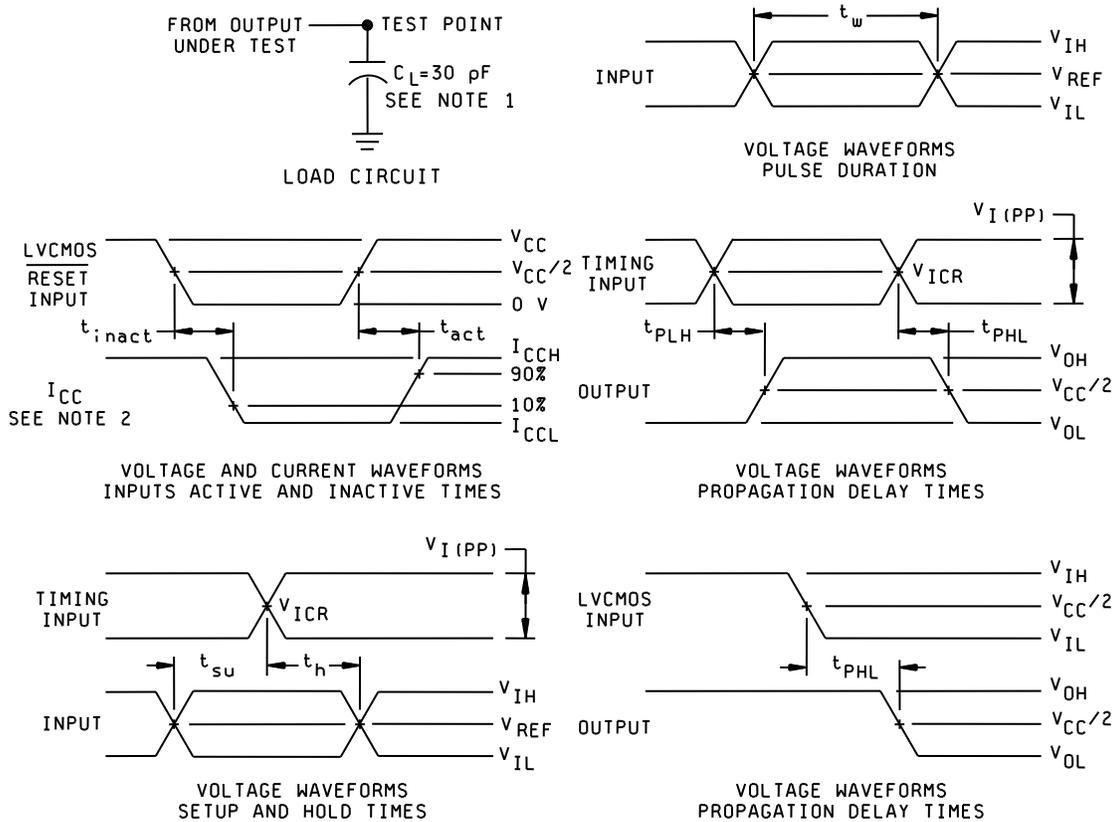


	1	2	3	4	5	6
A	D1	V _{CC}	GND	V _{DDQ}	Q1	Q2
B	D3	D2	V _{REF}	GND	Q3	Q4
C	D5	D4	NC	GND	Q5	Q6
D	D7	D6	GND	V _{DDQ}	Q7	Q8
E	D9	D8	V _{CC}	GND	Q9	V _{DDQ}
F	D11	D10	GND	V _{DDQ}	Q10	GND
G	D13	D12	V _{CC}	V _{DDQ}	Q12	Q11
H	D15	D14	GND	GND	GND	Q13
J	CLK	NC	GND	GND	GND	Q14
K	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	V _{CC}	V _{DDQ}	Q15	Q16
L	D16	D17	GND	V _{DDQ}	Q17	GND
M	D18	D19	V _{CC}	GND	Q18	V _{DDQ}
N	D20	D21	GND	V _{DDQ}	Q20	Q19
P	D22	D23	NC	GND	Q22	Q21
R	D24	D25	NC	GND	Q24	Q23
T	D26	V _{CC}	GND	V _{DDQ}	Q26	Q25

NC = No connection

FIGURE 4. Terminal connections.

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NOTES:

1. $C_L = 30 \text{ pF}$, and includes probe and jig capacitance.
2. I_{CC} tested with clock and data inputs held at V_{CC} or GND , and $I_O = 0 \text{ mA}$.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise noted).
4. The outputs are measured one at a time with one input transition per measurement.
5. $V_{REF} = V_{DDQ}/2$
6. $V_{IH} = V_{REF} + 310 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
7. $V_{IL} = V_{REF} - 310 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = GND$ for LVC MOS input.
8. t_{PLH} and t_{PHL} are the same as t_{pd} .

FIGURE 5. Test circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06676-01XE	01295	CSSTV32867SGKEREP	S867EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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