REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	19-07-03	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A					
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PMIC N/A	PREPARED BY RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 07-08-09	CHECKED BY RAJESH PITHADIA	TITLE
	APPROVED BY ROBERT M. HEBER	MICROCIRCUIT, LINEAR, LOW NOISE, HIGH SPEED, PRECISION OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE A / CODE IDENT. NO. 16236	DWG NO. **V62/06674**
	REV A	PAGE 1 OF 12

AMSC N/A

5962-V044-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low noise, high speed, precision operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06674	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLE2027-EP	Low noise, high speed, precision operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Positive supply voltage ($+V_{CC}$)	+19 V maximum 2/
Negative supply voltage ($-V_{CC}$)	-19 V maximum 2/
Differential input voltage (VID)	±1.2 V maximum 3/
Input voltage range (V_I) (any input)	$\pm V_{CC}$ maximum
Input current (I_{IN}) (each input)	±1 mA maximum
Output current (I_{OUT})	±50 mA maximum
Total current into $+V_{CC}$ terminal	50 mA maximum
Total current out of $-V_{CC}$ terminal	50 mA maximum
Duration of short circuit current at (or below) +25°C	Unlimited 4/
Continuous total power dissipation (P_D)	See dissipation rating table
Storage temperature range	-65°C to +150°C 5/
Lead temperature, soldering 1.6 mm (1/16 inch) from case for 10 seconds:	+260°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction to ambient (θ_{JC})	38.3°C/W
Thermal resistance, junction to ambient (θ_{JA})	176°C/W

1.4 Recommended operating conditions. 6/

Supply voltage range ($\pm V_{CC}$)	±4 V dc minimum, ±19 V dc maximum
Common-mode input voltage (V_{IC}) (T_A = +25°C)	-11 V dc minimum, +11 V dc maximum
Common-mode input voltage (V_{IC}) (T_A = -55°C to +125°C)	-10.3 V dc minimum, +10.3 V dc maximum
Ambient operating free-air temperature (T_A)	-55°C to +125°C

1.5 Dissipation rating table.

Case outline	$T_A \leq$ 25°C power rating	Derating factor above T_A = +25°C	T_A = +70°C power rating	T_A = +105°C power rating	T_A = +125°C power rating
X	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential voltages, are with respect to the midpoint between $+V_{CC}$ and $-V_{CC}$.

3/ Differential voltages are at the +INPUT with respect to the -INPUT. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.

4/ The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

5/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer for additional information on enhanced product packaging.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Test circuit. The test circuits shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $\pm V_{CC} = \pm 15$ V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	01		100	µV
			-55°C to +125°C			200	
Temperature coefficient of input offset voltage	αV_{IO}	$V_{IC} = 0$, $R_S = 50\ \Omega$	-55°C to +125°C	01	0.4 typical		µV/°C
Input offset voltage 2/ long-term drift		$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	01	0.006 typical		µV/mo
Input offset current	I_{IO}	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	01		90	nA
			-55°C to +125°C			150	
Input bias current	I_{IB}	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	01		90	nA
			-55°C to +125°C			150	
Common mode input voltage range	V_{ICR}	$R_S = 50\ \Omega$	25°C	01	-11 to 11		V
			-55°C to +125°C		-10.3 to 10.3		
Maximum positive peak output voltage swing	$+V_{OM}$	$R_L = 600\ \Omega$	25°C	01	10.5		V
			-55°C to +125°C		10		
		$R_L = 2$ kΩ	25°C		12		
			-55°C to +125°C		11		
Maximum negative peak output voltage swing	$-V_{OM}$	$R_L = 600\ \Omega$	25°C	01	-10.5		V
			-55°C to +125°C		-10		
		$R_L = 2$ kΩ	25°C		-12		
			-55°C to +125°C		-11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $\pm V_{CC} = \pm 15$ V unless otherwise specified	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Large signal differential voltage amplification	A_{VD}	$V_O = \pm 11$ V, $R_L = 2$ kΩ	25°C	01	5		V/μV
		$V_O = \pm 10$ V, $R_L = 2$ kΩ	-55°C to +125°C		2.5		
		$V_O = \pm 10$ V, $R_L = 1$ kΩ	25°C		3.5		
			-55°C to +125°C		1.8		
		$V_O = \pm 10$ V, $R_L = 600$ Ω	25°C		2		
Input capacitance	C_I		25°C	01	8 typical		pF
Open loop output impedance	z_O	$I_O = 0$	25°C	01	50 typical		Ω
Common mode rejection ratio	CMRR	$V_{IC} = V_{ICR}$min, $R_S = 50$ Ω	25°C	01	100		dB
			-55°C to +125°C		96		
Supply voltage rejection ratio ($\Delta \pm V_{CC} / \Delta V_{IO}$)	k_{SVR}	$\pm V_{CC} = \pm 4$ V to ± 18 V, $R_S = 50$ Ω	25°C	01	94		dB
			-55°C to +125°C		90		
Supply current	I_{CC}	$V_O = 0$, no load	25°C	01		5.3	mA
			-55°C to +125°C			5.6	
Slew rate at unity gain	SR	$R_L = 2$ kΩ, $C_L = 100$ pF, see figure 3	25°C	01	1.7		V/μs
			-55°C to +125°C		1		
Equivalent input noise voltage	V_n	$R_S = 20$ Ω, f = 10 Hz, see figure 3	25°C	01	3.3 typical		nV / $\sqrt{Hz}$
		$R_S = 20$ Ω, f = 1 kHz, figure 3			2.5 typical		
Peak to peak equivalent input noise voltage	$V_{N(PP)}$	f = 0.1 Hz to 10 Hz	25°C	01	50 typical		nV
Equivalent input noise current	I_n	f = 10 Hz	25°C	01	1.5 typical		pA / $\sqrt{Hz}$
		f = 1 kHz			0.4 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $\pm V_{CC} = \pm 15$ V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Total harmonic distortion	THD	$V_O = 10$ V, $A_{VD} = 1$ 3/	25°C	01	<0.002% typical		
Unity gain bandwidth	B_1	$R_L = 2$ kΩ, $C_L = 100$ pF, see figure 3	25°C	01	13 typical		MHz
Maximum output swing bandwidth	B_{OM}	$R_L = 2$ kΩ	25°C	01	30 typical		kHz
Phase margin at unity gain	φ_m	$R_L = 2$ kΩ, $C_L = 100$ pF, see figure 3	25°C	01	55° typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

3/ Measured distortion of the source used in the analysis was 0.002 %.

Case X

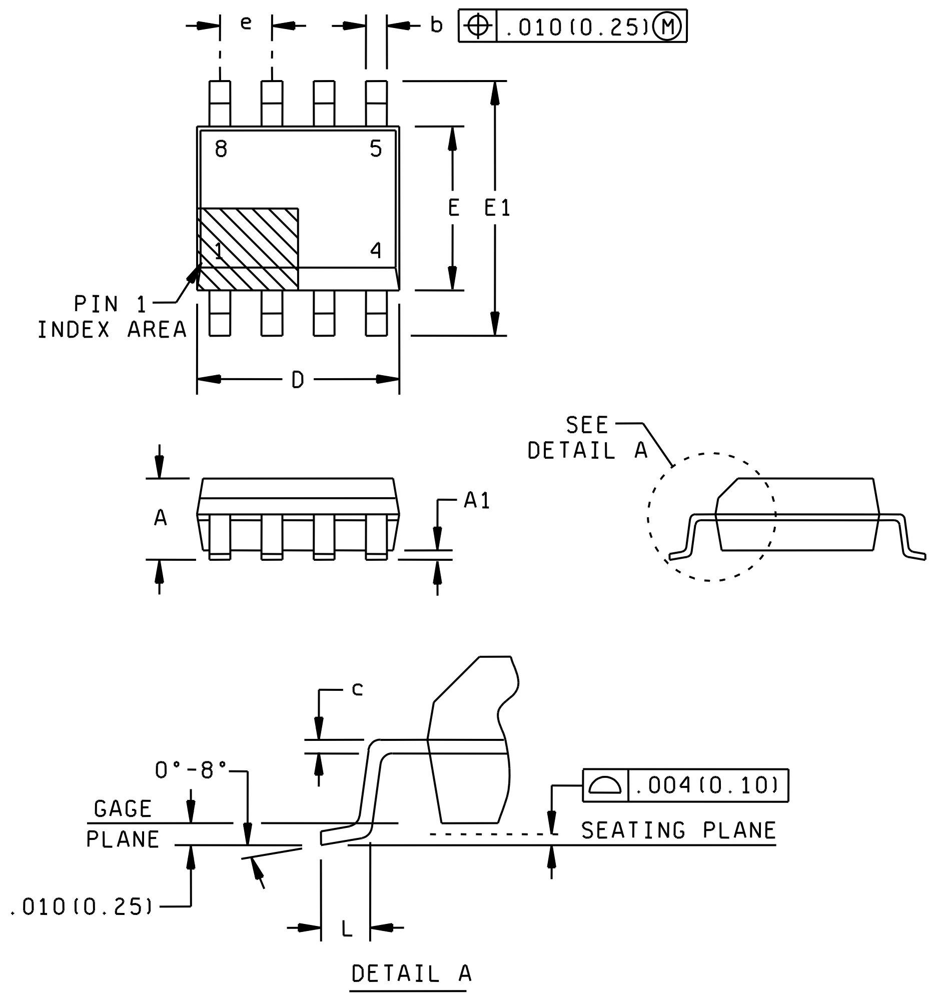


FIGURE 1. Case outline.

Case X – continued.

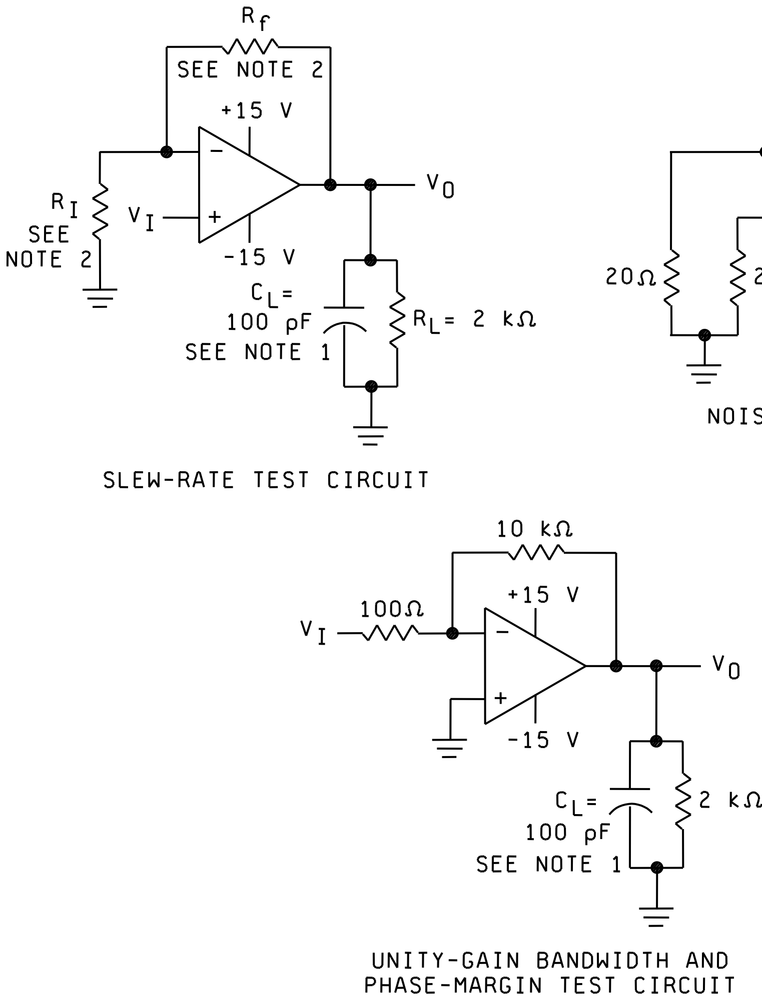
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension E, body Length does not include mold flash, protrusions or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) each side.
3. For dimension D, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OFFSET N1
2	-INPUT
3	+INPUT
4	$-V_{CC}$
5	NC
6	OUTPUT
7	$+V_{CC}$
8	OFFSET N2

FIGURE 2. Terminal connections.



NOTES:

1. C_L includes fixture capacitance.
2. The values of R_f and R_I are not specified because the circuit is connected in a non-inverting configuration with the specified load values.

FIGURE 3. Test circuits.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity 2/	V_{IO} maximum at 25°C	Vendor part number
V62/06674-01XE	01295	Tape and Reel, 2500	100 μV	TLE2027MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's datasheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243