REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-06-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A							
	PAGE	1	2	3	4	5	6	7	8	9	10							

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-10-17	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, BIPOLAR CMOS, OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06672**
	REV **A**	**PAGE** 1 **OF** 10

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer/driver with open-collector outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06672	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74BCT760-EP	Octal buffer/driver with open-collector outputs

1.2.2 Case outlines. The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7 V
Input voltage range (V_I) ..... -0.5 V to 7 V 2/
Input current range (I_I) ..... -30 mA to 5 mA
Voltage range applied to any output
in the disabled or power-off state (V_O) ..... -0.5 V to 5.5 V
Voltage range applied to any output
in the high state (V_O) ..... -0.5 V to V_{CC}
Current into any output in the low state (I_O) ..... 96 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C 3/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.5 V to 5.5 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Maximum high level output voltage (V_{OH}) ..... 5.5 V
Maximum input clamp current (I_{IK}) ..... -18 mA
Maximum low level output current (I_{OL}) ..... 48 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

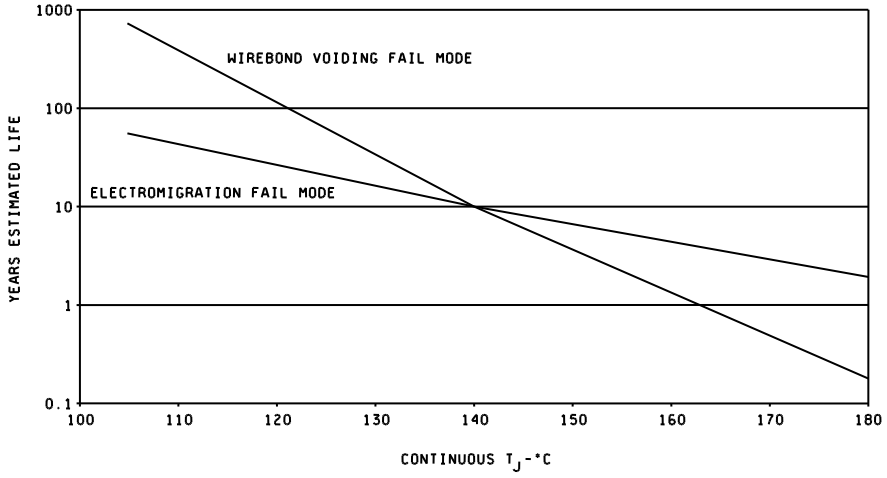


FIGURE 1. Operating life derating chart.

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The negative input voltage rating may be exceeded if the input clamp-current rating is observed.
3/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See figure 1.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 2.

3.5.2 Function table. The function table shall be as shown in figure 3.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 5.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

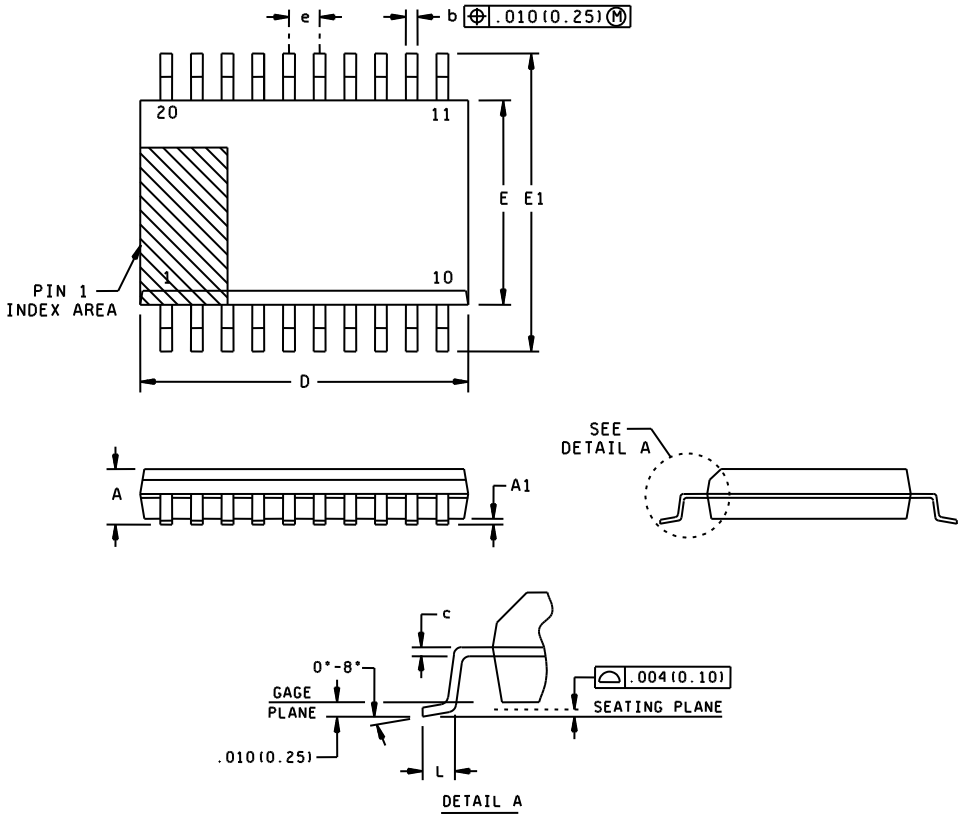
Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	4.5 V	25°C, -55°C to 125°C		-1.2	V
Low level outpu voltage	V_{OL}	I_{OL} = 48 mA	4.5 V			0.55	V
Input current	I_I	V_I = 7 V	5.5 V			0.1	mA
High level input current	I_{IH}	V_I = 2.7 V	5.5 V			20	µA
Low level input current	I_{IL}	V_I = 0.5 V	5.5 V			-1	mA
High level output voltage	I_{OH}	V_{OH} = 5.5 V	4.5 V			0.1	mA
Quiescent supply current	I_{CC}	(Outputs open) Outputs high.	5.5 V			33	mA
		(Outputs open) Outputs low.				76	
		(Outputs open) $\overline{OE}$ disabled.				10	
Input capacitance	C_i	V_I = 2.5 V or 0.5 V	5 V	25°C	6 TYP		pF
Output capacitance	C_O	V_O = 2.5 V or 0.5 V	5 V		10 TYP		pF
Propagation delay time, A to Y	t_{PLH}		5 V	25°C	6.3	9.5	ns
			4.5 V to 5.5 V	-55°C to 125°C	6.3	11.1	
	t_{PHL}		5 V	25°C	2.1	6.5	
			4.5 V to 5.5 V	-55°C to 125°C	2.1	7.7	
Propagation delay time, $\overline{OE}$ to Y	t_{PLH}		5 V	25°C	8.6	15.2	
			4.5 V to 5.5 V	-55°C to 125°C	8.6	18.7	
	t_{PHL}		5 V	25°C	3.2	8.9	
			4.5 V to 5.5 V	-55°C to 125°C	3.2	10.4	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.104	---	2.65	E	0.291	0.299	7.40	7.60
A1	0.004	0.012	0.10	0.30	E1	0.393	0.419	9.97	10.63
b	0.012	0.020	0.31	0.51	e	0.050 BSC		1.27 BSC	
c	0.008	0.013	0.20	0.33	L	0.016	0.050	0.40	1.27
D	0.496	0.512	12.60	13.00					

NOTES:
1. All linear dimensions are in inches (millimeters). Millimeters equivalents are shown for general reference only.
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 in (0.15 millimeters).
4. Fall within JEDEC MS-013 variation AC.

FIGURE 2. Case outline.

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	H

H = High voltage level
L = Low voltage level
X = Immaterial

FIGURE 3. Function table.

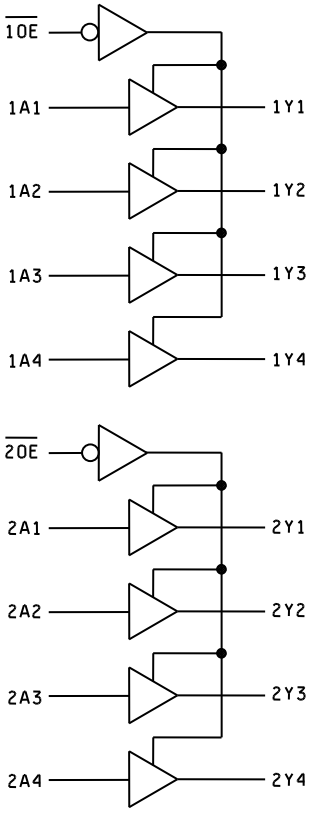
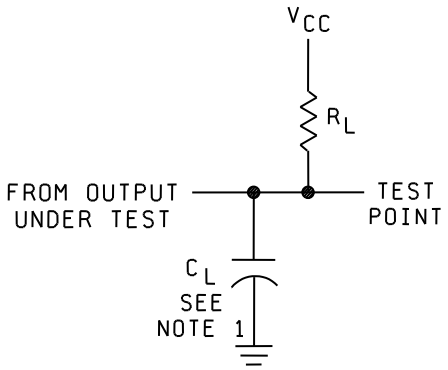
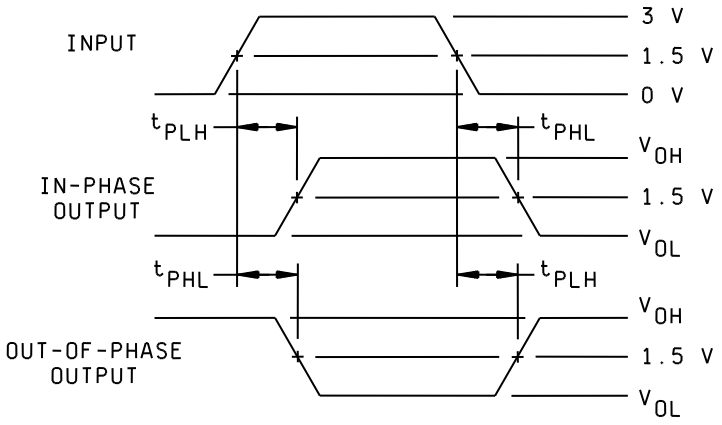


FIGURE 4. Logic diagram.

Device type:	All
Case outline:	X
Terminal number	Terminal symbol
1	$1\overline{OE}$
2	1A1
3	2Y4
4	1A2
5	2Y3
6	1A3
7	2Y2
8	1A4
9	2Y1
10	GND
11	2A1
12	1Y4
13	2A2
14	1Y3
15	2A3
16	1Y2
17	2A4
18	1Y1
19	$2\overline{OE}$
20	V_{CC}

FIGURE 5. Terminal connections.





NOTES:
1. C_L = 50 pF, and includes probe and jig capacitance.
2. R_L = 500 Ω.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 6. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06672-01XE	01295	SN74BCT760MDWREP	BCT760MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493