REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under Table I, make changes to Linearity error and Zero code error tests limits for device types 03 and 04 only. Add one note under figure 1 for both case outlines X and Y. Update document paragraphs to current requirements. - ro	14-10-20	C. SAFFLE
B	Delete Transport media quantity column from paragraph 1.2.1. Under Linearity error test, for device type 03, 04, delete ±0.4 LSB and replace with ±4.0 LSB as specified under Table I. Update min "c" dimension limit for both cases X and Y as specified under Figure 1. Delete last sentence of Case X note 3 as specified under Figure 1. Update document paragraphs to current requirements. - ro	20-07-23	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B																			
PAGE	18	19																			

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-09-14	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 16-BIT, LOW POWER, VOLTAGE OUTPUT, DIGITAL-TO-ANALOG CONVERTERS, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06671**
	REV B	**PAGE** 1 **OF** 19

AMSC N/A

5962-V041-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance16 bit, low power, voltage output, digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06671	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DAC8830-REP	16 bit, low power, voltage output, digital to analog converter
02	DAC8830-EP	16 bit, low power, voltage output, digital to analog converter
03	DAC8831-REP	16 bit, low power, voltage output, digital to analog converter
04	DAC8831-EP	16 bit, low power, voltage output, digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline
Y	14	MS-012-AB	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND ..... -0.3 V to 7 V
Digital input voltage to DGND ..... -0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND ..... -0.3 V to V_{DD} + 0.3 V
AGND, AGNDF, AGNDS to DGND ..... -0.3 V to +0.3 V
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Junction temperature range (T_J) ..... +150°C
Power dissipation (P_D) :
  X package ..... 167.2 mW
  Y package ..... 239.2 mW
Thermal resistance, junction to ambient (θ_{JA}):
  X package ..... 149.5°C/W
  Y package ..... 104.5°C/W
Lead temperature, soldering :
  Vapor phase (60 seconds) ..... 215°C
  Infrared (15 seconds) ..... 220°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance							
Resolution			-55°C to +125°C	All	16		bits
Linearity error			25°C	All		±1	LSB
			-55°C to +125°C	01, 02		±1.5	
				03, 04		±4.0	
Differential linearity error		All grades	-55°C to +125°C	All		±1	LSB
Gain error			25°C	All		±5	LSB
			-55°C to +125°C			±7	
Gain drift			-55°C to +125°C	All	±0.1 typical		ppm/°C
Zero code error			25°C	All		±1	LSB
			-55°C to +125°C	01, 02		±2	
				03, 04		±3	
Zero code drift			-55°C to +125°C	All	±0.05 typical		ppm/°C
Output characteristics							
Voltage output 3/		Unipolar operation	-55°C to +125°C	All	0	V_{REF}	V
		Bipolar operation		03, 04	$-V_{REF}$	V_{REF}	
Output impedance			-55°C to +125°C	All	6.25 typical		kΩ
Settling time	t_S	To 1/2 LSB of FS, C_L = 10 pF	-55°C to +125°C	All	1 typical		µs
Slew rate 4/	SR	C_L = 10 pF	-55°C to +125°C	All	25 typical		V/µs
Digital to analog glitch		1 LSB change around major carry	-55°C to +125°C	All	8 typical		nV-s
Digital feedthrough 5/			-55°C to +125°C	All	0.2 typical		nV-s
Output noise			25°C	01, 02	10 typical		nV / $\sqrt{Hz}$
				03, 04	18 typical		
Power supply rejection	PSR	V_{DD} varies ±10%	-55°C to +125°C	All		±1	LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics - continued.							
Bipolar resistor matching		R_{FB} / R_{INV}	-55°C to +125°C	03, 04	1 typical		Ω / Ω
		Ratio error				±0.01	%
Bipolar zero error			25°C	03, 04		±5	LSB
			-55°C to +125°C			±7	
Bipolar zero drift			-55°C to +125°C	03, 04	±0.2 typical		ppm/°C
Reference input							
Reference input 6/ voltage range			-55°C to +125°C	All	1.25	V_{DD}	V
Reference input 7/ impedance		Unipolar operation	-55°C to +125°C	All	9		kΩ
		Bipolar operation		03, 04	7.5		
Reference -3 dB bandwidth	BW	Code = FFFFh	-55°C to +125°C	All	1.3 typical		MHz
Reference feedthrough		Code = 0000h, V_{REF} = 1 V_{PP} at 100 kHz	-55°C to +125°C	All	1 typical		mV
Signal to noise ratio	SNR		-55°C to +125°C	All	92 typical		dB
Reference input capacitance		Code = 0000h	-55°C to +125°C	All	75 typical		pF
		Code = FFFFh			120 typical		
Digital inputs							
Input low voltage	V_{IL}	V_{DD} = 2.7 V	-55°C to +125°C	All		0.6	V
		V_{DD} = 5 V				0.8	
Input high voltage	V_{IH}	V_{DD} = 2.7 V	-55°C to +125°C	All	2.1		V
		V_{DD} = 5 V			2.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital inputs - continued.							
Input current	I_{IN}		-55°C to +125°C	All		±1	µA
Input capacitance	C_{IN}		-55°C to +125°C	All		10	pF
Hysteresis voltage			-55°C to +125°C	All	0.4 typical		V
Power supply							
Supply voltage	V_{DD}		-55°C to +125°C	All	2.7	5.5	V
Supply current	I_{DD}	V_{DD} = 3 V	-55°C to +125°C	All		20	µA
		V_{DD} = 5 V				20	
Power		V_{DD} = 3 V	-55°C to +125°C	All		60	µW
		V_{DD} = 5 V				100	
Temperature range							
Specified performance			-55°C to +125°C	All	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 3 V or V_{DD} = 5 V, V_{REF} = 2.5 V.

3/ The device type 01 output is unipolar (0 V to V_{REF}). The device type 02 output is bipolar (±V_{REF}) when it connects to an external buffer (see the bipolar output operation section under manufacturer's datasheet).

4/ Slew rate is measure from 10% to 90% of transition when the output changes from 0 to full scale.

5/ Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change, $\overline{CS}$ is held high, while SCLK and DIN signals are toggled.

6/ Specified by design, V_{ref} production tested only at 2.5 V.

7/ Reference input resistance is code dependent, minimum at 8555h.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 8/ 9/ V_{DD} = 5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristic		See figure 4.					
SCLK period	t_{sck}		-55°C to +125°C	All	20		ns
SCLK high or low time	t_{wsck}		-55°C to +125°C	All	10		ns
Delay from SCLK high to $\overline{CS}$ low	t_{Delay}		-55°C to +125°C	All	18		ns
$\overline{CS}$ enable lead time	t_{Lead}		-55°C to +125°C	All	12		ns
$\overline{CS}$ enable lag time	t_{Lag}		-55°C to +125°C	All	15		ns
Delay from $\overline{CS}$ high to SCLK high	t_{DSCLK}		-55°C to +125°C	All	15		ns
$\overline{CS}$ high between active period	t_{td}		-55°C to +125°C	All	30		ns
Data setup time (input)	t_{su}		-55°C to +125°C	All	10		ns
Data hold time (input)	t_{ho}		-55°C to +125°C	All	0		ns
$\overline{LDAC}$ width	t_{WLDAC}		-55°C to +125°C	All	30		ns
Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	t_{DLDAC}		-55°C to +125°C	All	30		ns
V_{DD} high to $\overline{CS}$ low (power up delay)			-55°C to +125°C	All	10		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 8/ 9/ V_{DD} = 3 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristic		See figure 4.					
SCLK period	t_{sck}		-55°C to +125°C	All	20		ns
SCLK high or low time	t_{wsck}		-55°C to +125°C	All	10		ns
Delay from SCLK high to $\overline{CS}$ low	t_{Delay}		-55°C to +125°C	All	18		ns
$\overline{CS}$ enable lead time	t_{Lead}		-55°C to +125°C	All	15		ns
$\overline{CS}$ enable lag time	t_{Lag}		-55°C to +125°C	All	15		ns
Delay from $\overline{CS}$ high to SCLK high	t_{DSCLK}		-55°C to +125°C	All	15		ns
$\overline{CS}$ high between active period	t_{td}		-55°C to +125°C	All	30		ns
Data setup time (input)	t_{su}		-55°C to +125°C	All	10		ns
Data hold time (input)	t_{ho}		-55°C to +125°C	All	0		ns
$\overline{LDAC}$ width	t_{WLDAC}		-55°C to +125°C	All	30		ns
Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	t_{DLDAC}		-55°C to +125°C	All	30		ns
V_{DD} high to $\overline{CS}$ low (power up delay)			-55°C to +125°C	All	10		µs

8/ Specified by design. Not production tested.

9/ Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

Case X

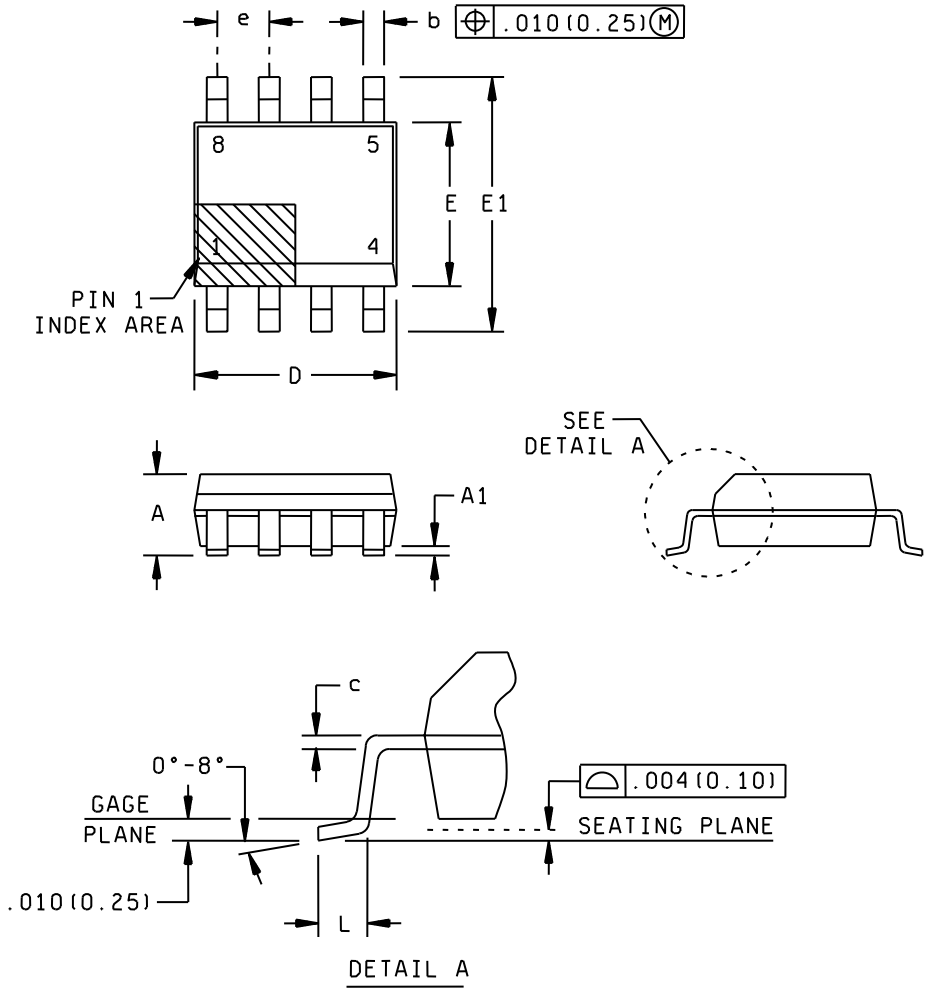

FIGURE 1. Case outlines.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
E1	.228	.244	5.80	6.20
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outlines – Continued.

Case Y

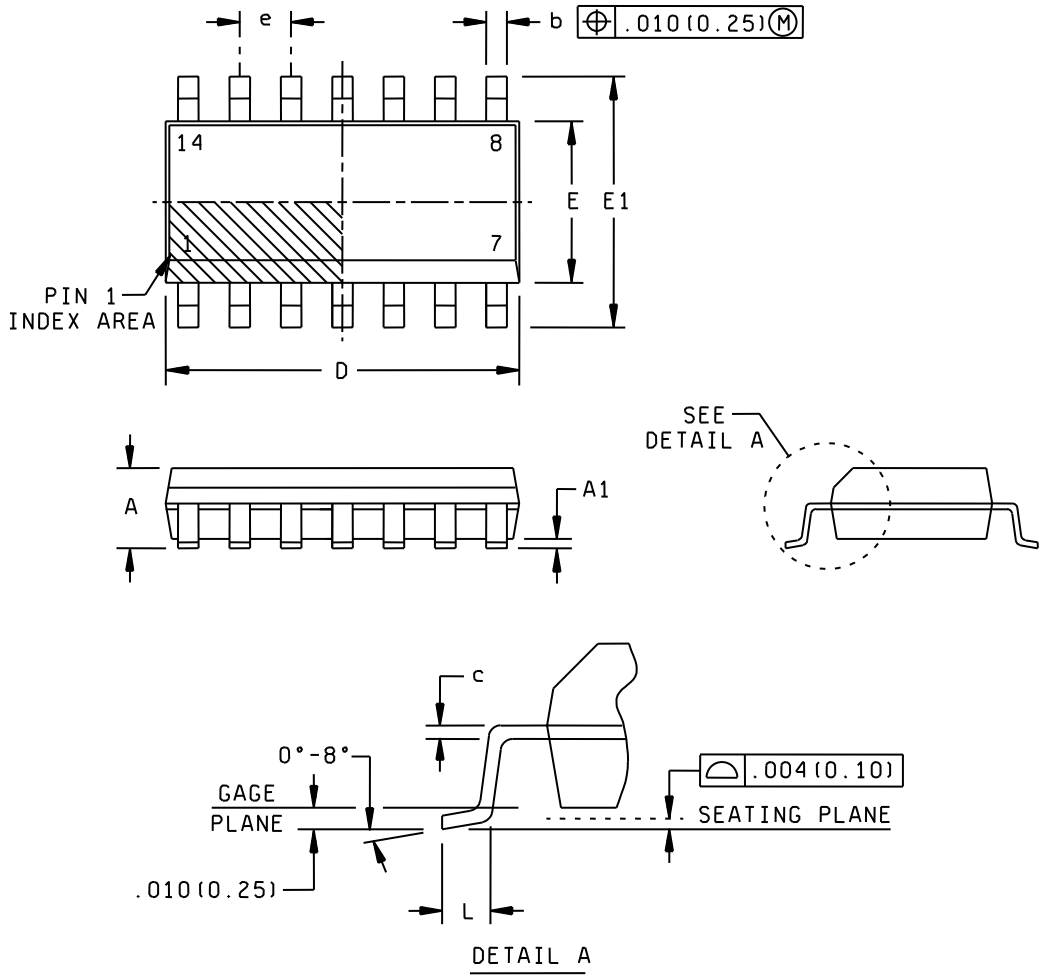

FIGURE 1. Case outlines – Continued.

Case Y - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.337	.344	8.55	8.75
e	.050 BSC		1.27 BSC	
E	.150	.157	3.80	4.00
E1	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
n	14 leads		14 leads	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MO-012-AB.

FIGURE 1. Case outlines - Continued.

Device types	01, 02	03, 04
Case outlines	X	Y
Terminal number	Terminal symbol	
1	V_{OUT}	RFB
2	AGND	V_{OUT}
3	V_{REF}	AGNDF
4	$\overline{CS}$	AGNDS
5	SCLK	V_{REF}-S
6	SDI	V_{REF}-F
7	DGND	$\overline{CS}$
8	V_{DD}	SCLK
9	---	NC
10	---	SDI
11	---	$\overline{LDAC}$
12	---	DGND
13	---	INV
14	---	V_{DD}

FIGURE 2. Terminal connections.

Device types 01, 02	
Terminal symbol	Description
V_{OUT}	Analog output of DAC.
AGND	Analog ground.
V_{REF}	Voltage reference input.
$\overline{CS}$	Chip select input (active low). Data is not clocked into SDI unless $\overline{CS}$ is low.
SCLK	Serial clock input.
SDI	Serial data input. Data is latched into input register on the rising edge of SCLK.
DGND	Digital ground.
V_{DD}	Analog power supply, 3 V to 5 V.

Device types 03, 04	
Terminal symbol	Description
RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
V_{OUT}	Analog output of DAC.
AGNDF	Analog ground (Force).
AGNDS	Analog ground (Sense).
V_{REF}-S	Voltage reference input (Sense). Connect to external voltage reference.
V_{REF}-F	Voltage reference input (Force). Connect to external voltage reference.
$\overline{CS}$	Chip select input (active low). Data is not clocked into SDI unless $\overline{CS}$ is low.
SCLK	Serial clock input.
NC	No internal connection.
SDI	Serial data input. Data is latched into input register on the rising edge of SCLK.
$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is low, the DAC latch is simultaneously updated with the content of the input register.
DGND	Digital ground.
INV	Junction point of internal scaling resistors. Connect to external operational amplifier's inverting input in bipolar mode.
V_{DD}	Analog power supply, 3 V to 5 V.

FIGURE 2. Terminal connections – Continued.

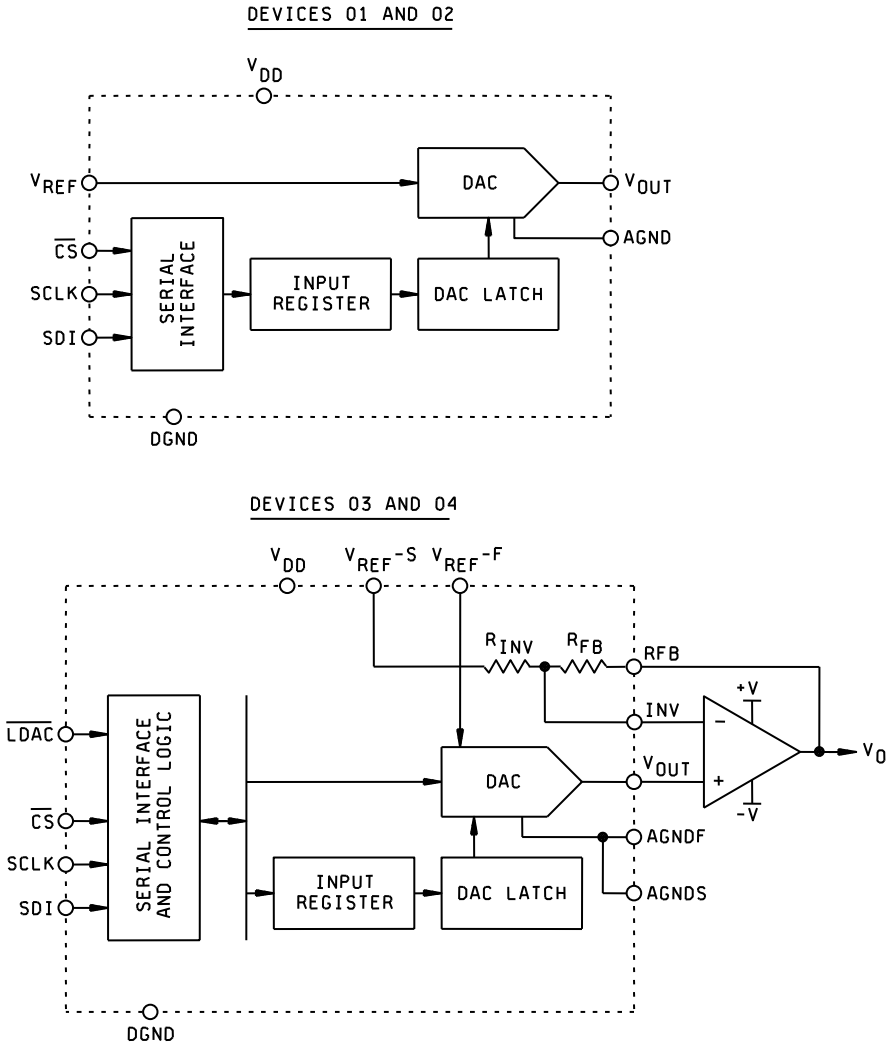

FIGURE 3. Logic diagrams.

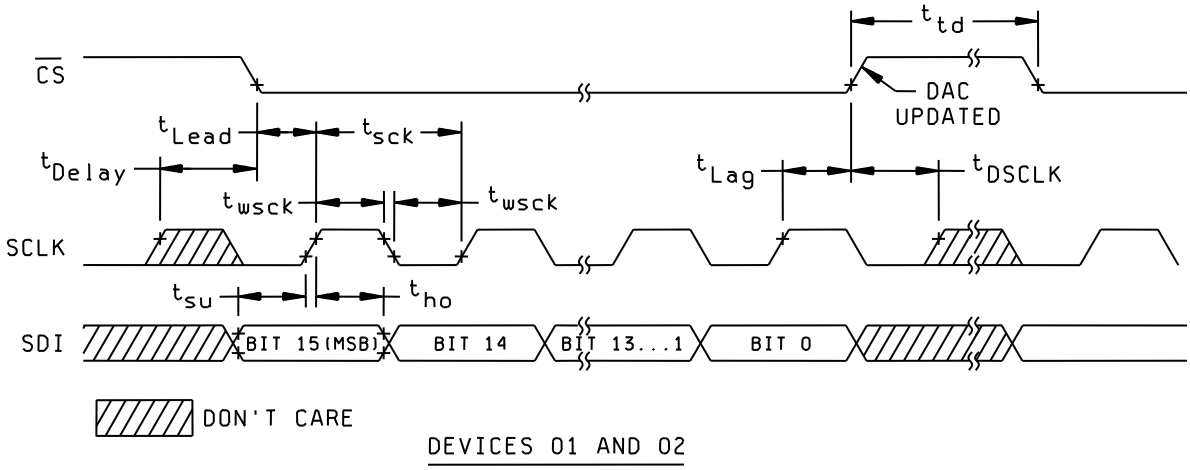

FIGURE 4. Timing waveforms.

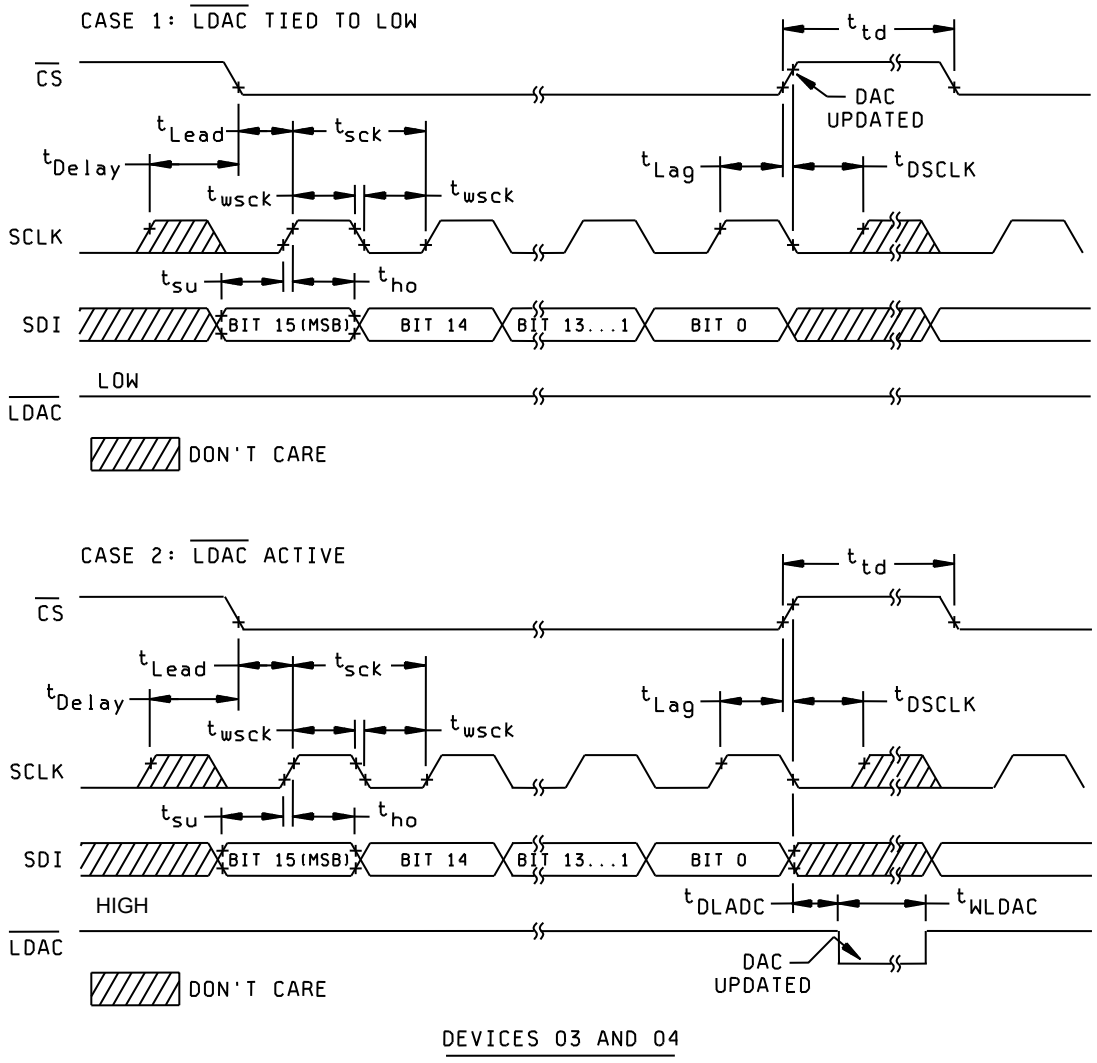

FIGURE 4. Timing waveforms – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package marking	Transport media, quantity	Vendor part number
V62/06671-01XE	01295	8830M	Tape and reel, 2500 units	DAC8830MCDREP
V62/06671-02XE	01295	8830M	Tube, 75 units	DAC8830MCDEP
V62/06671-03YE	01295	8831M	Tape and reel, 2500 units	DAC8831MCDREP
V62/06671-04YE	01295	8831M	Tube, 50 units	DAC8831MCDEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243