

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Under paragraph 1.2.1, delete 250 MSPS and replace with 210 MSPS.	06-10-10	R. MONNIN
B	Update document paragraphs to current requirements. - ro	14-08-12	C. SAFFLE
C	Update document paragraphs to current requirements. - ro	20-05-21	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD  06-08-31	CHECKED BY TOM HESS	TITLE MICROCIRCUIT, DIGITAL-LINEAR, 13-BIT, 210 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/06669</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 13-bit, 210 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06669</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADS5440-EP	13 bit, 210 MSPS, analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	80	MS-026	Plastic quad flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage :

AVDD to GND .....	6 V
DRVDD to GND .....	5 V
Analog input to GND .....	-0.3 V to AVDD + 0.3 V
Clock input to GND .....	-0.3 V to AVDD + 0.3 V
CLK to $\overline{\text{CLK}}$ .....	$\pm 2.5$ V
Digital data output to GND .....	-0.3 V to DRVDD + 0.3 V
Maximum junction temperature (T <sub>J</sub> ) .....	150°C
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to 150°C
Electrostatic discharge (ESD) human body model (HBM) .....	2.5 kV

1.4 Recommended operating conditions. 2/

Supplies:

Analog supply voltage (AVDD) .....	4.75 V to 5.25 V
Output driver supply voltage (DRVDD) .....	3 V to 3.6 V

Analog input:

Differential input range .....	2.2 V <sub>PP</sub> nominal
Input common mode voltage (V <sub>CM</sub> ) .....	2.4 V nominal

Clock input:

ADCLK input sample rate (sine wave) (1/t <sub>C</sub> ) .....	10 MSPS to 210 MSPS
Clock amplitude, differential sine wave .....	3 V <sub>PP</sub> nominal
Clock duty cycle .....	50 % nominal
Operating free-air temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

1.5 Thermal characteristics. 3/

Parameter	Test conditions	Typical limits
θ <sub>JA</sub>	Soldered slug, no airflow	21.7°C/W
θ <sub>JA</sub>	Soldered slug, 250 LPFM airflow	15.4°C/W
θ <sub>JA</sub>	Unsoldered slug, no airflow	50°C/W
θ <sub>JA</sub>	Unsoldered slug, 250 LPFM airflow	43.4°C/W
θ <sub>JC</sub>	Bottom of package (heat slug)	2.99°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 3/ Using 36 thermal vias (6 x 6 array). See application section of vendor datasheet.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +125°C	01	13 typical		Bits
Analog inputs section							
Differential input range			-55°C to +125°C	01	2.2 typical		V <sub>PP</sub>
Differential input resistance (DC)	R <sub>DI</sub>		-55°C to +125°C	01	1 typical		kΩ
Differential input capacitance	C <sub>DI</sub>		-55°C to +125°C	01	1.5 typical		pF
Analog input bandwidth			-55°C to +125°C	01	800 typical		MHz
Internal reference voltages section							
Reference voltage	V <sub>REF</sub>		-55°C to +125°C	01	2.4 typical		V
Dynamic accuracy section							
No missing codes			-55°C to +125°C	01	Assured typical		
Differential linearity error	DNL	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	-1	1	LSB
Integral linearity error	INL	f <sub>IN</sub> = 10 MHz	+25°C	01	-2.2	2.2	LSB
			-55°C to +125°C		-3.2	3.2	
Offset error			-55°C to +125°C	01	-11	11	mV
Offset temperature coefficient			-55°C to +125°C	01	0.0005 typical		mV / °C
Gain error			-55°C to +125°C	01	-5	5	%FS
Gain temperature coefficient			-55°C to +125°C	01	-0.02 typical		Δ% / °C
Power supply rejection ratio	PSRR	f <sub>IN</sub> = 100 MHz	-55°C to +125°C	01	1 typical		mV/V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power supply section							
Analog supply current	I <sub>AVDD</sub>	V <sub>IN</sub> = full scale, f <sub>IN</sub> = 100 MHz, F <sub>S</sub> = 210 MSPS	-55°C to +125°C	01		410	mA
Output buffer supply current	I <sub>DRVDD</sub>	V <sub>IN</sub> = full scale, f <sub>IN</sub> = 100 MHz, F <sub>S</sub> = 210 MSPS	-55°C to +125°C	01		100	mA
Power dissipation	P <sub>D</sub>	V <sub>IN</sub> = full scale, f <sub>IN</sub> = 100 MHz, F <sub>S</sub> = 210 MSPS	-55°C to +125°C	01		2.35	W
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	69.8 typical		dBc
		f <sub>IN</sub> = 70 MHz			69.2 typical		
		f <sub>IN</sub> = 100 MHz	25°C		67.5		
			-55°C to +125°C		66		
		f <sub>IN</sub> = 170 MHz	-55°C to +125°C		68.3 typical		
		f <sub>IN</sub> = 230 MHz			68 typical		
		f <sub>IN</sub> = 300 MHz			66.9 typical		
f <sub>IN</sub> = 400 MHz	65 typical						
Spurious free dynamic range	SFDR	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	84 typical		dBc
		f <sub>IN</sub> = 70 MHz			77 typical		
		f <sub>IN</sub> = 100 MHz	25°C		70		
			-55°C to +125°C		64.5		
		f <sub>IN</sub> = 170 MHz	-55°C to +125°C		74 typical		
		f <sub>IN</sub> = 230 MHz			74 typical		
		f <sub>IN</sub> = 300 MHz			69 typical		
f <sub>IN</sub> = 400 MHz	64 typical						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Second harmonic	HD2	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	96 typical		dBc
		f <sub>IN</sub> = 70 MHz			83 typical		
		f <sub>IN</sub> = 100 MHz			87 typical		
		f <sub>IN</sub> = 170 MHz			76 typical		
		f <sub>IN</sub> = 230 MHz			76 typical		
		f <sub>IN</sub> = 300 MHz			69 typical		
		f <sub>IN</sub> = 400 MHz			64 typical		
Third harmonic	HD3	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	84 typical		dBc
		f <sub>IN</sub> = 70 MHz			77 typical		
		f <sub>IN</sub> = 100 MHz			76 typical		
		f <sub>IN</sub> = 170 MHz			74 typical		
		f <sub>IN</sub> = 230 MHz			74 typical		
		f <sub>IN</sub> = 300 MHz			73 typical		
		f <sub>IN</sub> = 400 MHz			70 typical		
Worst harmonic / spur (other than HD2 and HD3)		f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	92 typical		dBc
		f <sub>IN</sub> = 70 MHz			92 typical		
		f <sub>IN</sub> = 100 MHz			87 typical		
		f <sub>IN</sub> = 170 MHz			87 typical		
		f <sub>IN</sub> = 230 MHz			83 typical		
		f <sub>IN</sub> = 300 MHz			83 typical		
		f <sub>IN</sub> = 400 MHz			80 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Signal-to-noise + distortion	SINAD	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	69.6 typical		dBc
		f <sub>IN</sub> = 70 MHz			68.8 typical		
		f <sub>IN</sub> = 100 MHz			68 typical		
		f <sub>IN</sub> = 170 MHz			66.8 typical		
		f <sub>IN</sub> = 230 MHz			66 typical		
		f <sub>IN</sub> = 300 MHz			64 typical		
		f <sub>IN</sub> = 400 MHz			60 typical		
Effective number of bits	ENOB	f <sub>IN</sub> = 10 MHz	-55°C to +125°C	01	11.4 typical		Bits
RMS idle channel noise		Inputs tied to common mode	-55°C to +125°C	01	0.4 typical		LSB
Digital characteristics - LVDS digital outputs							
Differential output voltage	V <sub>DO</sub>		-55°C to +125°C	01	0.247	0.452	V
Output offset voltage	V <sub>OS</sub>		-55°C to +125°C	01	1.125	1.375	V
Timing characteristics							
Aperture delay	t <sub>A</sub>		-55°C to +125°C	01	500 typical		ps
Clock scope independent aperture uncertainty (jitter)	t <sub>J</sub>		-55°C to +125°C	01	150 typical		fs RMS
Latency			-55°C to +125°C	01	4 typical		cycles

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Clock input section		See figure 4					
Clock period	tCLK		-55°C to +125°C	01	4.76 typical		ns
Clock pulse width high	tCLKH		-55°C to +125°C	01	2.38 typical		ns
Clock pulse width low	tCLKL		-55°C to +125°C	01	2.38 typical		ns
Clock to data ready (DRY) section		See figure 4					
Clock rising to data ready falling	tDR		-55°C to +125°C	01	1.1 typical		ns
Clock rising to data ready rising	tC(DR)	Clock duty cycle = 50 % <u>3/</u>	-55°C to +125°C	01	3.1	3.9	ns
Clock to DATA, over range (OVR) section <u>4/</u>		See figure 4					
Data rise time (20% to 80%)	t <sub>r</sub>		-55°C to +125°C	01	0.6 typical		ns
Data fall time (80% to 20%)	t <sub>f</sub>		-55°C to +125°C	01	0.6 typical		ns
Data valid to clock (setup time)	t <sub>su</sub> (C)		-55°C to +125°C	01	3.5 typical		ns
Clock to invalid data (hold time)	t <sub>h</sub> (C)		-55°C to +125°C	01	0.2 typical		ns
Data ready (DRY) to DATA, over range (OVR) section		See figure 4					
Data valid to DRY	t <sub>su</sub> (DR)		-55°C to +125°C	01	2.1		ns
Data ready (DRY) to invalid data	t <sub>h</sub> (DR)		-55°C to +125°C	01	0.9		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, sampling rate = 210 MSPS, 50 % clock duty cycle, AVDD = 5 V, DRVDD = 3.3 V, -1 dBFS differential input, and 3 VPP differential clock.

3/ t<sub>C\_DR</sub> = tDR + tCLKH for clock duty cycles other than 50%.

4/ Data is updated with clock falling edge or data ready (DRY) rising edge.

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Case X

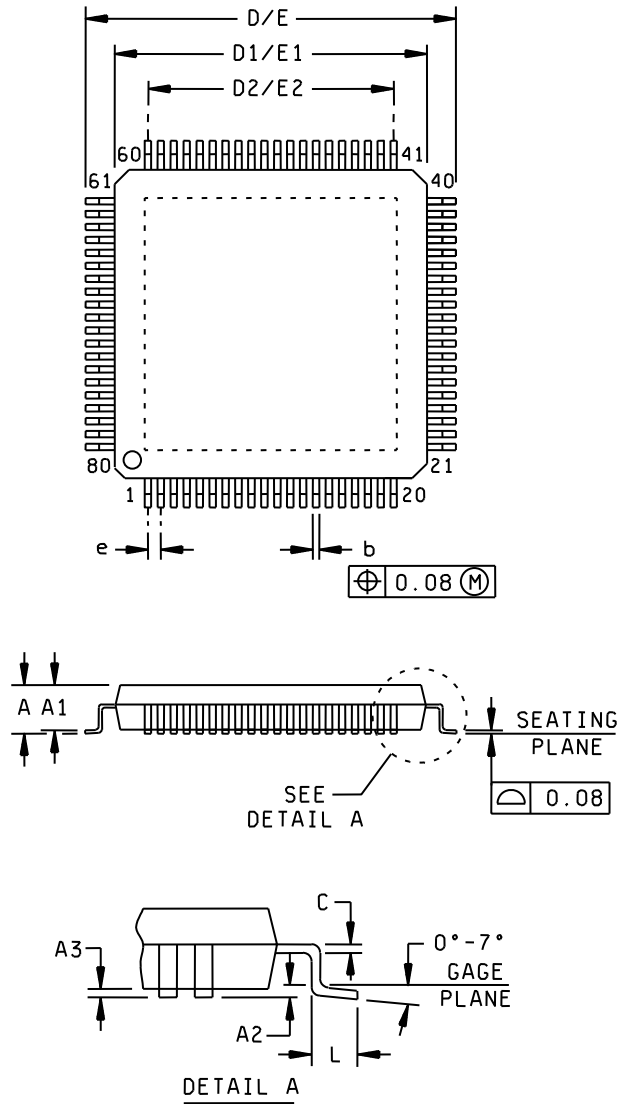


FIGURE 1. Case outline.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/06669</b></p>
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.037	0.041	0.95	1.05
A2	0.009	---	0.25	---
A3	0.001	0.005	0.05	0.15
b	0.006	0.010	0.17	0.27
c	0.005 NOM		0.13 NOM	
D	0.543	0.559	13.80	14.20
D1	0.464	0.480	11.80	12.20
D2	0.037	---	0.95	---
e	0.019 BSC		0.50 BSC	
E	0.543	0.559	13.80	14.20
E1	0.464	0.480	11.80	12.20
E2	0.037	---	0.95	---
L	0.017	0.029	0.45	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout. The vendor datasheet is available from the manufacturer.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outline – Continued.

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Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DVDD	21	AVDD	41	$\overline{\text{OVR}}$	61	$\overline{\text{D5}}$
2	GND	22	GND	42	OVR	62	D5
3	AVDD	23	AVDD	43	NC	63	$\overline{\text{D6}}$
4	NC	24	GND	44	NC	64	D6
5	NC	25	AVDD	45	NC	65	GND
6	VREF	26	GND	46	NC	66	DVDD
7	GND	27	AVDD	47	NC	67	$\overline{\text{D7}}$
8	AVDD	28	GND	48	NC	68	D7
9	GND	29	NC	49	$\overline{\text{D0}}$	69	$\overline{\text{D8}}$
10	CLK	30	GND	50	D0	70	D8
11	$\overline{\text{CLK}}$	31	AVDD	51	DVDD	71	$\overline{\text{D9}}$
12	GND	32	GND	52	GND	72	D9
13	AVDD	33	NC	53	$\overline{\text{D1}}$	73	$\overline{\text{D10}}$
14	AVDD	34	GND	54	D1	74	D10
15	GND	35	AVDD	55	$\overline{\text{D2}}$	75	$\overline{\text{D11}}$
16	AIN	36	GND	56	D2	76	D11
17	$\overline{\text{AIN}}$	37	AVDD	57	$\overline{\text{D3}}$	77	$\overline{\text{D12}}$
18	GND	38	GND	58	D3	78	D12
19	AVDD	39	AVDD	59	$\overline{\text{D4}}$	79	$\overline{\text{DRY}}$
20	GND	40	GND	60	D4	80	DRY

NC = No connection

FIGURE 2. Terminal connections.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06669</b>
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Terminal symbol	Description
AVDD	Analog power supply.
DVDD	Output driver power supply.
GND	Ground.
VREF	Reference voltage.
CLK	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	Differential input clock (negative).
A $\overline{\text{IN}}$	Differential input signal (positive).
$\overline{\text{AIN}}$	Differential input signal (negative).
OVR, $\overline{\text{OVR}}$	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, $\overline{\text{D0}}$	LVDS digital output pair, least-significant bit (LSB).
D1 - D6, $\overline{\text{D1}}$ - $\overline{\text{D6}}$	LVDS digital output pairs.
D7 - D11, $\overline{\text{D7}}$ - $\overline{\text{D11}}$	LVDS digital output pairs.
D12, $\overline{\text{D12}}$	LVDS digital output pair, most significant bit (MSB).
DRY, $\overline{\text{DRY}}$	Data ready LVDS output pair.
NC	No connection.

FIGURE 2. Terminal connections – continued.

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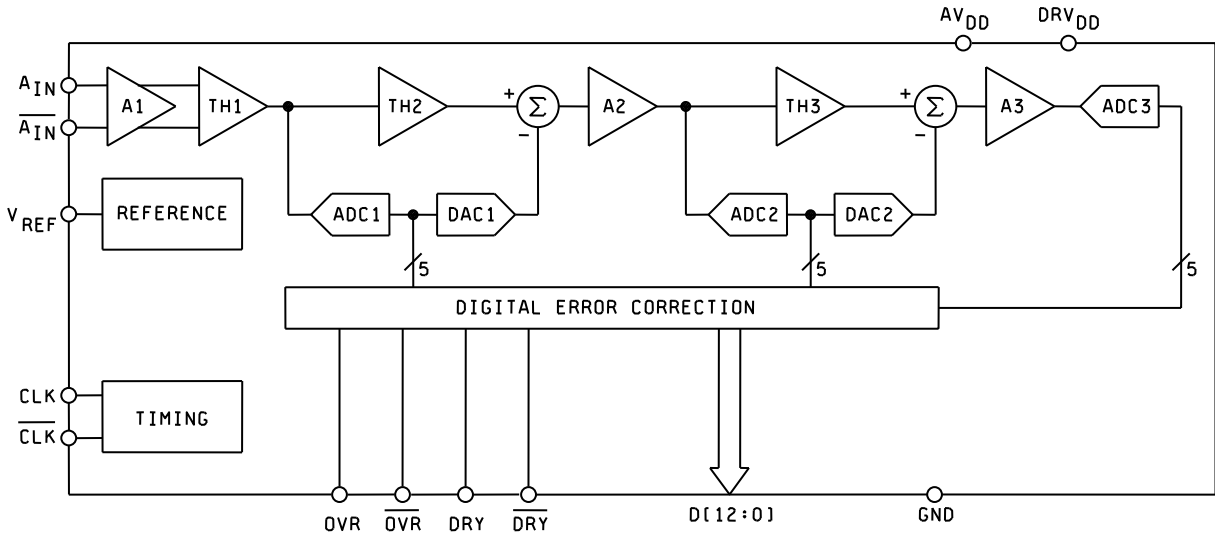


FIGURE 3. Block diagram.

<b>DEFENSE SUPPLY CENTER, COLUMBUS</b> <b>COLUMBUS, OHIO</b>	<b>SIZE</b> <b>A</b>	<b>CODE IDENT NO.</b> <b>16236</b>	<b>DWG NO.</b> <b>V62/06669</b>
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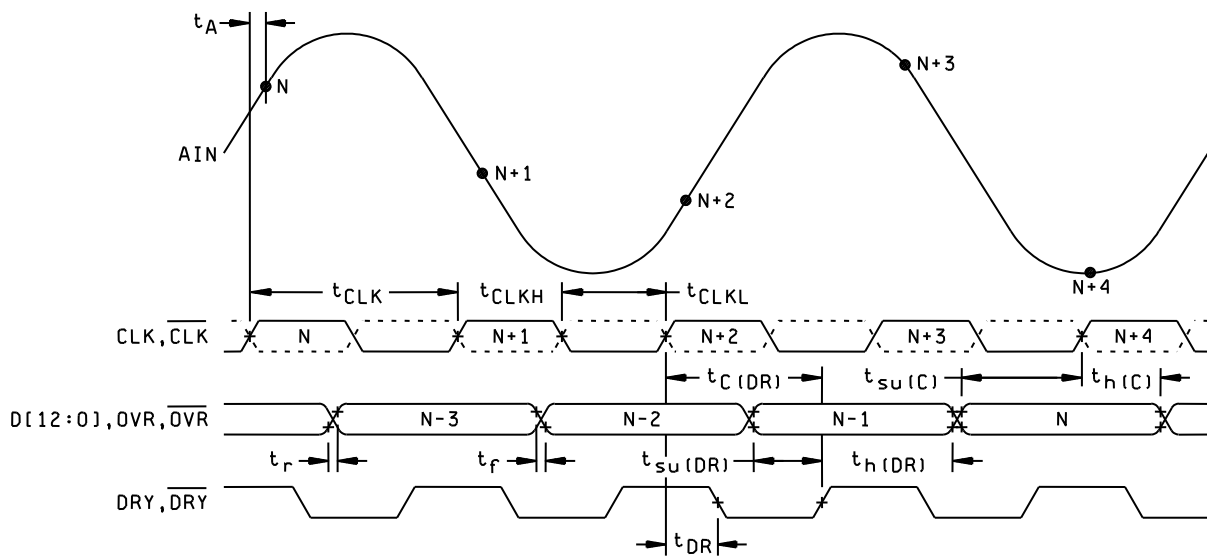


FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package <u>2/</u> lead	Transport media, quantity	Package marking	Vendor part number
V62/06669-01XE	01295	HTQFP-80 (thermal pad)	Tray, 96	ADS5440M-EP	ADS5440MPFPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Thermal pad size: 7.5 mm x 7.5 mm ( 0.2952 inch ) typical.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06669</b>
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