REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	14-08-06	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	20-07-15	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-08-31	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 13-BIT, 250 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06668**
	REV **B**	**PAGE** 1 **OF** 16

AMSC N/A

5962-V035-20

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 13-bit, 250 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06668	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADS5444-EP	13 bit, 250 MSPS, analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	80	MS-026	Plastic quad flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage :
- AV_{DD} to GND ..... 6 V
- DRV_{DD} to GND ..... 5 V

Analog input to GND ..... -0.3 V to AV_{DD} + 0.3 V
Clock input to GND ..... -0.3 V to AV_{DD} + 0.3 V
CLK to $\overline{CLK}$ ..... ±2.5 V
Digital data output to GND ..... -0.3 V to DRV_{DD} + 0.3 V
Maximum junction temperature (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Electrostatic discharge (ESD) human body model (HBM) ..... 2.5 kV

1.4 Recommended operating conditions. 2/

Supplies:
- Analog supply voltage (AV_{DD}) ..... 4.75 V to 5.25 V
- Output driver supply voltage (DRV_{DD}) ..... 3 V to 3.6 V

Analog input:
- Differential input range ..... 2.2 V_{PP} nominal
- Input common mode voltage (V_{CM}) ..... 2.4 V nominal

Clock input:
- ADCLK input sample rate (sine wave) ($1/t_C$) ..... 10 MSPS to 250 MSPS
- Clock amplitude, differential sine wave ..... 3 V_{PP} nominal
- Clock duty cycle ..... 50 % nominal

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. 3/

Parameter	Test conditions	Typical limits
θ_{JA}	Soldered slug, no airflow	21.7°C/W
θ_{JA}	Soldered slug, 250 LPFM airflow	15.4°C/W
θ_{JA}	Unsoldered slug, no airflow	50°C/W
θ_{JA}	Unsoldered slug, 250 LPFM airflow	43.4°C/W
θ_{JC}	Bottom of package (heat slug)	2.99°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
3/ Using 36 thermal vias (6 x 6 array). See application section of vendor datasheet.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +125°C	01	13 typical		Bits
Analog inputs section							
Differential input range			-55°C to +125°C	01	2.2 typical		V_{PP}
Differential input resistance (DC)	R_{DI}		-55°C to +125°C	01	1 typical		kΩ
Differential input capacitance	C_{DI}		-55°C to +125°C	01	1.5 typical		pF
Analog input bandwidth			-55°C to +125°C	01	800 typical		MHz
Internal reference voltages section							
Reference voltage	V_{REF}		-55°C to +125°C	01	2.4 typical		V
Dynamic accuracy section							
No missing codes			-55°C to +125°C	01	Assured typical		
Differential linearity error	DNL	f_{IN} = 10 MHz	+25°C	01	-1	1	LSB
			-55°C to +125°C		-1	2	
Integral linearity error	INL	f_{IN} = 10 MHz	+25°C	01	-2.2	2.2	LSB
			-55°C to +125°C		-4.3	4.3	
Offset error			-55°C to +125°C	01	-11	11	mV
Offset temperature coefficient			-55°C to +125°C	01	0.0005 typical		mV / °C
Gain error			-55°C to +125°C	01	-5	5	%FS
Gain temperature coefficient			-55°C to +125°C	01	-0.02 typical		Δ% / °C
Power supply rejection ratio	PSRR	f_{IN} = 100 MHz	-55°C to +125°C	01	1 typical		mV/V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
Analog supply current	I_{AVDD}	V_{IN} = full scale, f_{IN} = 100 MHz, F_S = 250 MSPS	-55°C to +125°C	01		430	mA
Output buffer supply current	I_{DRVDD}	V_{IN} = full scale, f_{IN} = 100 MHz, F_S = 250 MSPS	-55°C to +125°C	01		100	mA
Power dissipation	P_D	V_{IN} = full scale, f_{IN} = 100 MHz, F_S = 250 MSPS	-55°C to +125°C	01		2.37	W
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f_{IN} = 10 MHz	-55°C to +125°C	01	69.3 typical		dBc
		f_{IN} = 70 MHz			69 typical		
		f_{IN} = 100 MHz	25°C		67		
			-55°C to +125°C		64.25		
		f_{IN} = 170 MHz	-55°C to +125°C		68.3 typical		
		f_{IN} = 230 MHz			67.7 typical		
		f_{IN} = 300 MHz			67 typical		
		f_{IN} = 400 MHz			66 typical		
Spurious free dynamic range	SFDR	fIN = 10 MHz	-55°C to +125°C	01	85 typical		dBc
		fIN = 70 MHz			77 typical		
		f_{IN} = 100 MHz	25°C		70		
			-55°C to +125°C		64		
		f_{IN} = 170 MHz	-55°C to +125°C		74 typical		
		f_{IN} = 230 MHz			77 typical		
		f_{IN} = 300 MHz			70 typical		
		f_{IN} = 400 MHz			64 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Second harmonic	HD2	f_{IN} = 10 MHz	-55°C to +125°C	01	87 typical		dBc
		f_{IN} = 70 MHz			77 typical		
		f_{IN} = 100 MHz			80 typical		
		f_{IN} = 170 MHz			74 typical		
		f_{IN} = 230 MHz			78 typical		
		f_{IN} = 300 MHz			70 typical		
		f_{IN} = 400 MHz			64 typical		
Third harmonic	HD3	f_{IN} = 10 MHz	-55°C to +125°C	01	86 typical		dBc
		f_{IN} = 70 MHz			82 typical		
		f_{IN} = 100 MHz			79 typical		
		f_{IN} = 170 MHz			80 typical		
		f_{IN} = 230 MHz			91 typical		
		f_{IN} = 300 MHz			80 typical		
		f_{IN} = 400 MHz			69 typical		
Worst harmonic / spur (other than HD2 and HD3)		f_{IN} = 10 MHz	-55°C to +125°C	01	90 typical		dBc
		f_{IN} = 70 MHz			95 typical		
		f_{IN} = 100 MHz			82 typical		
		f_{IN} = 170 MHz			80 typical		
		f_{IN} = 230 MHz			83 typical		
		f_{IN} = 300 MHz			86 typical		
		f_{IN} = 400 MHz			85 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic AC characteristics section - continued.							
Signal-to-noise + distortion	SINAD	f_{IN} = 10 MHz	-55°C to +125°C	01	69 typical		dBc
		f_{IN} = 70 MHz			68 typical		
		f_{IN} = 100 MHz			67.6 typical		
		f_{IN} = 170 MHz			66.5 typical		
		f_{IN} = 230 MHz			67 typical		
		f_{IN} = 300 MHz			65 typical		
		f_{IN} = 400 MHz			61 typical		
Effective number of bits	ENOB	f_{IN} = 10 MHz	-55°C to +125°C	01	11.2 typical		Bits
RMS idle channel noise		Input pins tied to common mode	-55°C to +125°C	01	0.4 typical		LSB
Digital characteristics - LVDS digital outputs							
Differential output voltage	V_{DO}		-55°C to +125°C	01	0.247	0.452	V
Output offset voltage	V_{OS}		-55°C to +125°C	01	1.125	1.375	V
Timing characteristics							
Aperture delay	t_A		-55°C to +125°C	01	500 typical		ps
Clock scope independent aperture uncertainty (jitter)	t_J		-55°C to +125°C	01	200 typical		fs RMS
Latency			-55°C to +125°C	01	4 typical		cycles

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Clock input section		See figure 4					
Clock period	t_{CLK}		-55°C to +125°C	01	4 typical		ns
Clock pulse width high	t_{CLKH}		-55°C to +125°C	01	2 typical		ns
Clock pulse width low	t_{CLKL}		-55°C to +125°C	01	2 typical		ns
Clock to data ready (DRY) section		See figure 4					
Clock rising to data ready falling	t_{DR}		-55°C to +125°C	01	1.1 typical		ns
Clock rising to data ready rising	$t_{C(DR)}$	Clock duty cycle = 50 % 3/	-55°C to +125°C	01	2.7	3.5	ns
Clock to DATA, over range (OVR) section 4/		See figure 4					
Data rise time (20% to 80%)	t_r		-55°C to +125°C	01	0.6 typical		ns
Data fall time (80% to 20%)	t_f		-55°C to +125°C	01	0.6 typical		ns
Data valid to clock (setup time)	$t_{su(C)}$		-55°C to +125°C	01	3.1 typical		ns
Clock to invalid data (hold time)	$t_{h(C)}$		-55°C to +125°C	01	0.2 typical		ns
Data ready (DRY) to DATA, over range (OVR) section		See figure 4					
Data valid to DRY	$t_{su(DR)}$		-55°C to +125°C	01	1.7		ns
Data ready (DRY) to invalid data	$t_{h(DR)}$		-55°C to +125°C	01	0.9		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, sampling rate = 250 MSPS, 50 % clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, -1 dBFS differential input, and 3 V_{PP} differential cock.

3/ $t_{C\_DR} = t_{DR} + t_{CLKH}$ for clock duty cycles other than 50%.

4/ Data is updated with clock falling edge or data ready (DRY) rising edge.

Case X

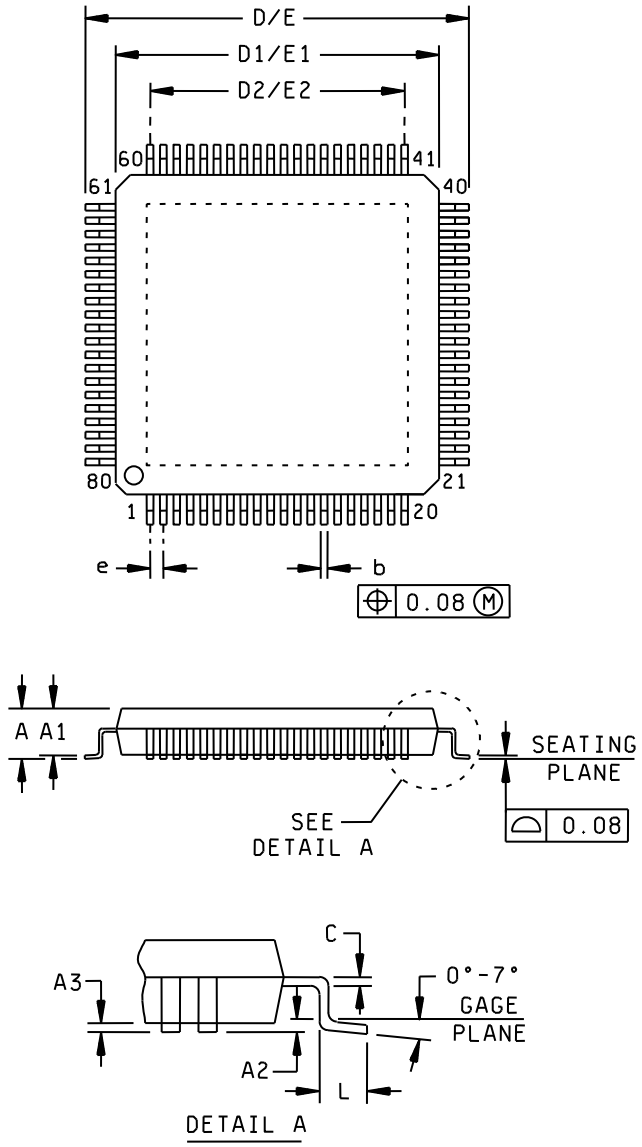

FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.037	0.041	0.95	1.05
A2	0.009	---	0.25	---
A3	0.001	0.005	0.05	0.15
b	0.006	0.010	0.17	0.27
c	0.005 NOM		0.13 NOM	
D	0.543	0.559	13.80	14.20
D1	0.464	0.480	11.80	12.20
D2	0.37	---	9.50	---
e	0.019 BSC		0.50 BSC	
E	0.543	0.559	13.80	14.20
E1	0.464	0.480	11.80	12.20
E2	0.37	---	9.50	---
L	0.017	0.029	0.45	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout. The datasheet is available from the manufacturer.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outline – Continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DV_{DD}	21	AV_{DD}	41	$\overline{OVR}$	61	$\overline{D5}$
2	GND	22	GND	42	OVR	62	D5
3	AV_{DD}	23	AV_{DD}	43	NC	63	$\overline{D6}$
4	NC	24	GND	44	NC	64	D6
5	NC	25	AV_{DD}	45	NC	65	GND
6	V_{REF}	26	GND	46	NC	66	DV_{DD}
7	GND	27	AV_{DD}	47	NC	67	$\overline{D7}$
8	AV_{DD}	28	GND	48	NC	68	D7
9	GND	29	NC	49	$\overline{D0}$	69	$\overline{D8}$
10	CLK	30	GND	50	D0	70	D8
11	$\overline{CLK}$	31	AV_{DD}	51	DV_{DD}	71	$\overline{D9}$
12	GND	32	GND	52	GND	72	D9
13	AV_{DD}	33	NC	53	$\overline{D1}$	73	$\overline{D10}$
14	AV_{DD}	34	GND	54	D1	74	D10
15	GND	35	AV_{DD}	55	$\overline{D2}$	75	$\overline{D11}$
16	AIN	36	GND	56	D2	76	D11
17	$\overline{AIN}$	37	AV_{DD}	57	$\overline{D3}$	77	$\overline{D12}$
18	GND	38	GND	58	D3	78	D12
19	AV_{DD}	39	AV_{DD}	59	$\overline{D4}$	79	$\overline{DRY}$
20	GND	40	GND	60	D4	80	DRY

NC = No connection

FIGURE 2. Terminal connections.

Terminal symbol	Description
AV_{DD}	Analog power supply.
DV_{DD}	Output driver power supply.
GND	Ground.
V_{REF}	Reference voltage.
CLK	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{CLK}$	Differential input clock (negative).
AIN	Differential input signal (positive).
$\overline{AIN}$	Differential input signal (negative).
OVR, $\overline{OVR}$	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, $\overline{D0}$	LVDS digital output pair, least-significant bit (LSB).
D1 - D6, $\overline{D1}$ - $\overline{D6}$	LVDS digital output pairs.
D7 – D11, $\overline{D7}$ - $\overline{D11}$	LVDS digital output pairs.
D12, $\overline{D12}$	LVDS digital output pair, most significant bit (MSB).
DRY, $\overline{DRY}$	Data ready LVDS output pair.
NC	No connection.

FIGURE 2. Terminal connections – continued.

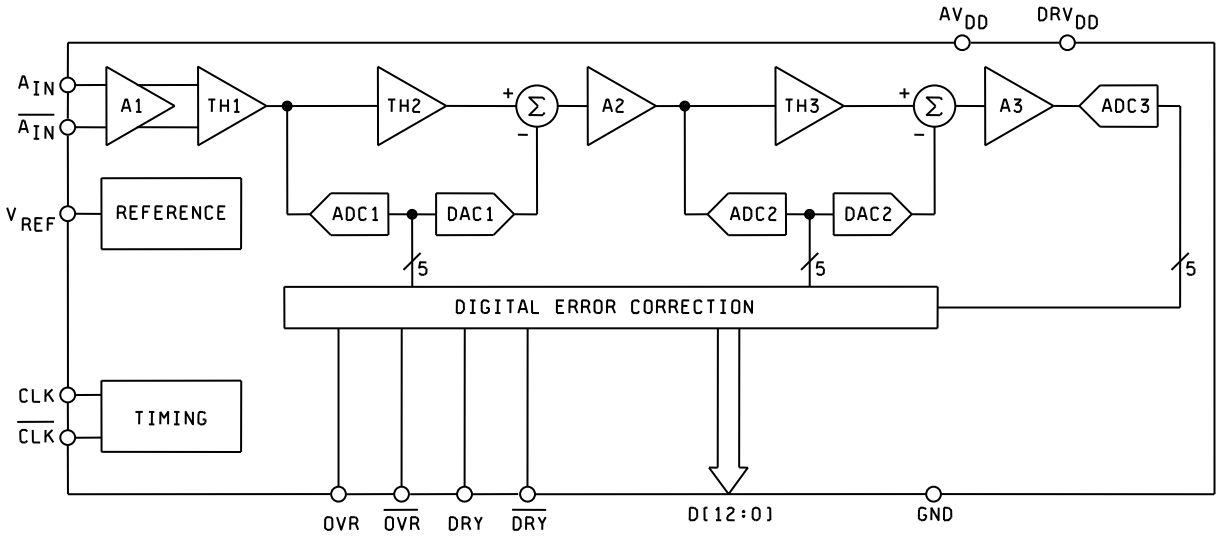

FIGURE 3. Block diagram.

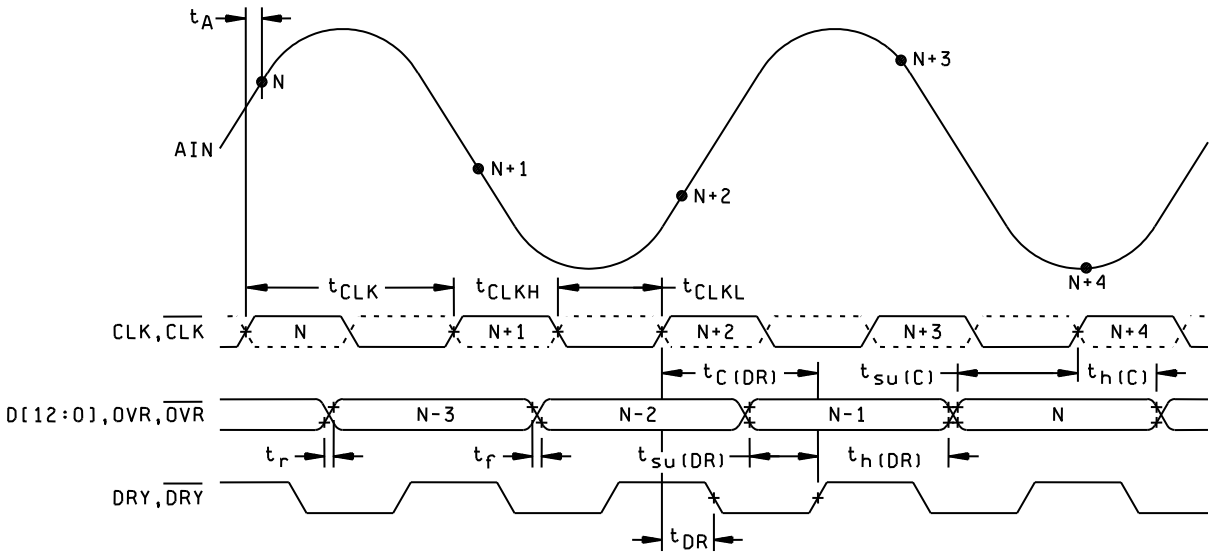

FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/ lead	Mode of transportation and quantity	Top side marking	Vendor part number
V62/06668-01XE	01295	HTQFP-80 (thermal pad)	TRAY, 96	ADS5444M-EP	ADS5444MPFPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Thermal pad size: 7.5 mm x 7.5 mm (0.2952 inch) typical.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243