REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-06-24	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	21-12-09	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B									
	PAGE		1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-08-23	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06667**
	REV **B**	**PAGE** 1 **OF** 10

AMSC N/A

5962-V114-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer/driver with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06667	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ABT244A-EP	Octal buffer/driver with 3-state outputs

1.2.2 Case outlines. The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-150	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7 V
Input voltage range (V_I) ..... -0.5 V to 7 V 2/
Voltage range applied to any output
in the high or power-off state (V_O) ..... -0.5 V to 5.5 V
Current into any output in the low state (I_O) ..... 96 mA
Input clamp current (I_{IK}) ($V_I < 0$) ..... -18 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Package thermal impedance (θ_{JA}) ..... 115°C/W 3/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC}) ..... 4.5 V to 5.5 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Input voltage range (V_I) ..... 0 V to V_{CC}
Maximum high level output current (I_{OH}) ..... -24 mA
Maximum low level output current (I_{OL}) ..... 48 mA
Input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled) ..... 5 ns/V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ Unused inputs must be held high or low to prevent them from floating.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	4.5 V	25°C, -55°C to 125°C	All		-1.2	V
High level output voltage	V_{OH}	I_{OH} = -3 mA	4.5 V			2.5		V
		I_{OH} = -3 mA	5 V			3		
		I_{OH} = -24 mA	4.5 V			2		
Low level output voltage	V_{OL}	I_{OL} = 48 mA	4.5 V				0.55	V
Hysteresis voltage	V_{hys}		5 V	25°C		100 TYP		mV
Input current	I_I	V_I = V_{CC} or GND	5.5 V	25°C, -55°C to 125°C			±1	µA
3-state output current high	I_{OZH}	V_O = 2.7 V	5.5 V				10	µA
3-state output current low	I_{OZL}	V_O = 0.5 V	5.5 V				-10	µA
Input/output power-off leakage current	I_{off}	V_I or $V_O \leq$ 5.5 V	0 V	25°C			±100	µA
Output high leakage current	I_{CEX}	Outputs high	5.5 V	25°C, -55°C to 125°C			50	µA
Output current	I_O 2/	V_O = 2.5 V	5.5 V			-50	−180	µA
Quiescent supply current	I_{CC}	Outputs high. V_I = V_{CC} or GND, I_O = 0 A	5.5 V				250	µA
		Outputs low. V_I = V_{CC} or GND, I_O = 0 A					30	mA
		Outputs disabled. V_I = V_{CC} or GND, I_O = 0 A					250	µA
Quiescent supply current delta	ΔI_{CC} 3/	Data inputs. Outputs enabled. One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V				1.5	mA
		Data inputs. Outputs disabled. One input at 3.4 V, Other inputs at V_{CC} or GND					50	µA
		Control inputs. One input at 3.4 V, Other inputs at V_{CC} or GND					1.5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

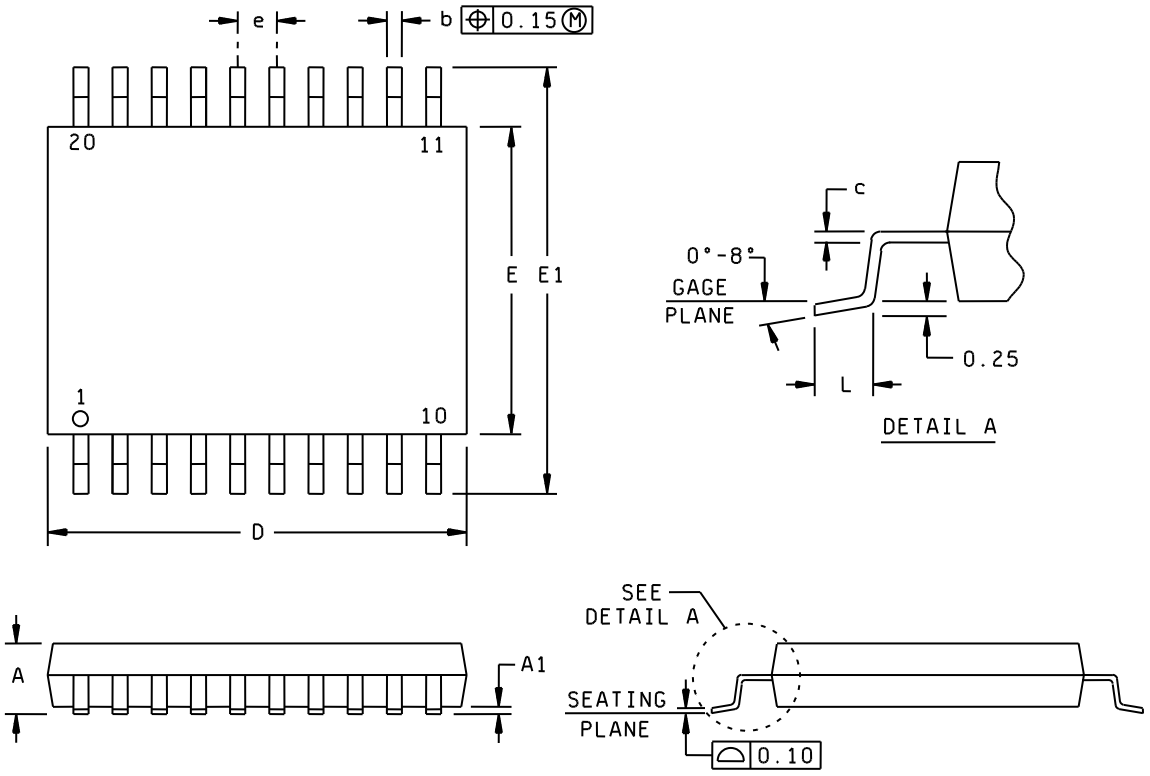
Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Input capacitance	C_i	V_I = 2.5 V or 0.5 V	5 V	25°C	All	3.5 TYP		pF
Output capacitance	C_O	V_O = 2.5 V or 0.5 V	5 V			7.5 TYP		pF
Propagation delay time, A to Y	t_{PLH}	C_L = 50 pF See figure 5.	5 V	25°C		1	4.1	ns
			4.5 V to 5.5 V	-55°C to 125°C		1	5.3	
	t_{PHL}		5 V	25°C		1	4.2	
			4.5 V to 5.5 V	-55°C to 125°C		1	5	
Propagation delay time, output enable, OE to Y	t_{PZH}	C_L = 50 pF See figure 5.	5 V	25°C		1.1	4.6	ns
			4.5 V to 5.5 V	-55°C to 125°C		0.8	5.7	
	t_{PZL}		5 V	25°C		2.1	5.6	
			4.5 V to 5.5 V	-55°C to 125°C		1.2	7.9	
Propagation delay time, output disable, OE to Y	t_{PHZ}	C_L = 50 pF See figure 5.	5 V	25°C		2.1	5.6	ns
			4.5 V to 5.5 V	-55°C to 125°C		1.2	7.6	
	t_{PLZ}		5 V	25°C		1.5	5.6	
			4.5 V to 5.5 V	-55°C to 125°C		1	7.9	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00	---	0.079	E	5.00	5.60	0.197	0.220
A1	0.05	---	0.002	---	E1	7.40	8.20	0.291	0.323
b	0.22	0.38	0.009	0.015	e	0.65 BSC		0.026 BSC	
c	0.09	0.25	0.004	0.010	L	0.55	0.95	0.022	0.037
D	6.90	7.50	0.272	0.295					

NOTES:
1. All linear dimensions are in millimeters (inches). Inches equivalents are shown for general reference only.
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-150.

FIGURE 1. Case outline.

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

H = High voltage level X = Immaterial
L = Low voltage level Z = High-impedance state

FIGURE 2. Function table.

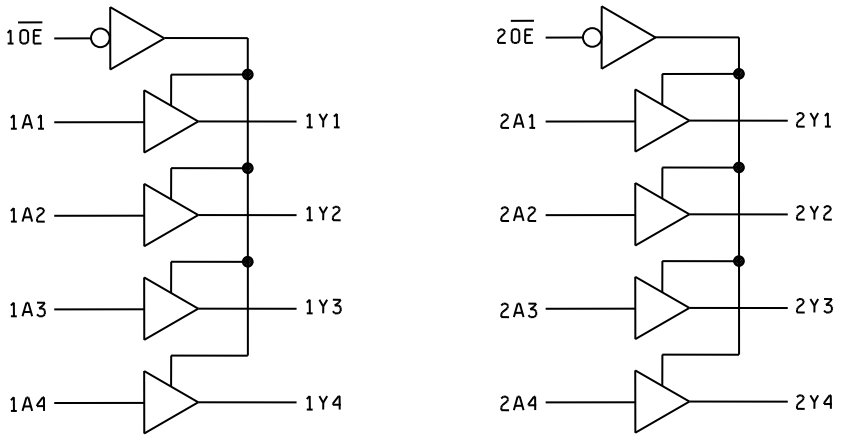
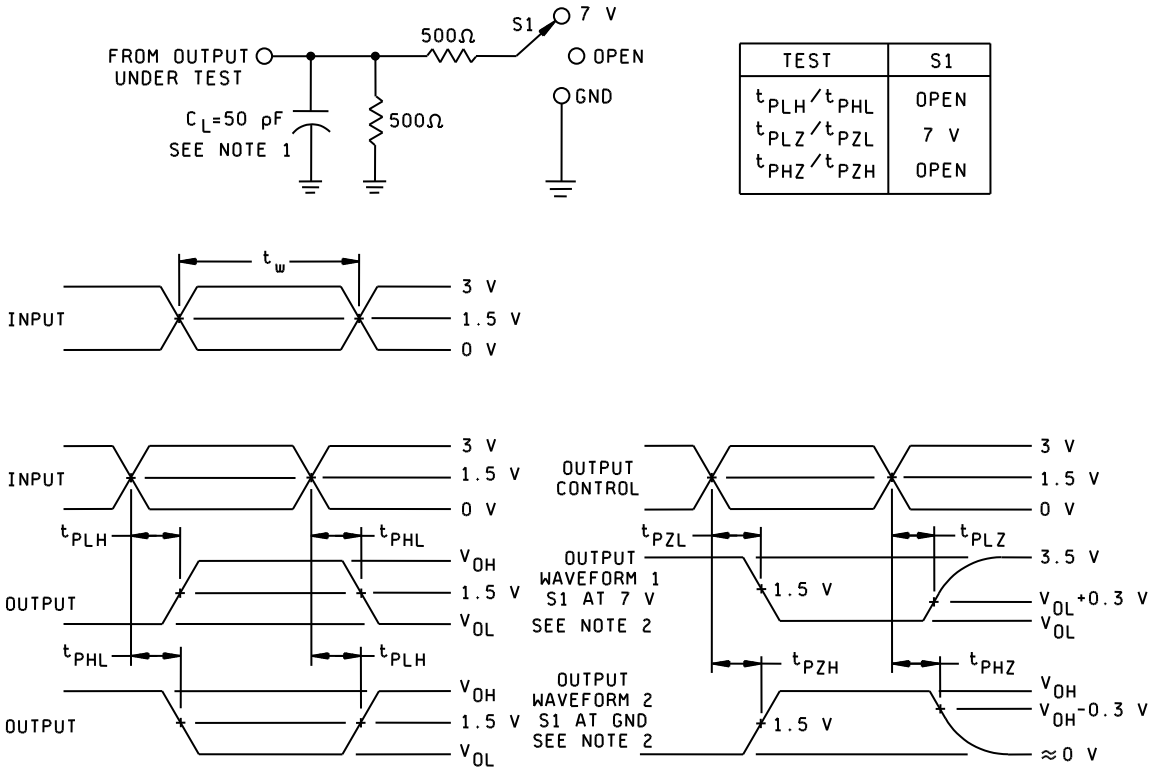


FIGURE 3. Logic diagram.

Device type:	All		
Case outline:	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1$\overline{OE}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2$\overline{OE}$
10	GND	20	V_{CC}

FIGURE 4. Terminal connections.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, and t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06667-01XE	01295	SN74ABT244AMDBREP	ABT244AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243