REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-06-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A									
	PAGE		1	2	3	4	5	6	7	8	9	10	11									

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO**
Original date of drawing YY MM DD 07-05-02	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06665**
	REV A	**PAGE** 1 **OF** 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual retriggerable mono stable multi vibrator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06665	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AHC123A-EP	Dual retriggerable mono stable multi vibrator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +7.0 V 2/
Input voltage range (V_I) ..... -0.5 V to +7.0 V 3/
Output voltage range in high or low state (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Output voltage range in power off state (V_O) ..... -0.5 V to +7.0 V 2/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -20 mA
Output clamp current (I_{OK}) ($V_O <$ 0 V or $V_O < V_{CC}$) ..... ±20 mA
Continuous output current (I_O) (V_O = 0 V to V_{CC})..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}) ..... 73°C/W 4/
Storage temperature range (T_{STG})..... -65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage (V_{CC}) ..... 2.0 V to +5.5 V
Minimum high level input voltage (V_{IH}):
V_{CC} = 2.0 V ..... +1.5 V
V_{CC} = 3.0 V ..... +2.1 V
V_{CC} = 5.5 V ..... +3.85 V
Maximum low level input voltage (V_{IL}):
V_{CC} = 2.0 V ..... +0.5 V
V_{CC} = 3.0 V ..... +0.9 V
V_{CC} = 5.5 V ..... +1.65 V
Input voltage (V_I) ..... 0 V to 5.5 V
Output voltage (V_O) ..... 0 to V_{CC}
Maximum high level output current (I_{OH}):
V_{CC} = 2.0 V ..... -50 µA
V_{CC} = 3.3 V ±0.3 V ..... -4 mA
V_{CC} = 5 V ±0.5 V ..... -8 mA
Maximum low level output current (I_{OL}):
V_{CC} = 2.0 V ..... 50 µA
V_{CC} = 3.3 V ±0.3 V ..... 4 mA
V_{CC} = 5 V ±0.5 V ..... 8 mA
Minimum external timing resistance:
V_{CC} = 2.0 V ..... 5 kΩ
V_{CC} > 3.0 V ..... 1 kΩ V
Minimum power up ramp rate ($\Delta t/\Delta V_{CC}$) .....1 ms/V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Voltage values are with respect to the network ground terminal.
3/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Unused Rext/Cext terminals should be left unconnected. All remaining unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Input/Output timing diagram. The input/output timing diagram shall be as shown in figure 5.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions unless otherwise specified	V_{CC}	Limits				Unit
					T_A = 25°C		-55°C ≤ T_A ≤ 125°C		
					Min	Max	Min	Max	
High level output voltage		V_{OH}	I_{OH} = -50 μA	2 V	1.9		1.9		V
				3 V	2.9		2.9		
				4.5 V	4.4		4.4		
			I_{OH} = -4 mA	3 V	2.58		2.48		
			I_{OH} = -8 mA	4.5 V	3.94		3.8		
Low level output voltage		V_{OL}	I_{OL} = 50 μA	2 V		0.1		0.1	V
				3 V		0.1		0.1	
				4.5 V		0.1		0.1	
			I_{OL} = 4 mA	3 V		0.36		0.44	
			I_{OL} = 8 mA	4.5 V		0.36		0.44	
Input current	R_{ext}/C_{ext} 2/	I_I	V_I = V_{CC} or GND	5.5 V		±0.25		±2.5	μA
	$\overline{A}$, B, and $\overline{CLR}$		V_I = V_{CC} or GND	0 V to 5.5 V		±0.1		±1 3/	
Quiescent supply current		I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V		4		40	μA
Active state (per circuit)		I_{CC}	V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V		250		280	μA
				4.5 V		500		650	
				5.5 V		750		975	
Input capacitance		C_i	V_I = V_{CC} or GND	5 V		10		10	pF
Pulse duration	$\overline{CLR}$	t_w		3.3 V ±0.3 V	5		5		ns
				5 V ±0.5 V	5		5		
	$\overline{A}$ or B trigger			3.3 V ±0.3 V	5		5		
				5 V ±0.5 V	5		5		
Pulse retrigger time		t_{rr}	R_{ext} = 1 kΩ, C_{ext} = 100 pF	3.3 V ±0.3 V	4/ 76 Typ		4/		ns
			R_{ext} = 1 kΩ, C_{ext} = 0.01 μF		4/ 1.8 Typ		4/		
			R_{ext} = 1 kΩ, C_{ext} = 100 pF	5 V ±0.5 V	4/ 59 Typ		4/		μs
			R_{ext} = 1 kΩ, C_{ext} = 0.01 μF		4/ 1.5 Typ		4/		
Switching characteristics									
From input $\overline{A}$ or B to output Q or $\overline{Q}$		t_{PLH}	C_L = 15 pF	3.3 V ±0.3 V		20.6 5/		24 5/	ns
				5 V ±0.5 V		12 5/		14 5/	
		t_{PHL}		3.3 V ±0.3 V		20.6 5/		24 5/	
				5 V ±0.5 V		12 5/		14 5/	

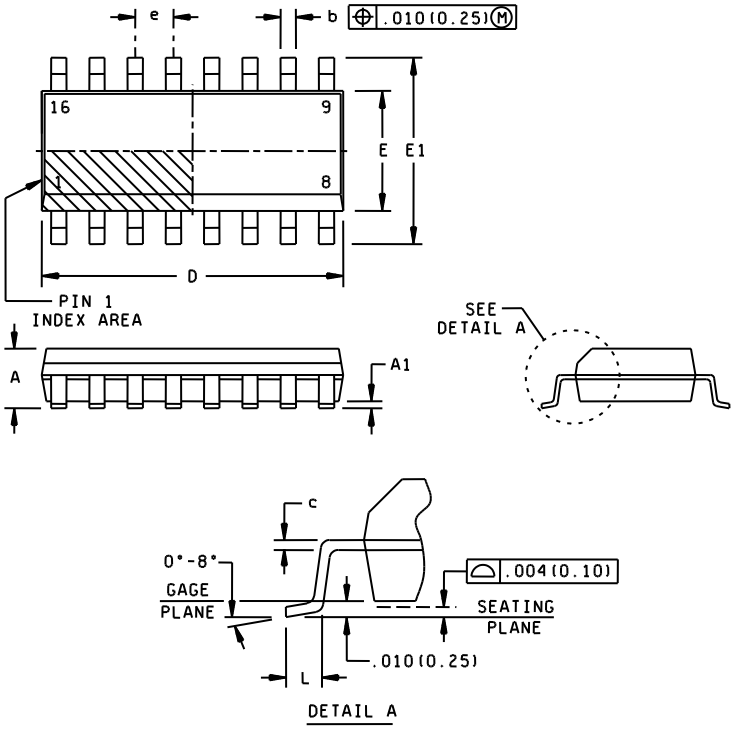
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions unless otherwise specified	V_{CC}	Limits				Unit
				T_A = 25°C		-55°C ≤ T_A ≤ 125°C		
				Min	Max	Min	Max	
Switching characteristics - continued								
From input $\overline{CLR}$ to output Q or $\overline{Q}$	t_{PLH}	C_L = 15 pF	3.3 V ±0.3 V		15.8 5/		18.5 5/	ns
			5 V ±0.5 V		9.4 5/		11 5/	
	t_{PHL}		3.3 V ±0.3 V		15.8 5/		18.5 5/	
			5 V ±0.5 V		9.4 5/		11 5/	
From input $\overline{CLR}$ trigger to output Q or $\overline{Q}$	t_{PLH}		3.3 V ±0.3 V		22.4 5/		26 5/	
			5 V ±0.5 V		12.9 5/		15 5/	
	t_{PHL}		3.3 V ±0.3 V		22.4 5/		26 5/	
			5 V ±0.5 V		12.9 5/		15 5/	
From input $\overline{A}$ or B to output Q or $\overline{Q}$	t_{PLH}	C_L = 50 pF	3.3 V ±0.3 V		24.1		27.5	
			5 V ±0.5 V		14		16	
	t_{PHL}		3.3 V ±0.3 V		24.1		27.5	
			5 V ±0.5 V		14		16	
From input $\overline{CLR}$ to output Q or $\overline{Q}$	t_{PLH}		3.3 V ±0.3 V		19.3		22	
			5 V ±0.5 V		11.4		13	
	t_{PHL}		3.3 V ±0.3 V		19.3		22	
			5 V ±0.5 V		11.4		13	
From input $\overline{CLR}$ trigger to output Q or $\overline{Q}$	t_{PLH}		3.3 V ±0.3 V		25.9		29.5	
			5 V ±0.5 V		14.9		17	
	t_{PHL}		3.3 V ±0.3 V		25.9		29.5	
			5 V ±0.5 V		14.9		17	
Pulse duration at Q or $\overline{Q}$	t_w	C_L = 50 pF, C_{ext} = 28 μF, R_{ext} = 2 kΩ	3.3 V ±0.3 V		240		300	ns
			5 V ±0.5 V		200		240	
		C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	3.3 V ±0.3 V		110		110	μs
			5 V ±0.5 V		110		110	
		C_L = 50 pF, C_{ext} = 0.1 μF, R_{ext} = 10 kΩ	3.3 V ±0.3 V		1.1		1.1	ms
			5 V ±0.5 V		1.1		1.1	
Output pulse duration variation (Q or $\overline{Q}$) between circuits in same package			3.3 V ±0.3 V	±1% Typ				
			5 V ±0.5 V	±1% Typ				
Operating Characteristics								
Power dissipation capacitance			5 V	29 Typ				pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ This test is performed with the terminal in the off state condition.
3/ On products compliant to MIL-PRF-38535, this parameter in not production tested at V_{CC} = 0 V.
4/ See retriggering in the manufacturer data.
5/ On products compliant to MIL-PRF-38535, this parameter in not production tested.

Case X



Dimension									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.75	E	.150	.157	3.80	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.007	.010	0.17	0.25	L	.016	.050	0.40	1.27
D	.386	.394	9.80	10.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gat burrs. Mold flash, protrusions, or gat burs shall not exceed .006 inches (0.15 mm) per end.
4. Body width does not include interlead flash. Interlead flash shall not exceed .017 inches (0.43 mm) per side.
5. Falls within JEDEC MS-012 variation AC

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$1\overline{A}$	9	$2\overline{A}$
2	1B	10	2B
3	$1\overline{CLR}$	11	$2\overline{CLR}$
4	$1\overline{Q}$	12	$2\overline{Q}$
5	2Q	13	1Q
6	$2C_{ext}$	14	$1C_{ext}$
7	$2R_{ext}/C_{ext}$	15	$1R_{ext}/C_{ext}$
8	GND	16	V_{CC}

FIGURE 2. Terminal connections.

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L SEE NOTE	H SEE NOTE
X	X	L	L SEE NOTE	H SEE NOTE
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

Note:

These outputs are based on the assumption that the indicated steady-state condition at the $\overline{A}$ and B inputs have been set up long enough to complete any pulse started before the setup.

FIGURE 3. Function table.

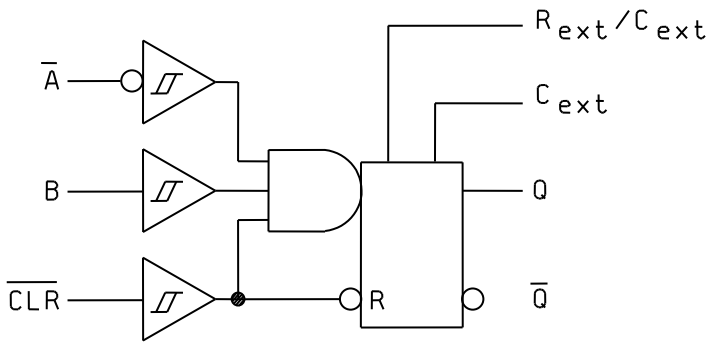


FIGURE 4. Logic diagram.

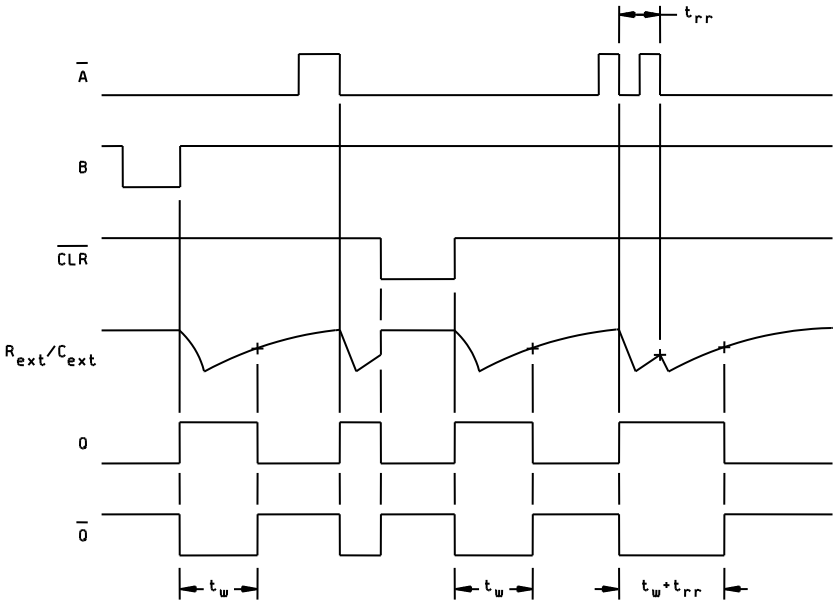
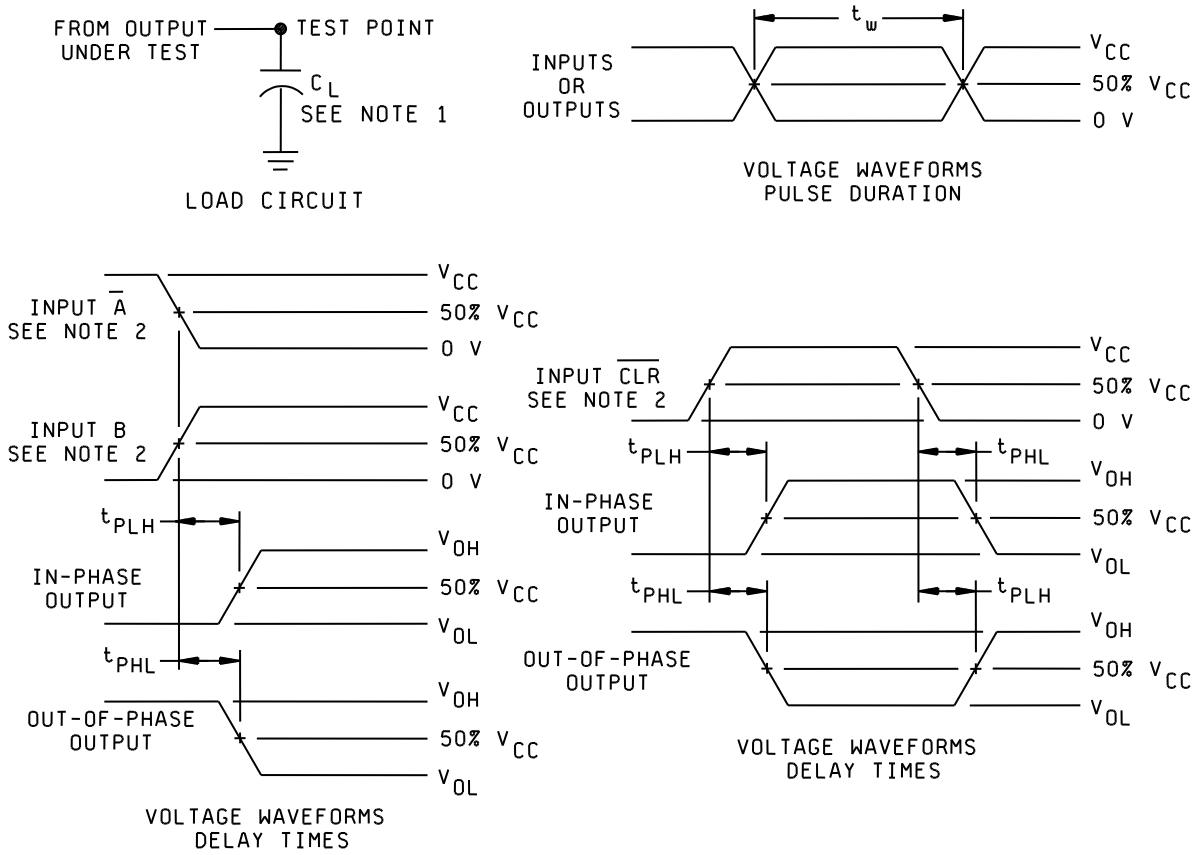


FIGURE 5. Input/output timing diagram



NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns..
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06665-01XE	01295	SN74AHC123AMDREP	AHC123A-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493