

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance hex inverter buffer/driver with open-drain outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06661</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC06A-EP	Hex inverter buffer/driver with open-drain outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	14	MS-012	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_i)	-0.5 V to 6.5 V <u>2/</u>
Output voltage range (V_o)	-0.5 V to 6.5 V
Maximum input clamp current (I_{IK}) ($V_i < 0V$)	-50 mA
Maximum output clamp current (I_{OK}) ($V_o < 0V$)	-50 mA
Maximum continuous output current (I_o)	± 50 mA
Maximum continuous output current through V_{CC} or GND	± 100 mA
Package thermal impedance (θ_{JA}): <u>3/</u>	
X package	86°C/W
Storage temperature range (T_{STG})	-65°C to 150°C
Maximum power dissipation (P_{tot}) ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	500 mW <u>4/</u>

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range (V_{CC}):	
Operating	1.65 V to 3.6 V
Data retention only	1.5 V minimum
Input voltage range (V_i)	0 V to 5.5 V
Output voltage range (V_o)	0 V to 5.5 V
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$
$V_{CC} = 2.3$ V to 2.7 V	1.7 V
$V_{CC} = 2.7$ V to 3.6 V	2 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$
$V_{CC} = 2.3$ V to 2.7 V	0.7 V
$V_{CC} = 2.7$ V to 3.6 V	0.8 V
Maximum low level output current (I_{OL}):	
$V_{CC} = 1.65$ V	4 mA
$V_{CC} = 2.3$ V	8 mA
$V_{CC} = 2.7V$	12 mA
$V_{CC} = 3$ V	24 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- 3/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 4/ Above 70°C the value of P_{tot} derates linearly with 8 mW/K.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 6/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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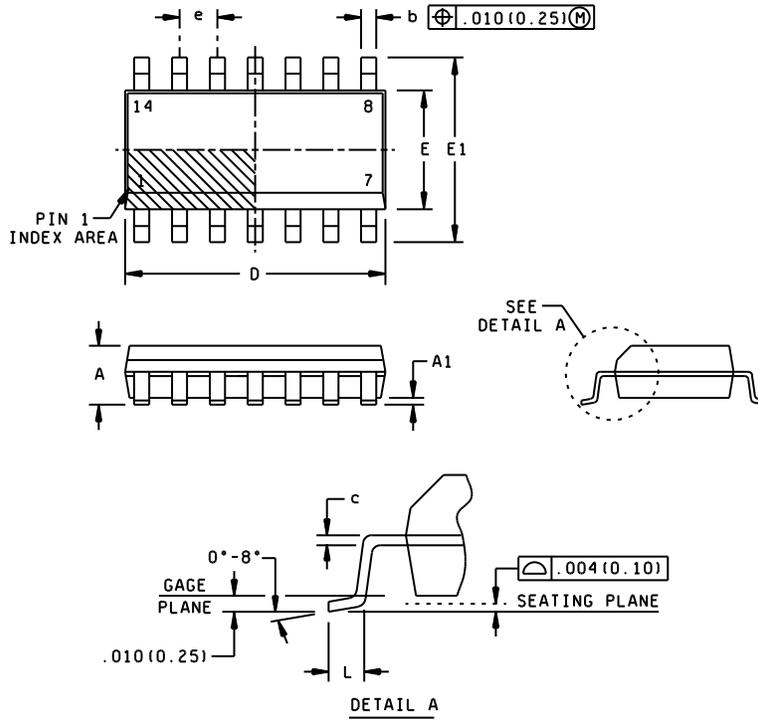
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Limits		Unit
					Min	Max	
Low level output voltage	V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	25°C		0.1	V
				-55°C to +125°C		0.3	
		I _{OL} = 4 mA	1.65 V	25°C		0.24	
				-55°C to +125°C		0.6	
		I _{OL} = 8 mA	2.3 V	25°C		0.3	
				-55°C to +125°C		0.75	
		I _{OL} = 12 mA	2.7 V	25°C		0.4	
				-55°C to +125°C		0.6	
		I _{OL} = 24 mA	3 V	25°C		0.55	
				-55°C to +125°C		0.8	
Input current	I _I	V _I = 5.5 V or GND	3.6 V	25°C		±1	μA
				-55°C to +125°C		±20	
Input/output power-off leakage current	I _{off}	V _I or V _O = 5.5 V	0 V	25°C		±1	μA
				-55°C to +125°C		±20	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	25°C		1	μA
				-55°C to +125°C		40	
Quiescent supply current delta	ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	25°C		500	μA
				-55°C to +125°C		5000	
Input capacitance	C _I	V _I = V _{CC} or GND	3.3 V	25°C		5 TYP	pF
Power dissipation capacitance per buffer/driver	C _{pd}	f = 10 MHz	1.8 V	25°C		2.1 TYP	pF
			2.5 V			2.3 TYP	
			3.3 V			2.5 TYP	
Propagation delay time, A to Y	t _{pd}	See figure 5.	1.65 V to 1.95 V	25°C	1.4	5.1	ns
				-55°C to +125°C	1.4	7.6	
			2.3 V to 2.7 V	25°C	1	2.8	
				-55°C to +125°C	1	4	
			2.7 V	25°C	1	3.7	
				-55°C to +125°C	1	5	
			3.0 V to 3.6 V	25°C	1	3.5	
				-55°C to +125°C	1	5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.80	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.012	0.020	0.31	0.51	e	0.050 BSC		1.27 BSC	
c	0.007	0.010	0.17	0.25	L	0.016	0.050	0.40	1.27
D	0.337	0.344	8.55	8.75					

NOTES:

1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0.15) per end.
4. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0.43) per side.
5. Reference JEDEC MS-012 variation AB.

FIGURE 1. Case outline.

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Input	Output
A	Y
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

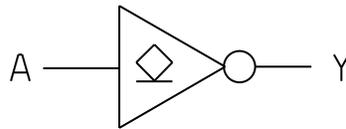


FIGURE 3. Logic diagram.

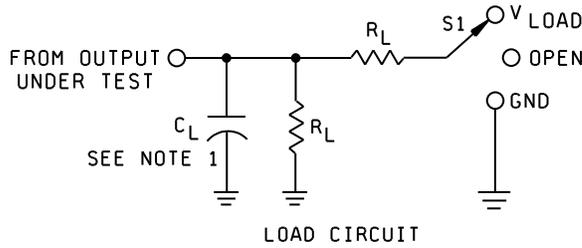
Device type 01

|| This value was obtained with continuous external writes, CLKOFF = 0 and load = 15 pF.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	36	13	6A
7	GND	14	V _{CC}

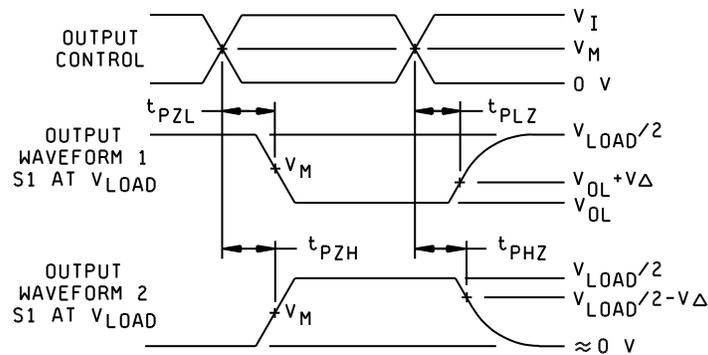
FIGURE 4. Terminal connections.

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TEST	S1
t_{PZL} (SEE NOTE 4 AND 5)	V_{LOAD}
t_{PLZ} (SEE NOTE 4 AND 6)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V \pm 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES:

- C_L includes probe jig and capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- t_{PZL} is measured at V_M .
- t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-side marking
V62/06661-01XA	01295	SN74LVC06AMDREP	LVC06AM

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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