

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-04-23	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	21-11-12	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236  
 HAS CHANGED NAMES TO:  
 DLA LAND AND MARITIME  
 COLUMBUS, OHIO 43218-3990



Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B									
	PAGE	1	2	3	4	5	6	7	8	9										

PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing  YY MM DD  08-05-06	CHECKED BY  Charles F. Saffle	TITLE  MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, DUAL BUFFER GATE, MONOLITHIC SILICON	
	APPROVED BY  Thomas M. Hess		
	SIZE <b>A</b>	CODE IDENT. NO. <b>16236</b>	DWG NO. <b>V62/06659</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual buffer gate microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06659</u>   Drawing number	-	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>E</u>   Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC2G34-EP	Dual buffer gate

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	JEDEC MO-203	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range, (V <sub>CC</sub> ) .....	-0.5 V to +6.5 V
Input voltage range (V <sub>I</sub> ) .....	-0.5 V to +6.5 V <u>2/</u>
Voltage range applied to any output in the high impedance or power-off stage (V <sub>O</sub> ) .....	-0.5 V to +6.5 V <u>2/</u>
Voltage range applied to any output in the high or slow state (V <sub>O</sub> ) .....	-0.5 V to V <sub>CC</sub> + 0.5 V <u>2/ 3/</u>
Input clamp current (I <sub>IK</sub> ) (V <sub>I</sub> < 0) .....	-50 mA
Output clamp current (I <sub>OK</sub> ) (V <sub>O</sub> < 0) .....	-50 mA
Continuous output current (I <sub>O</sub> ) .....	±50 mA
Continuous current through V <sub>CC</sub> or GND .....	±100 mA
Package thermal impedance (θ <sub>JA</sub> ) .....	259°C/W <u>4/</u>
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage (V <sub>CC</sub> ):	
Operating .....	+1.65 V to +5.5 V
Minimum data retention only .....	+1.5 V
Minimum high level input voltage (V <sub>IH</sub> ):	
V <sub>CC</sub> = 1.65 V to 1.95 V .....	0.65 x V <sub>CC</sub>
V <sub>CC</sub> = 2.3 V to 2.7 V .....	+1.7 V
V <sub>CC</sub> = 3.0 to 3.6 V .....	+2.0 V
V <sub>CC</sub> = 4.5 V to 5.5 V .....	0.7 x V <sub>CC</sub>
Maximum low level input voltage (V <sub>IL</sub> ):	
V <sub>CC</sub> = 1.65 V to 1.95 V .....	0.35 x V <sub>CC</sub>
V <sub>CC</sub> = 2.3 V to 2.7 V .....	+0.7 V
V <sub>CC</sub> = 3.0 to 3.6 V .....	+0.8 V
V <sub>CC</sub> = 4.5 V to 5.5 V .....	0.3 x V <sub>CC</sub>
Input voltage (V <sub>I</sub> ) .....	0.0 V to +5.5 V
Output voltage (V <sub>O</sub> ) .....	0.0 V to V <sub>CC</sub>
Maximum high level output current (I <sub>OH</sub> ):	
V <sub>CC</sub> = 1.65 V .....	-4 mA
V <sub>CC</sub> = 2.3 V .....	-8 mA
V <sub>CC</sub> = 3.0 V .....	-16 mA
V <sub>CC</sub> = 3.0 V .....	-24 mA
V <sub>CC</sub> = 4.5 V .....	-24 mA
Maximum low level output current (I <sub>OL</sub> ):	
V <sub>CC</sub> = 1.65 V .....	4 mA
V <sub>CC</sub> = 2.3 V .....	8 mA
V <sub>CC</sub> = 3.0 V .....	16 mA
V <sub>CC</sub> = 3.0 V .....	24 mA
V <sub>CC</sub> = 4.5 V .....	24 mA
Maximum Input transition rise or fall rate (Δt/Δv):	
V <sub>CC</sub> = 1.65 V to 1.95 V, V <sub>CC</sub> = 2.3 V to 2.7 V .....	20 ns/V
V <sub>CC</sub> = 3 V to 3.6 V .....	10 ns/V
V <sub>CC</sub> = 4.5 V to 5.5 V .....	5 ns/V
Operating free air temperature (T <sub>A</sub> ) .....	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input negative-voltage and output voltage ratings may exceeded if the input and output current ratings are observed.
- 3/ The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

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## 2. APPLICABLE DOCUMENTS

### JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

(Copies of these documents are available online at <https://www.jedec.org>.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

### 3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

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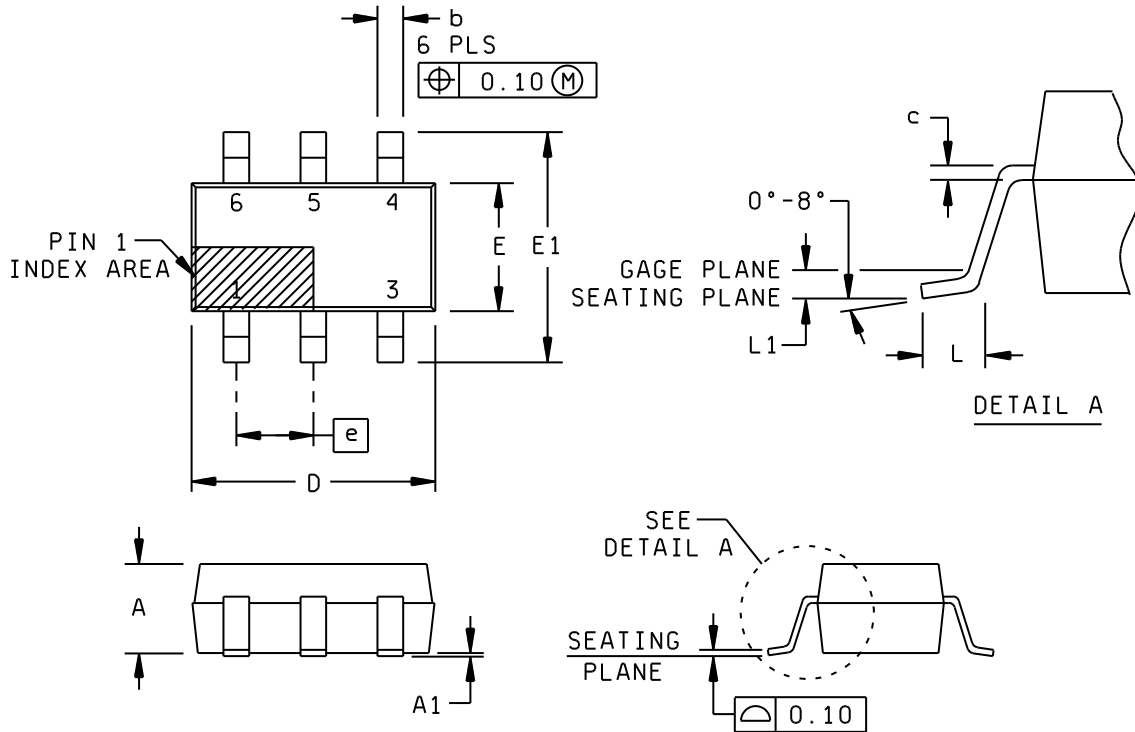
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V <sub>CC</sub>	Temperature, T <sub>A</sub>	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	25°C, -55°C to 125°C	V <sub>CC</sub> - 0.1		V
		I <sub>OH</sub> = -4 mA	1.65 V		1.2		
		I <sub>OH</sub> = -8 mA	2.3 V		1.9		
		I <sub>OH</sub> = -16 mA	3.0 V		2.4		
		I <sub>OH</sub> = -24 mA			2.3		
		I <sub>OH</sub> = -24 mA	4.5 V		3.8		
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
		I <sub>OL</sub> = 16 mA	3.0 V			0.4	
		I <sub>OL</sub> = 24 mA		0.55			
		I <sub>OL</sub> = 24 mA	4.5 V			0.55	
Input current, A inputs	I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0.0 V to 5.5 V			±5	μA
Input/output power-off leakage current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0 V			±10	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND I <sub>O</sub> = 0 A	1.65 V to 5.5 V			10	μA
Quiescent supply current delta	ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3.0 V to 5.5 V			500	μA
Input capacitance	C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	25°C	3.5 TYP		pF
Power dissipation capacitance	C <sub>pd</sub>	f = 10 MHz	1.8 V		14 TYP		
			2.5 V		14 TYP		
			3.3 V		15 TYP		
			5.0 V		17 TYP		
Propagation delay time, A to Y	t <sub>pd</sub>	See figure 5.	1.65 V to 1.95 V	25°C, -55°C to 125°C	3.2	11.5	ns
			2.3 V to 2.7 V		1.5	7.0	
			3.0 V to 3.6 V		1.4	6.1	
			4.5 V to 5.5 V		1.0	5.2	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.80	1.10	0.031	0.043	E	1.10	1.40	0.043	0.055
A1	0.00	0.10	0.00	0.004	E1	1.80	2.40	0.071	0.094
b	0.15	0.30	0.006	0.012	e	0.65 NOM		0.026 NOM	
c	0.08	0.22	0.003	0.009	L	0.26	0.46	0.010	0.018
D	1.85	2.15	0.073	0.085	L1	0.15 NOM		0.006 NOM	

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 mm (0.006 in) per side.
4. Falls within JEDEC MO-203, variation AB.

FIGURE 1. Case outline.

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Case X

Pin No.	Signal name
1	1A
2	GND
3	2A
4	2Y
5	V <sub>cc</sub>
6	1Y

FIGURE 2. Terminal connections.

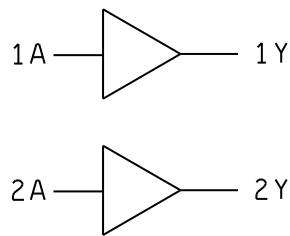


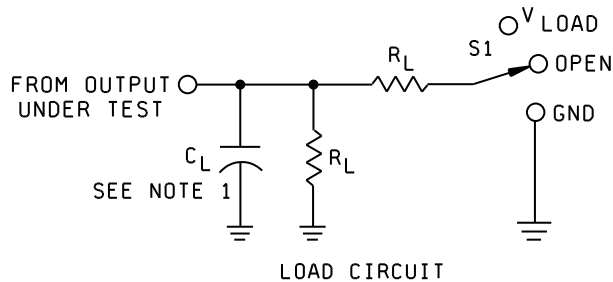
FIGURE 3. Logic diagram.

(each gate)

Input A	Output Y
H	H
L	L

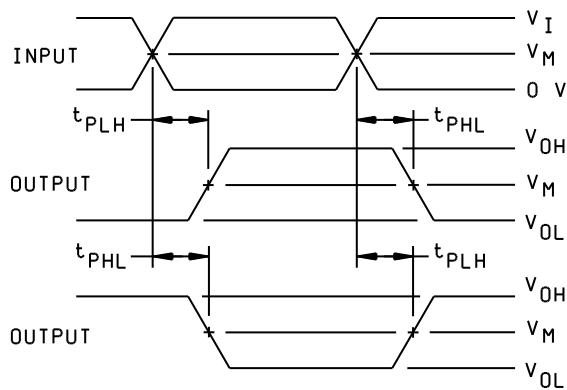
FIGURE 4. Function Table

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06659</b>
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TEST	S1
$t_{PLH}/t_{PHL}$	OPEN

$V_{CC}$	INPUTS		$V_M$	$C_L$	$R_L$
	$V_I$	$t_r/t_f$			
1.8 V $\pm$ 0.15 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	30 pF	1 k $\Omega$
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	30 pF	500 $\Omega$
3.3 V $\pm$ 0.3 V	3 V	$\leq 2.5$ ns	1.5 V	50 pF	500 $\Omega$
5 V $\pm$ 0.5 V	$V_{CC}$	$\leq 2.5$ ns	$V_{CC}/2$	50 pF	500 $\Omega$



Notes:

1.  $C_L$  includes probe and test fixture capacitance.
2. All input pulses are supplied by generators having following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ .
3. The outputs are measured one at a time with one transition per measurement.
4.  $t_{PLH}$  and  $t_{PHL}$  are the same  $t_{pd}$ .

FIGURE 5. Load circuit and voltage waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking <u>2/</u>
V62/06659-01XE	01295	SN74LVC2G34MDCKREP	CAZ

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ The actual top-side marking has one additional character that designates the assembly/test site.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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