REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-03-20	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A							
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 08-03-24	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, OCTAL DUAL SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND THREE-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06658**
	REV **A**	**PAGE** 1 **OF** 13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal dual supply bus transceiver with configurable output voltage and three-state outputs microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06658	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVCC4245A-EP	Octal dual supply bus transceiver with configurable output voltage and three-state outputs.

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range,:
(V_{CCA}) ..... -0.5 V to +6.0 V
(V_{CCB}) ..... -0.5 V to +6.0 V
Input voltage range, (V_I): 2/
I/O ports (A port) ..... -0.5 V to V_{CCA} + 0.5 V
I/O ports (B port) ..... -0.5 V to V_{CCB} + 0.5 V
Except I/O ports ..... -0.5 V to V_{CCA} + 0.5 V
Output voltage range, (V_O): 2/
A port ..... -0.5 V to V_{CCA} + 0.5 V
B port ..... -0.5 V to V_{CCB} + 0.5 V
Input clamp current, (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current, (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current, (I_O) ..... ±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND ..... ±100 mA
Package thermal impedance (θ_{JA}) ..... 88°C/W 3/
Storage temperature range, (T_{STG})..... -65°C to +150°C

1.4 Recommended operating conditions. 4/

		V_{CCA}	V_{CCB}	Min	Max	Unit
Supply voltage,	V_{CCA}			4.5	5.5	V
	V_{CCB}			2.7	5.5	
High level input voltage, (V_{IHA})		4.5 V	2.7 V	2		
			3.6 V	2		
		5.5 V	5.5 V	2		
High level input voltage, (V_{IHB})		4.5 V	2.7 V	2		
			3.6 V	2		
		5.5 V	5.5 V	3.85		
Low level input voltage, (V_{ILA})		4.5 V	2.7 V		0.8	V
			3.6 V		0.8	
		5.5 V	5.5 V		0.8	
Low level input voltage, (V_{ILB})		4.5 V	2.7 V		0.8	
			3.6 V		0.8	
		5.5 V	5.5 V		1.65	

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The value is limited to 6 V maximum.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ All unused inputs of the device must be held at the associated V_{CC} or GND to ensure prope device operation. See manufacturer data for more information available.

1.4 Recommended operating conditions – Continued

	V_{CCA}	V_{CCB}	Min	Max	Unit
High level input voltage (control pins)(referenced to V_{CCA}), (V_{IH})	4.5 V	2.7 V	2		V
		3.6 V	2		
	5.5 V	5.5 V	2		
Low level input voltage (control pins)(referenced to V_{CCA}), (V_{IL})	4.5 V	2.7 V		0.8	
		3.6 V		0.8	
	5.5 V	5.5 V		0.8	
Input voltage, (V_{IA})			0	V_{CCA}	V
Input voltage, (V_{IB})			0	V_{CCB}	
Output voltage, (V_{OA})			0	V_{CCA}	
Output voltage, (V_{OB})			0	V_{CCB}	
High level output current, (I_{OHA})	4.5 V	3 V		-24	mA
High level output current, (I_{OHB})	4.5 V	2.7 V to 4.5 V		-24	
Low level output current, (I_{OLA})	4.5 V	3 V		24	
Low level output current, (I_{OLB})	4.5 V	2.7 V to 4.5 V		24	
Operating free air temperature			-55	+125	°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions unless otherwise specified		V_{CCA}	V_{CCB}	Limits		Unit
							Min	Max	
High level output voltage		V_{OHA}	I_{OH} = -100 µA		4.5 V	3 V	4.4		V
			I_{OH} = -24 mA				3.76		
		V_{OHB}	I_{OH} = -100 µA		4.5 V	3 V	2.9		V
			I_{OH} = -12 mA		4.5 V	2.7 V	2.2		
						3 V	2.46		
			I_{OH} = -24 mA		4.5 V	2.7 V	2.1		
						3 V	2.25		
						4.5 V	3.76		
Low level output voltage		V_{OLA}	I_{OL} = 100 µA		4.5 V	3 V		0.1	V
			I_{OL} = 24 mA					0.44	
		V_{OLB}	I_{OL} = 100 µA		4.5 V	3 V		0.1	
			I_{OL} = 12 mA		4.5 V	2.7 V		0.44	
			I_{OL} = 24 mA		4.5 V	2.7 V		0.5	
						3 V		0.44	
						4.5 V		0.44	
Input current	Control inputs	I_I	$V_I = V_{CCA}$ or GND		5.5 V	3.6 V		±1	µA
						5.5 V		±1	
Off state output current	A or B port	I_{OZ} 2/	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}		5.5 V	3.6 V		±5	µA
Supply current	B to A	I_{CCA}	An = V_{CC} or GND		5.5 V	Open		80	µA
			I_O(A port) = 0, Bn = V_{CCB} or GND		5.5 V	3.6 V		80	
						5.5 V		80	
	A to B	I_{CCB}	An = V_{CCA} or GND, I_O(B port) = 0		5.5 V	3.6 V		50	µA
						5.5 V		80	
Supply current change 3/	A port	ΔI_{CCA}	$V_I = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}		5.5 V	5.5 V		1.5	mA
	$\overline{OE}$		$V_I = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA} or GND		5.5 V	5.5 V		1.5	
	DIR		$V_I = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at V_{CCA} or GND		5.5 V	5.5 V		1.5	
	B port	ΔI_{CCB}	$V_I = V_{CCB}$ – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at GND		5.5 V	3.6 V		0.5	mA
Input capacitance	Control inputs	C_i	$V_I = V_{CCA}$ or GND		Open	Open	5 TYP		pF
I/O Capacitance	A or B port	C_{io}	$V_O = V_{CCA/B}$ or GND		5 V	3.3 V	11 TYP		
Power dissipation capacitance per transceiver		C_{pd}	C_L = 0, f = 10 MHz, T_A = 25°C	Outputs enabled	5 V	3.3 V	20 TYP		
				Outputs disabled			6.5 TYP		

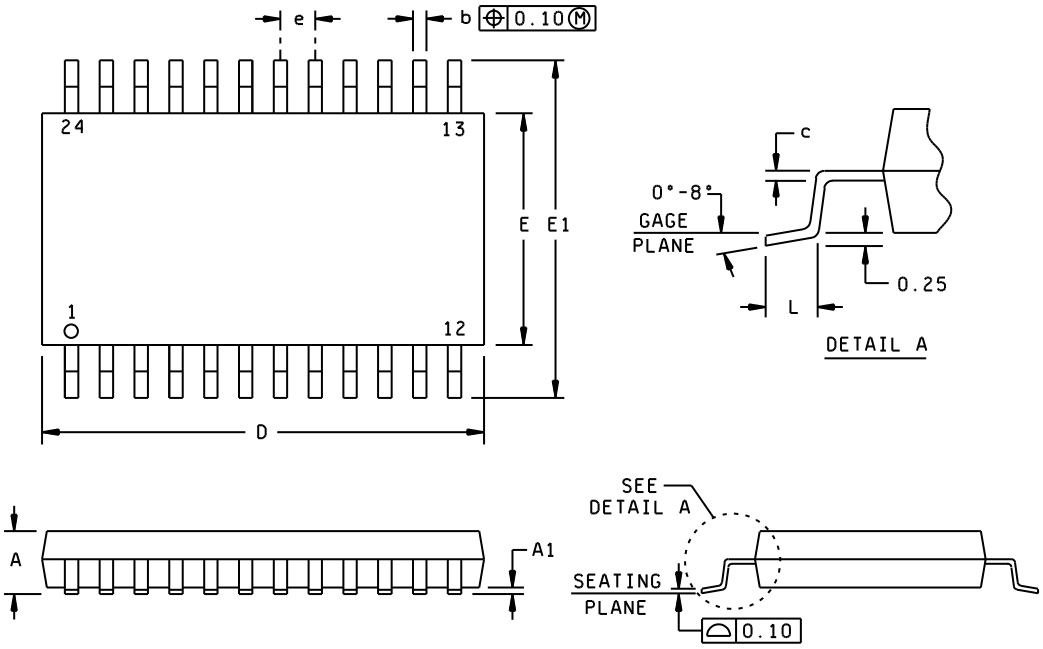
See footnote at end of the table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions unless otherwise specified	V_{CCA} = 5 V ±0.5 V, V_{CCB} = 5 V ±0.5 V		V_{CCA} = 5 V ±0.5 V, V_{CCB} = 2.7 V to 3.6 V		Unit
			Min	Max	Min	Max	
Propagation delay, from input A to output B	t_{PHL}	CL = 50 pF See figure 5	1	7.1	1	7	ns
	t_{PLH}		1	6	1	7	
Propagation delay, from input B to output A	t_{PHL}		1	6.8	1	6.2	
	t_{PLH}		1	6.1	1	5.3	
Enable time, from input $\overline{OE}$ to output A	t_{PZL}		1	9	1	9	
	t_{PZH}		1	8.3	1	8	
Enable time, from input $\overline{OE}$ to output B	t_{PZL}		1	8.2	1	10	
	t_{PZH}		1	8.1	1	10.2	
Disable time, from input $\overline{OE}$ to output A	t_{PLZ}		1	5.5	1	5.9	
	t_{PHZ}		1	5.7	1	5.9	
Disable time, from input $\overline{OE}$ to output B	t_{PLZ}		1	6.4	1	6.4	
	t_{PHZ}		1	7.8	1	8.9	

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.
3. This is the increase in supply current for each input that is one of the specified TTL voltage levels, rathert than 0 V or the associated V_{CC}.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	7.70	7.90			

Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines.

Pin No.	Signal name	Pin No.	Signal name
1	V_{CCA}	13	GND
2	DIR	14	B8
3	A1	15	B7
4	A2	16	B6
5	A3	17	B5
6	A4	18	B4
7	A5	19	B3
8	A6	20	B2
9	A7	21	B1
10	A8	22	$\overline{OE}$
11	GND	23	NC
12	GND	24	V_{CCB}

NC = No internal connection

FIGURE 2. Terminal connections.

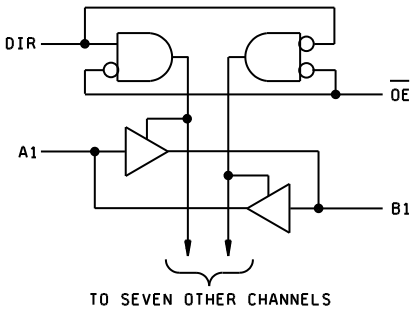
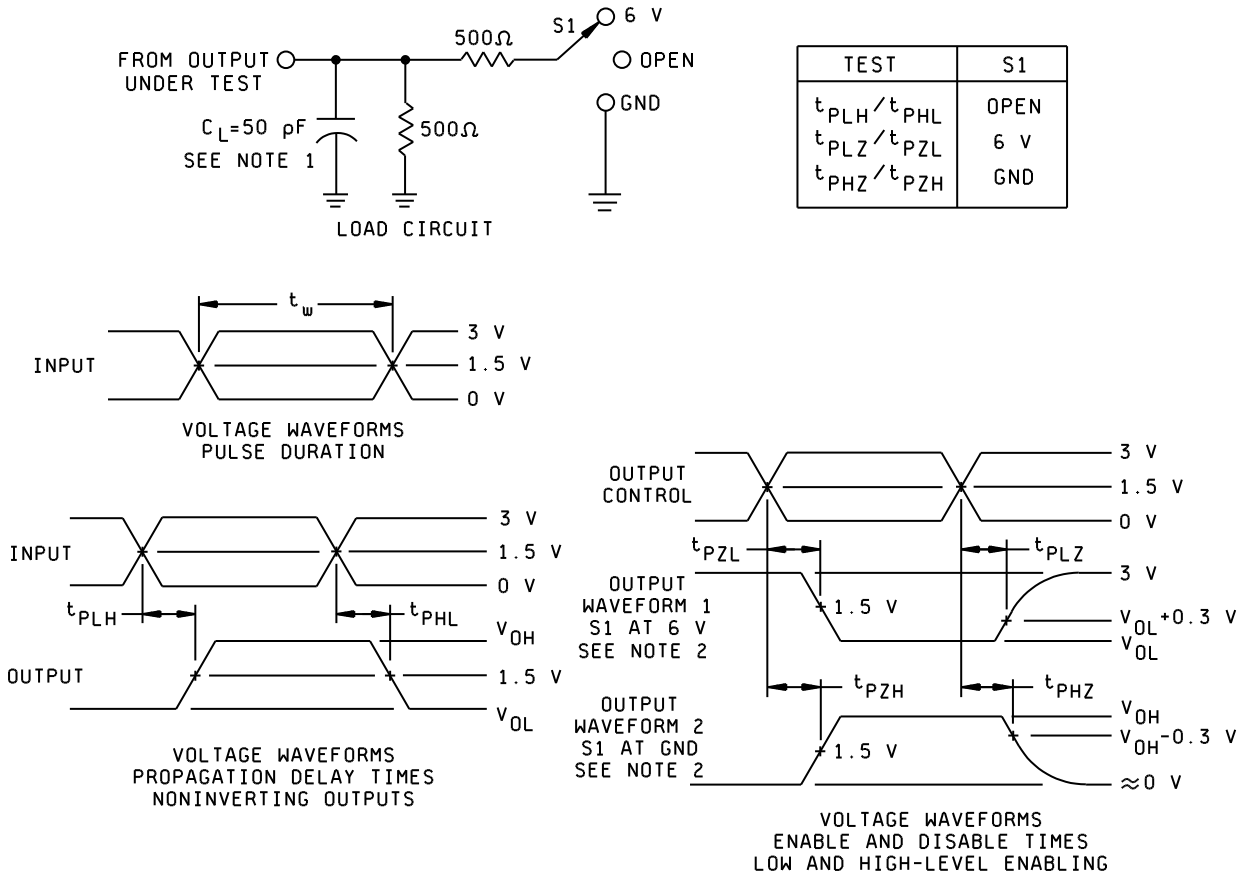


FIGURE 3. Logic diagram.

(Each transceiver)

Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

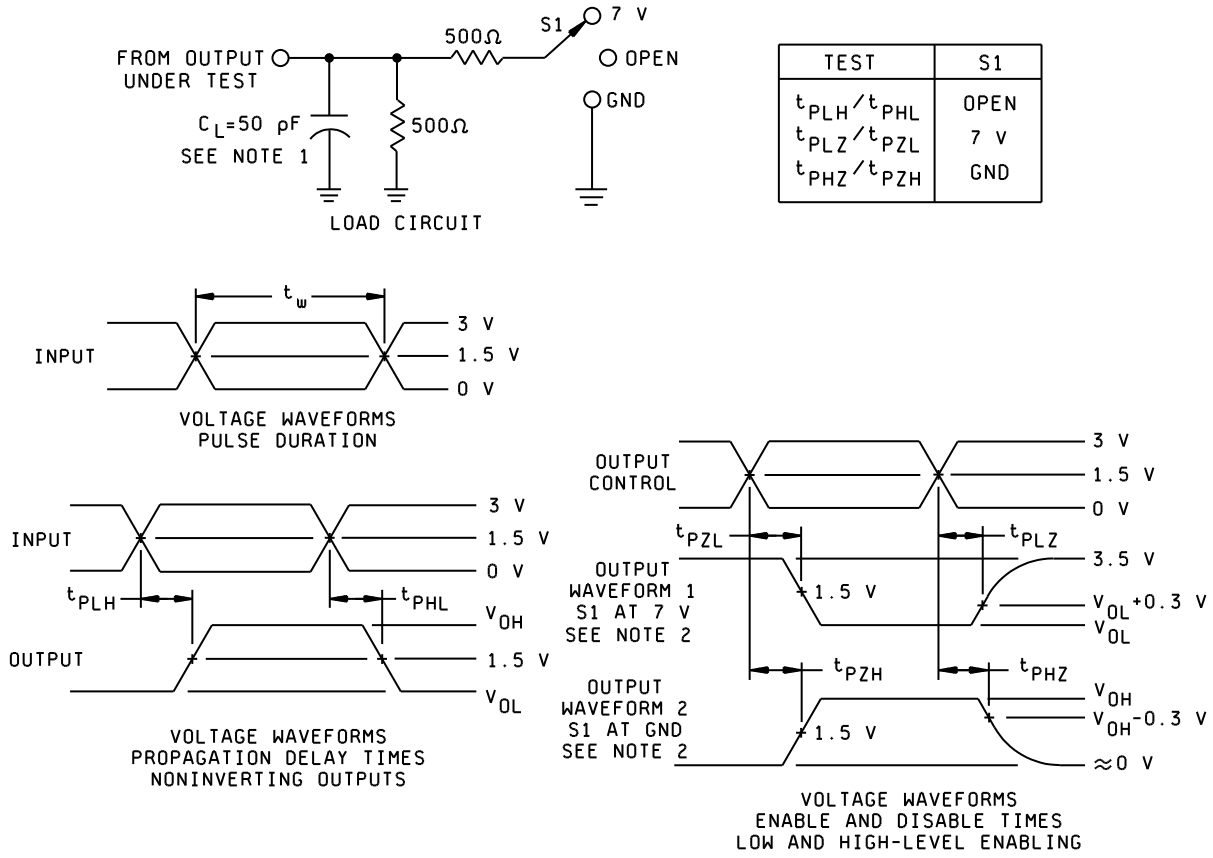
FIGURE 4. Function Table



Parameter measurement information for A to B
V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 V to 3.6 V

Notes:
1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

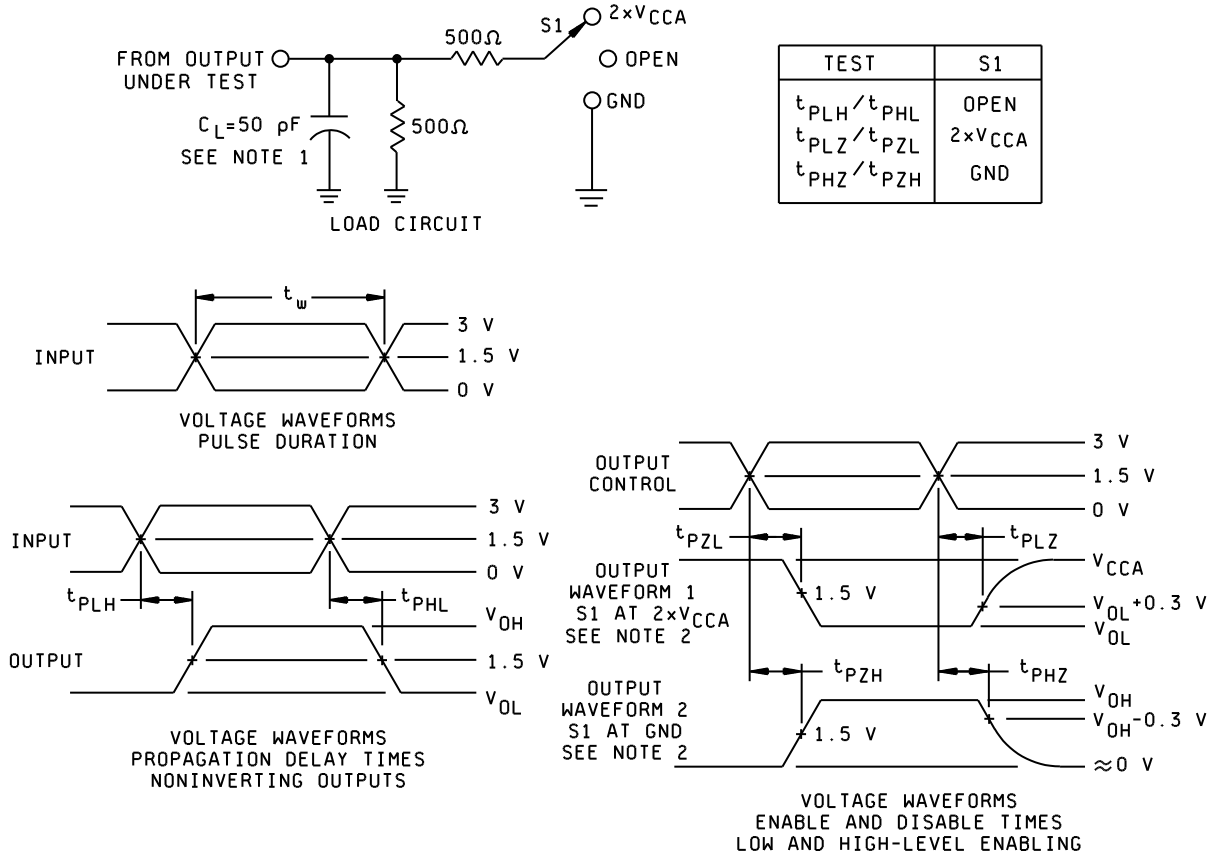
FIGURE 5. Load circuit and voltage waveforms.



Parameter measurement information for A to B
V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 3.6 V to 5.5 V

Notes:
1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

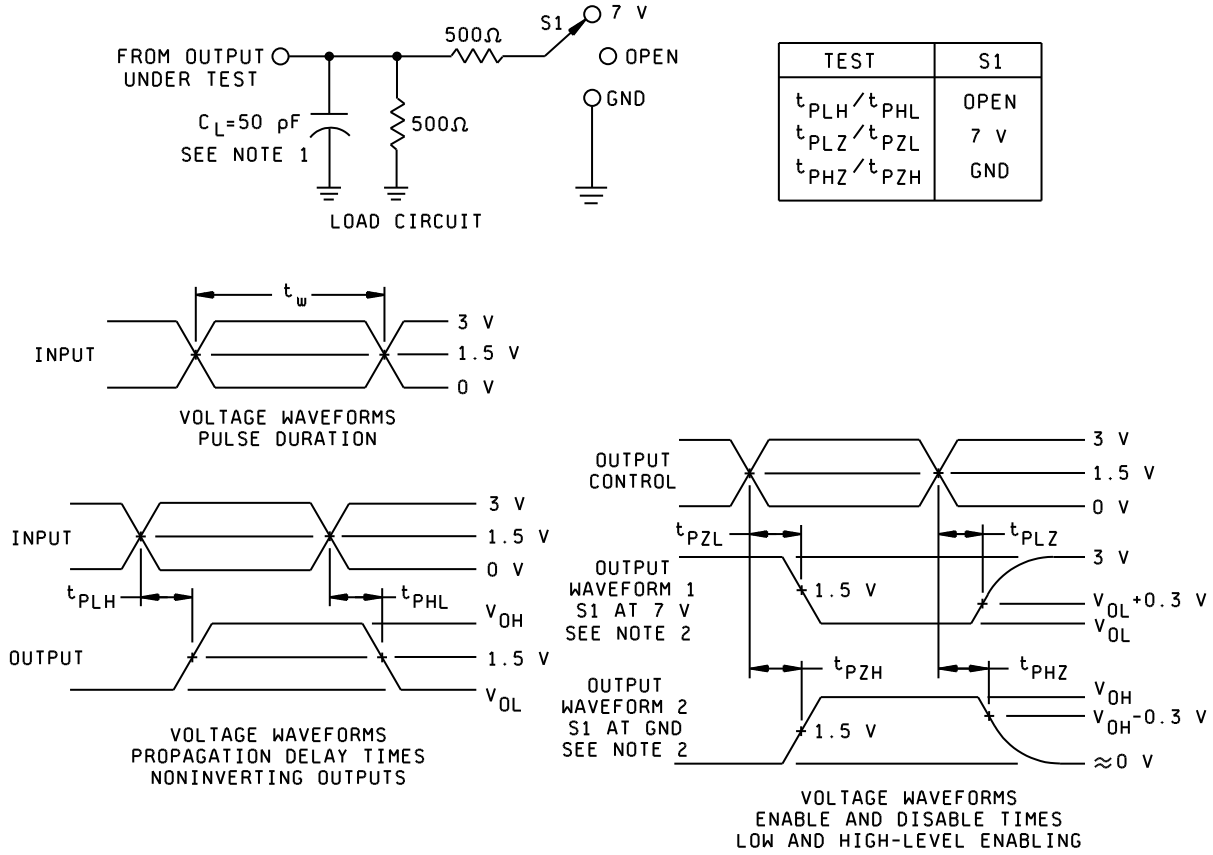
FIGURE 5. Load circuit and voltage waveforms - Continued.



Parameter measurement information for B to A
V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 V to 3.6 V

Notes:
6. C_L includes probe and test fixture capacitance.
7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
8. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
9. The outputs are measured one at a time with one transition per measurement.
10. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms - Continued.



Parameter measurement information for B to A
V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 3.6 V to 5.5 V

Notes:
11. C_L includes probe and test fixture capacitance.
12. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
13. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
14. The outputs are measured one at a time with one transition per measurement.
15. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06658-01XE	01295	CLVCC4245AMPWREP	LG245A-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493