

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single bus buffer gate with 3-state output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06656</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74AUC1G125-EP	Single bus buffer gate with 3-state output.

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-203	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +3.6 V
Input voltage range (V_I)	-0.5 V to +3.6 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to +3.6 V 2/
Output voltage range (V_O)	-0.5 V to $V_{CC} + 0.5$ V 2/
Maximum input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Maximum continuous output current (I_O)	± 20 mA
Maximum continuous current through V_{CC} or GND	± 100 mA
Maximum package thermal impedance (θ_{JA}):	252°C/W 3/
Storage temperature range (T_{STG})	-65°C to 150°C

1.4 Recommended operating conditions. 4/

Supply voltage (V_{CC})	0.8 V to 2.7 V
Minimum high level input voltage	
$V_{CC} = 0.8$ V	V_{CC}
$V_{CC} = 1.1$ V to 1.95 V	0.65 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	1.7 V
Maximum low level input voltage	
$V_{CC} = 0.8$ V	0 V
$V_{CC} = 1.1$ V to 1.95 V	0.35 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	0.7 V
Input voltage (V_I)	0 V to 3.6 V
Output voltage (V_O)	0 to V_{CC}
Maximum high level output current (I_{OH}):	
$V_{CC} = 0.8$ V	-0.7 mA
$V_{CC} = 1.1$ V	-3 mA
$V_{CC} = 1.4$ V	-5 mA
$V_{CC} = 1.65$ V	-8 mA
$V_{CC} = 2.3$ V	-9 mA
Maximum low level output current (I_{OL}):	
$V_{CC} = 0.8$ V	0.7 mA
$V_{CC} = 1.1$ V	3 mA
$V_{CC} = 1.4$ V	5 mA
$V_{CC} = 1.65$ V	8 mA
$V_{CC} = 2.3$ V	9 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$):	
$V_{CC} = 0.8$ V to 1.6 V	20 ns/V
$V_{CC} = 1.65$ V to 1.95 V	10 ns/V
$V_{CC} = 2.3$ V to 2.7 V	3 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figures 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -55°C ≤ T _A ≤ 125°C unless otherwise specified	V _{CC}	Limits		Unit	
				Min	Max		
High level output voltage	V _{OH}	I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} - 0.1		V	
		I _{OH} = -0.7 mA, T _A = 25°C	0.8 V	0.55 Typ			
		I _{OH} = -3 mA	1.1 V	0.8			
		I _{OH} = -5 mA	1.4 V	1			
		I _{OH} = -8 mA	1.65 V	1.2			
		I _{OH} = -9 mA	2.3 V	1.8			
Low level output voltage	V _{OL}	I _{OL} = 100 μA	0.8 V to 2.7 V		0.2	V	
		I _{OL} = 0.7 mA, T _A = 25°C	0.8 V	0.25 Typ			
		I _{OL} = 3 mA	1.1 V		0.3		
		I _{OL} = 5 mA	1.4 V		0.4		
		I _{OL} = 8 mA	1.65 V		0.45		
		I _{OL} = 9 mA	2.3 V		0.6		
Input current	A or \overline{OE} inputs	I _I	V _I = V _{CC} or GND	0 to 2.7 V		±5	μA
Off current		I _{off}	V _I or V _O = 2.7 V	0		±10	μA
Off state output current		I _{oz}	V _O = V _{CC} or GND	2.7 V		±10	μA
Supply current		I _{CC}	V _I = 5.5 V or GND, I _O = 0,	0.8 V to 2.7 V		10	μA
Input capacitance		C _i	V _I = V _{CC} or GND, T _A = 25°C	2.5 V		2.5 Typ	pF
Output capacitance		C _o	V _O = V _{CC} or GND, T _A = 25°C	2.5 V		5.5 Typ	

See footnote at end of table.

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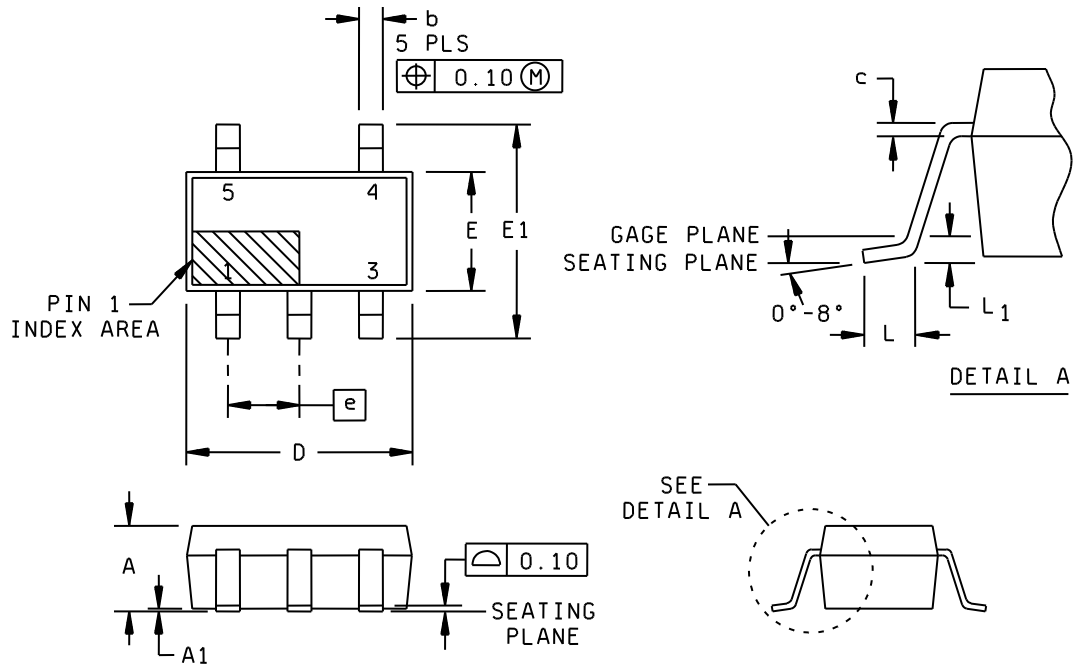
TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions -55°C ≤ T _A ≤ 125°C unless otherwise specified	V _{CC} = 0.8 V		V _{CC} = 1.2 V ±0.1 V		V _{CC} = 1.5 V ±0.1 V		V _{CC} = 1.8 V ±0.15 V		V _{CC} = 2.5 V ±0.2 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Switching characteristics													
Propagation delay from input A to output Y	t _{pd}	See figure 5	4.7 Typ		0.8	7.5	0.4	6	0.7	5.5	0.9	5	ns
Enable time from input \overline{OE} to output Y	t _{en}		5.4 Typ		0.7	7.8	0.5	7	1	6.5	1.1	5	
Disable time from input \overline{OE} to output Y	t _{dis}		4.8 Typ		1.4	8.3	1.4	7	1.8	6.8	0.8	6	
Operating characteristics													
Test	Symbol	Conditions -55°C ≤ T _A ≤ 125°C unless otherwise specified	V _{CC} = 0.8 V		V _{CC} = 1.2 V		V _{CC} = 1.5V		V _{CC} = 1.8 V		V _{CC} = 2.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power dissipation capacitance	Output enabled	f = 10 MHz, T _A = 25°C	14 Typ		14 Typ		14 Typ		15 Typ		16 Typ		pF
	Output disabled		1.5 Typ		1.5 Typ		1.5 Typ		2 Typ		2.5 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 Typ	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15	L1	0.15 Typ	

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm per side.
4. Falls within JEDEC MO-203 variation AB.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol
1	\overline{OE}
2	A
3	GND
4	Y
5	V _{cc}

FIGURE 2. Terminal connections.

Inputs		Output
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

FIGURE 3. Function table.

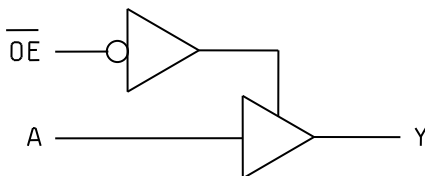
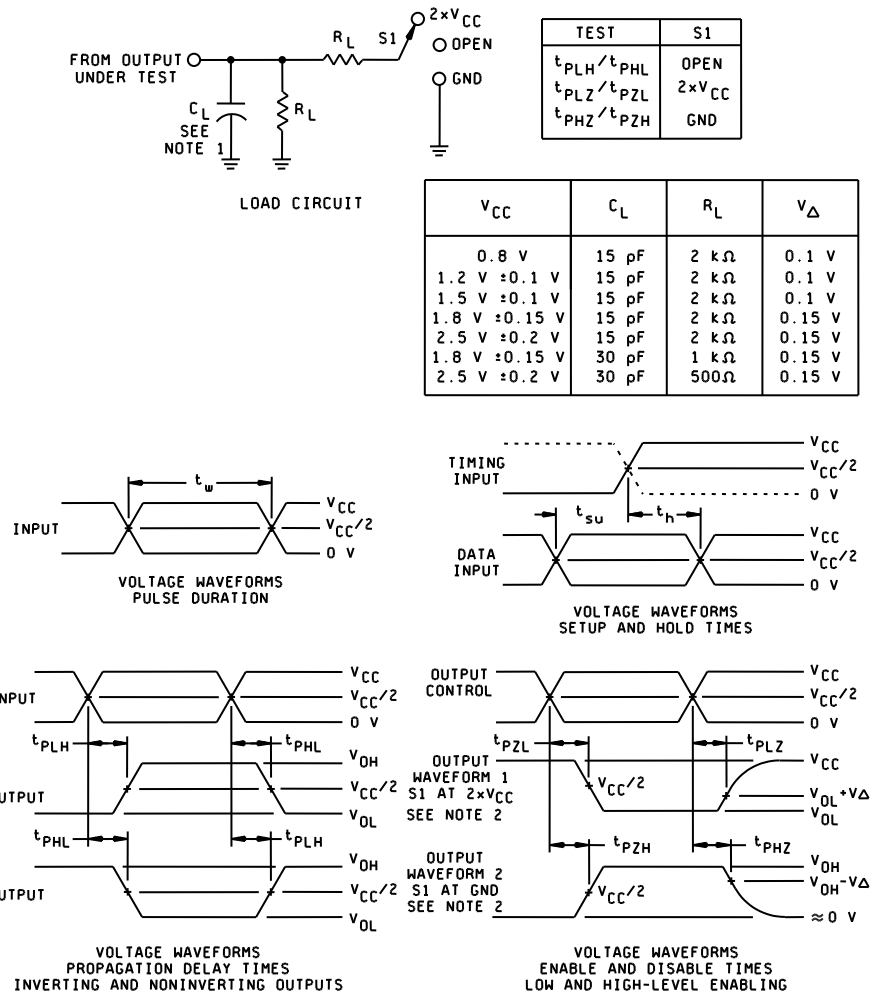


FIGURE 4. Logic diagram.

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NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \geq 1 V/ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PHL} and t_{PLH} are the same as t_{pd} .

FIGURE 5. Load circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side Marking <u>2/</u>
V62/06656-01XE	01295	CAUC1G125MDCKREP	UM

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ The actual topside marking has one additional character that designates the assembly/test site..

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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