REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-03-20	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	21-10-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B										
	PAGE			1	2	3	4	5	6	7	8	9										

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY MM DD 07-04-24	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06655**
	REV **B**	**PAGE** 1 **OF** 9

AMSC N/A

5962-V101-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single inverter buffer/driver with open-drain output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06655	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC1G06-EP	Single inverter buffer/driver with open-drain output

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	MO-203	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +6.5 V
Input voltage range (V_I)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to +6.5 V 2/ 3/
Maximum input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Maximum continuous output current (I_O)	±50 mA
Maximum continuous current through V_{CC} or GND	±100 mA
Maximum package thermal impedance (θ_{JA}): 4/	252°C/W
Storage temperature range (T_{STG})	-65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}):	
Operating	+1.65 V to +5.5 V
Data retention only	+1.5 V minimum
Minimum high level input voltage	
V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	1.7 V
V_{CC} = 3 V to 3.6 V	2.0 V
V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}
Maximum low level input voltage	
V_{CC} = 1.65 V to 1.95 V	0.35 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	0.7 V
V_{CC} = 3 V to 3.6 V	0.8 V
V_{CC} = 4.5 V to 5.5 V	0.3 x V_{CC}
Input voltage (V_I)	0 V to +5.5 V
Output voltage (V_O)	0 V to +5.5 V

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The value of V_{CC} is provided in the recommended operating conditions section.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

1.4 Recommended operating conditions - Continued.

Maximum low level output current (I_{OL}):
- V_{CC} = 1.65 V ..... 4 mA
- V_{CC} = 2.3 V ..... 8 mA
- V_{CC} = 3 V ..... 16 mA
- V_{CC} = 3 V ..... 24 mA
- V_{CC} = 4.5 V ..... 32 mA

Maximum input transition rise or fall rate ($\Delta t/\Delta v$) :
- V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2V ..... 20 ns/V
- V_{CC} = 3.3 V ±0.3 V ..... 10 ns/V
- V_{CC} = 5.0 V ±0.5 V ..... 5 ns/V

Operating free-air temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

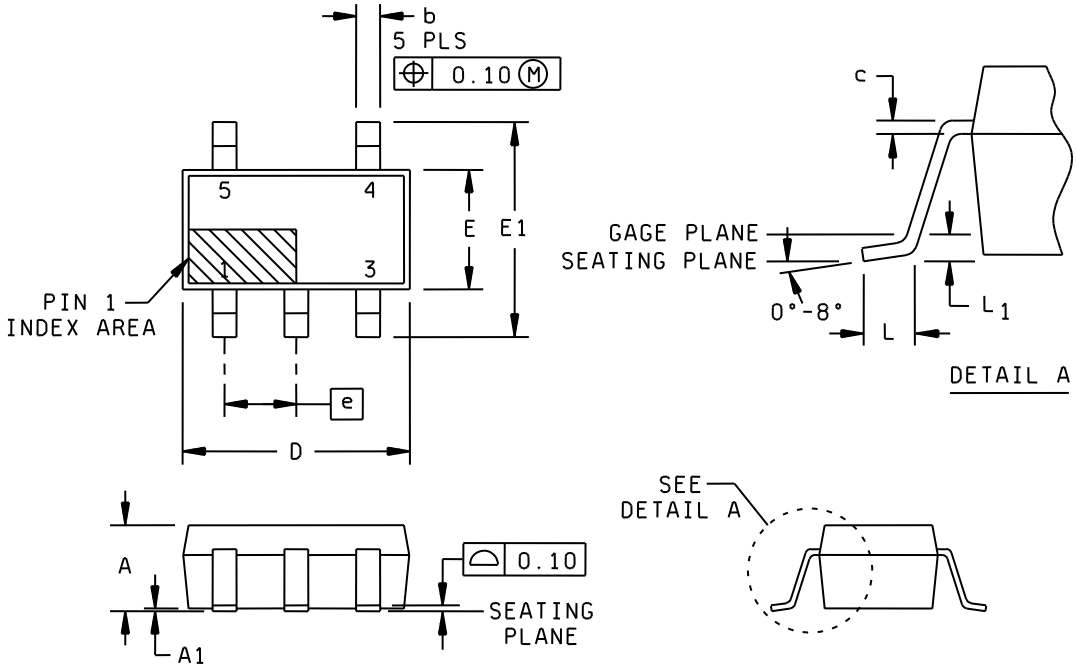
3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figures 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
Low level output voltage	V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V		0.1	V
		I_{OL} = 4 mA	1.65 V		0.45	
		I_{OL} = 8 mA	2.3 V		0.3	
		I_{OL} = 16 mA	3.0 V		0.4	
		I_{OL} = 24 mA			0.55	
		I_{OL} = 32 mA	4.5 V		0.55	
Input current A inputs	I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±1	µA
Off current	I_{off}	V_I or V_O = 5.5 V	0 V		±10	µA
Supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0,	1.65 V to 5.5V		10	µA
Quiescent supply current	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other input at V_{CC} or GND	3.0 V to 5.5V		500	µA
Input capacitance	C_i	V_I = VCC or GND, T_A = 25°C	3.3 V	4 Typ		pF
Output capacitance	C_o	V_O = VCC or GND, T_A = 25°C	3.3 V	5 Typ		
Switching characteristics						
Propagation from input A to output Y	t_{pd}	See figure 5	1.8 V ±0.15 V	2.2	8	ns
			2.5 V ±0.20 V	1.1	6	
			3.3 V ±0.30 V	1.2	6	
			5.0 V ±0.5 V	1.0	5.5	
Operating characteristics						
Power dissipation capacitance	C_{pd}	f = 10 MHz, T_A = 25°C	1.8 V	3 Typ		pF
			2.5 V	3 Typ		
			3.3 V	4 Typ		
			5.0 V	6 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 NOM	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15	L1	0.15 NOM	

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.15 mm per side.
4. Falls within JEDEC MO-203 variation AA.

FIGURE 1. Case outline - Continued.

Case X

Terminal number	Terminal symbol
1	NC
2	A
3	GND
4	Y
5	V_{CC}

NC = Not internal connection

FIGURE 2. Terminal connections.

Input A	Output Y
H	L
L	H

FIGURE 3. Function table.

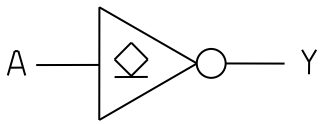
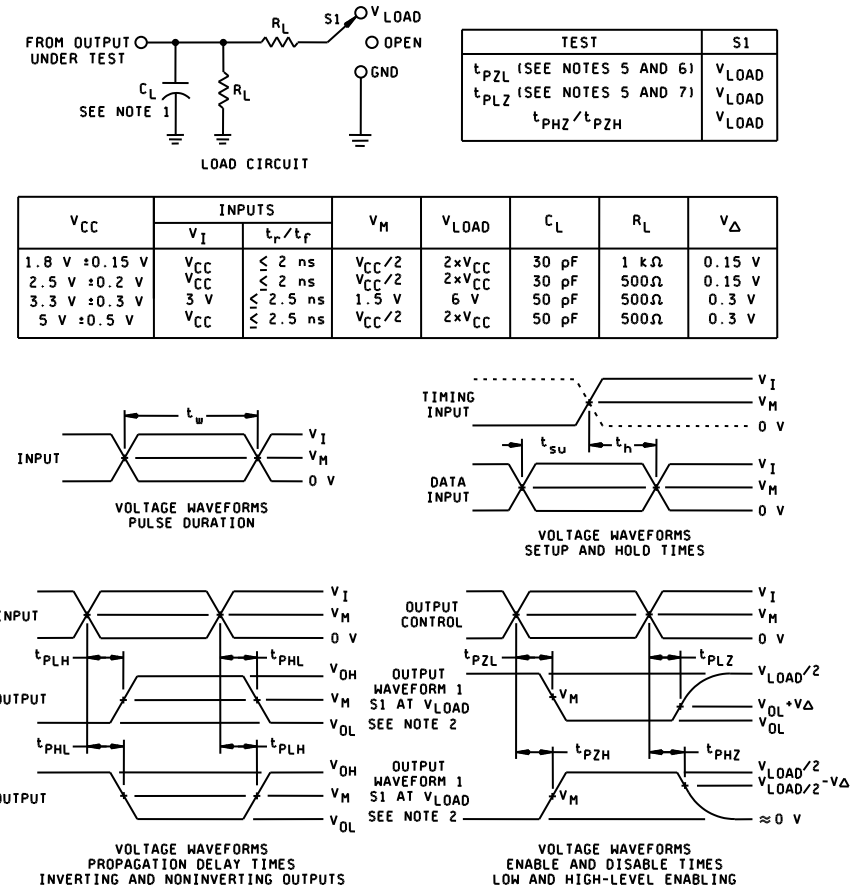


FIGURE 4. Logic diagram.



Open drain

NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. Since this device has open drain outputs, t_{PLZ} and t_{PHZ} are the same as t_{pd}.
6. t_{PZL} is measured at V_M.
7. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking 2/
V62/06655-01XE	3/	SN74LVC1G06MDCKREP	CBA

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The actual top-side marking has one additional character that designates the assembly/test site.
3/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243