

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT 16-bit transparent D-type latch with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06654</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVTH162373-EP	3.3-V ABT 16-bit transparent D-type latch with 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-118	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 4.6 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state (V_O)	-0.5 V to $V_{CC} + 0.5 V$ 2/
Current into any output in the low state (I_O)	30 mA
Current into any output in the high state (I_O)	30 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Package thermal impedance (θ_{JA})	63°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C 5/

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Minimum high level input voltage (V_{IH})	2 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum input voltage (V_I)	5.5 V
Maximum high level output current (I_{OH})	-12 mA
Maximum low level output current (I_{OL})	12 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled)	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$)	200 $\mu s/V$
Operating free-air temperature range (T_A)	-55°C to +125°C

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
 - 5/ Long-term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
 - 6/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IK}	I _I = -18 Ma	2.7 V	25°C, -55°C to +125°C	All		-1.2	V
High level output voltage	V _{OH}	I _{OH} = -12 Ma	3 V			2		V
Low level output voltage	V _{OL}	I _{OL} = 12 Ma	3 V				0.8	V
Input current	I _I	Control inputs V _I = 5.5 V	0 V or 3.6 V				10	μA
		Control inputs V _I = V _{CC} or GND	3.6 V				±1	
		Data inputs, V _I = V _{CC}	3.6 V				1	
		Data inputs, V _I = 0 V	3.6 V				-5	
Input current (hold)	I _{I(hold)}	Data inputs, V _I = 0.8 V	3 V			75		μA
		Data inputs, V _I = 2.0 V	3 V			-75		
3-state output current, high	I _{OZH}	V _O = 3 V	3.6 V				5	μA
3-state output current, low	I _{OZL}	V _O = 0.5 V	3.6 V				-5	μA
3-state output current, power-up	I _{OZPU} 2/	V _O = 0.5 V to 3 V, \overline{OE} = don't care	0 V to 1.5 V				±100	μA
3-state output current, power-down	I _{OZPD} 2/	V _O = 0.5 V to 3 V, \overline{OE} = don't care	1.5 V to 0 V				±100	μA
Quiescent supply current	I _{CC}	Outputs high I _O = 0, V _I = V _{CC} or GND	3.6 V				0.19	mA
		Outputs low I _O = 0, V _I = V _{CC} or GND	3.6 V				5	
		Outputs disabled I _O = 0, V _I = V _{CC} or GND	3.6 V		0.19			
Quiescent supply current delta	ΔI _{CC} 3/	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		0.2	mA		
Input capacitance	C _i	V _I = 3 V or 0 V	3.3 V	25°C	3 TYP		pF	
Output capacitance	C _o	V _O = 3 V or 0 V	3.3 V		9 TYP			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Pulse duration, LE high	t _w	See figure 5.	2.7 V	25°C, -55°C to +125°C	All	3		ns
			3.3 V ±0.3 V			3		
Setup time, data before LE↓	t _{su}	See figure 5.	2.7 V			0.6		ns
			3.3 V ±0.3 V			1.3		
Hold time, data after LE↓	t _h	See figure 5.	2.7 V			1.1		ns
			3.3 V ±0.3 V			1		
Propagation delay time, D to Q	t _{PLH}	C _L = 50 pF See figure 5.	2.7 V				5.7	ns
			3.3 V ±0.3 V			1.8	5	
	2.7 V					4.8		
	3.3 V ±0.3 V		1.8			4.4		
Propagation delay time, LE to Q	t _{PLH}	C _L = 50 pF See figure 5.	2.7 V				6.2	ns
			3.3 V ±0.3 V			2.1	5.4	
	2.7 V			4.7				
	3.3 V ±0.3 V		2.1	4.9				
Propagation delay time, output enable, \overline{OE} to Q	t _{pZH}	C _L = 50 pF See figure 5.	2.7 V		7	ns		
			3.3 V ±0.3 V	1.7	5.6			
	2.7 V			5.9				
	3.3 V ±0.3 V		1.7	5.3				
Propagation delay time, output disable, \overline{OE} to Q	t _{PHZ}	C _L = 50 pF See figure 5.	2.7 V		6.6	ns		
			3.3 V ±0.3 V	2.3	6.3			
	2.7 V			6.4				
	3.3 V ±0.3 V		1	7.4				

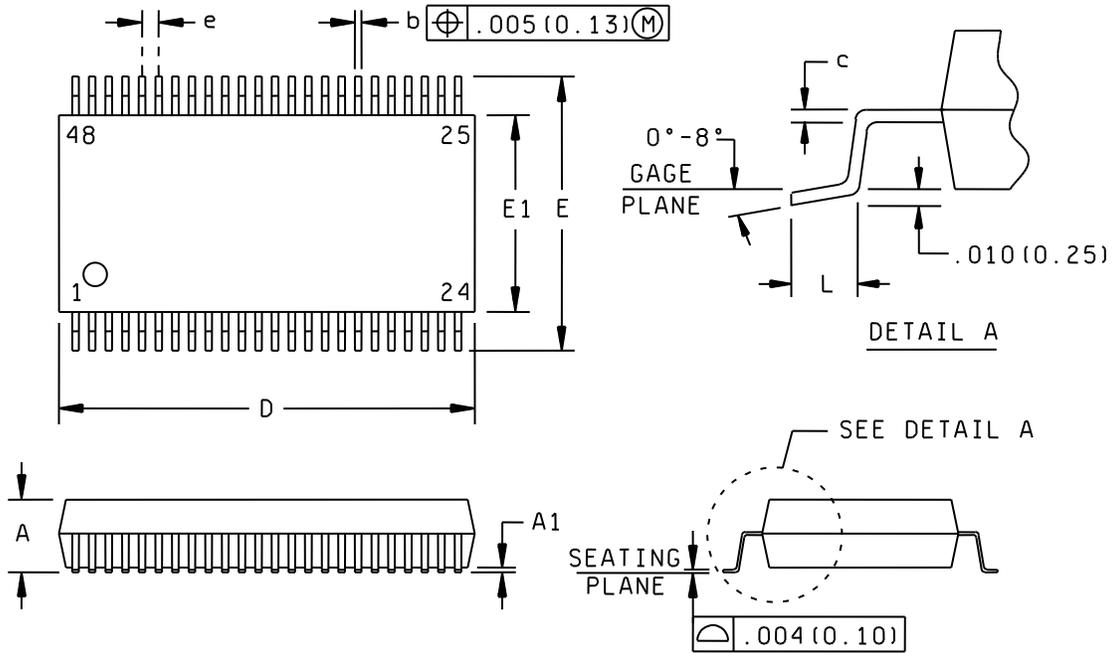
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ On products compliant to MIL-PRF-38535, this parameter is not production tested.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.110	---	2.79	E	0.395	0.420	10.03	10.67
A1	0.008	---	0.20	---	E1	0.291	0.299	7.39	7.59
b	0.008	0.014	0.20	0.34	e	0.025 BSC		0.635 BSC	
c	0.005	0.010	0.13	0.25	L	0.020	0.040	0.51	1.02
D	0.620	0.630	15.75	16.00					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-118.
3. All linear dimensions are in inches (millimeters). Millimeters equivalents are shown for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 millimeters).

FIGURE 1. Case outlines.

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Inputs			Output
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

H = High voltage level
L = Low voltage level
Q₀ = Level of Q before the indicated steady-state input conditions were established.

X = Irrelevant
Z = High Impedance state

FIGURE 2. Truth table.

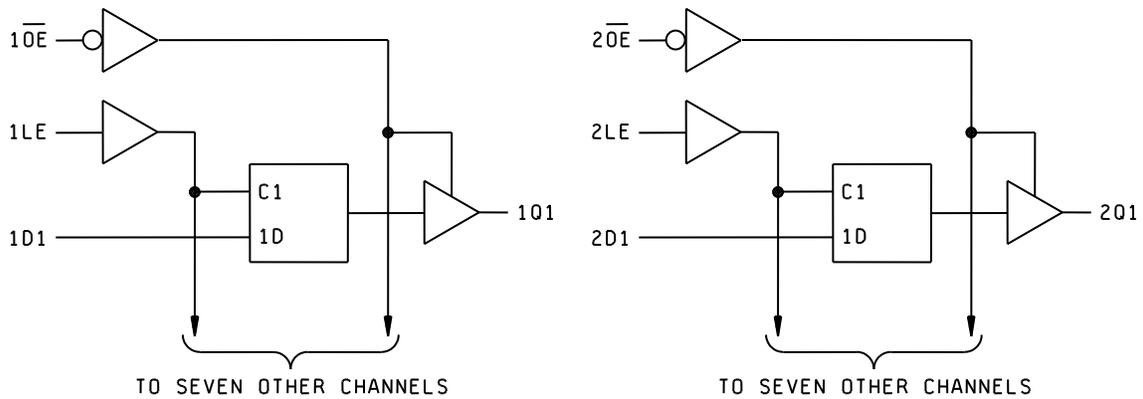


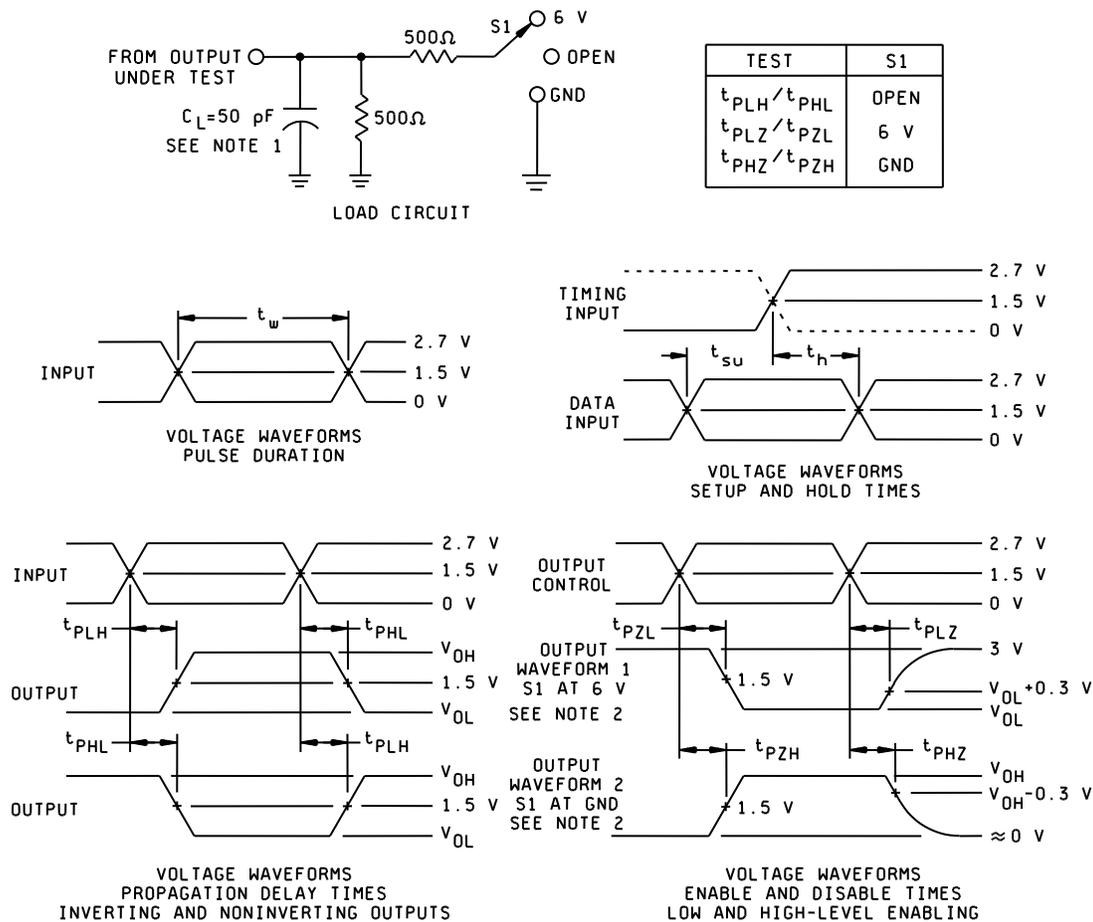
FIGURE 3. Logic diagram.

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Device type 01			
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	10E	25	2LE
2	1Q1	26	2D8
3	1Q2	27	2D7
4	GND	28	GND
5	1Q3	29	2D6
6	1Q4	30	2D5
7	V _{CC}	31	V _{CC}
8	1Q5	32	2D4
9	1Q6	33	2D3
10	GND	34	GND
11	1Q7	35	2D2
12	1Q8	36	2D1
13	2Q1	37	1D8
14	2Q2	38	1D7
15	GND	39	GND
16	2Q3	40	1D6
17	2Q4	41	1D5
18	V _{CC}	42	V _{CC}
19	2Q5	43	1D4
20	2Q6	44	1D3
21	GND	45	GND
22	2Q7	46	1D2
23	2Q8	47	1D1
24	20E	48	1LE

FIGURE 4. Terminal connections.

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NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
4. The outputs are measured one at a time, with one transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-side marking
V62/06654-01XE	01295	CLVTH162373MDLREP	LVTH162373EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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