REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-02-18	Thomas M. Hess
B	Make change to the Output compliance range test as specified under Table I by deleting -0.8 min and replace with -0.5 min. Make change to the Gain drift test as specified under Table I by deleting the words “With external” and replacing with “Without internal”. Make change to the Spurious free dynamic range test as specified under Table I with the condition of IF = 20.1 MHz, delete the words “PLL off”. Make change to the Four tone intermodulation to Nyquist test as specified under Table I by deleting 68 dBc and replacing with 66 dBc. Make change to the High level input voltage test as specified under Table I by deleting 3.3 V max. Update document paragraphs to current requirements. - ro	20-01-29	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-08-22	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 16-BIT 500 MSPS 2X-8X INTERPOLATING DUAL CHANNEL DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06650**
	REV **B**	**PAGE** 1 **OF** 17

AMSC N/A

5962-V125-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit 500 MSPS 2x-8x interpolating dual channel digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06650	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DAC5687-EP	16-bit 500 MSPS 2x-8x interpolating dual channel digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	100	MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:
- (AV_{DD}, $CLKV_{DD}$, IOV_{DD}, $PLLV_{DD}$) ..... -0.5 V to 4.0 V 2/
- (DV_{DD}) ..... -0.5 V to 2.3 V 3/

Voltage between AGND, DGND, CLKGND, PLLGND, and IOGND ..... -0.5 V to 0.5 V

Supply voltage range:
- AV_{DD} to DV_{DD} ..... -0.5 V to 2.6 V
- DA[15..0], DB[15..0], SLEEP, RESETB ..... -0.5 V to IOV_{DD} + 0.5 V 4/
- CLK 1/ 2, CLK 1/2C ..... -0.5 V to $CLKV_{DD}$ + 0.5 V 3/
- LPF ..... -0.5 V to $PLLV_{DD}$ + 0.5 V 4/
- IOUT1, IUOT2 ..... -1.0 V to AV_{DD} + 0.5 V 2/
- EXTIO, BIASJ ..... -0.5 V to AV_{DD} + 0.5 V 2/
- EXTLO ..... -0.5 V to IAV_{DD} + 0.5 V 2/

Peak input current (any input) ..... 20 mA

Peak total input current (all inputs) ..... 30 mA

Operating free-air temperature range (T_A) ..... -55°C to +125°C

Storage temperature range (T_{STG}) ..... -65°C to 150°C

Lead temperature (1.6 mm (1/16 inch) from the case for 10 seconds) ..... 260°C

Junction to ambient thermal conductivity (θ_{JA}): 5/
- Still air ..... 19.88°C/W
- 150 lfm ..... 14.37°C/W

Junction to case thermal conductivity (θ_{JC}) ..... 3.11°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Measured with respect to AGND.

3/ Measured with respect to DGND.

4/ Measured with respect to IOGND.

5/ Airflow or heatsinking reduces θ_{JA} and is highly recommended.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating life derating chart. The operating life derating chart shall be as shown in figure 4.

3.5.5 Timing diagram. The timing diagram shall be as shown in figures 5, 6, 7, 8, and 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
DC Specifications					
Resolution			16		Bits
DC Accuracy 3/					
Integral nonlinearity	INL	1 LSB = $I_{OUTFS}/2^{16}$, T_{MIN} to T_{MAX}	±4 typical		LSB
Differential nonlinearity	DNL	1 LSB = $I_{OUTFS}/2^{16}$, T_{MIN} to T_{MAX}	±5 typical		LSB
Analog output					
Coarse gain linearity		Worst case error from ideal linearity	±0.04 typical		LSB
Fine gain linearity		Worst case error from ideal linearity	±3 typical		LSB
Offset error		Mid code offset	0.01		%FSR
Gain error		Without internal reference	1 typical		%FSR
		With internal reference	0.7 typical		
Gain mismatch		With internal reference, dual DAC, and SSB mode	-2	2	%FSR
Minimum full scale output current 4/			2 typical		mA
Maximum full scale output current 4/			20 typical		mA
Output compliance range 5/		$IOUT_{FS}$ = 20 mA	AV_{DD} -0.5	AV_{DD} +0.5	
Output resistance	R_O		300 typical		kΩ
Output capacitance	C_O		5 typical		pF
Reference Output					
Reference voltage			1.14	1.26	V
Reference output current 6/			100 typical		nA
Reference Input					
Input voltage range	V_{EXTIO}		0.1	1.25	V
Input resistance			1 typical		MΩ
Small signal bandwidth			1.4 typical		MHz
Input capacitance	C_I		100 typical		pF
Temperature Coefficients					
Offset drift			±1 typical		7/
Gain drift		Without internal reference	±15 typical		7/
		With internal reference	±30 typical		
Reference voltage drift			±8 typical		7/

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/		Limits		Unit
				Min	Max	
Power Supply						
Analog supply voltage	AV_{DD}			3.0	3.6	V
Digital supply voltage	DV_{DD}			1.71	2.15	V
Clock supply voltage	$CLKV_{DD}$			3.0	3.6	V
I/O supply voltage	IOV_{DD}			1.71	3.6	V
PLL supply voltage	$PLLV_{DD}$			3.0	3.6	V
DC SPECIFICATION						
Analog supply current	I_{AVDD}	Mode 5 8/		41 typical		mA
		Mode 6 8/		80 typical		
Digital supply current 8/	I_{DVDD}	Mode 6 8/		587 typical		mA
Clock supply current 8/	I_{CLKVDD}	Mode 6 8/		5 typical		mA
PLL supply current 8/	I_{PLLVDD}	Mode 6 8/		20 typical		mA
IO supply current 8/	I_{IOVDD}	Mode 6 8/		2 typical		mA
Sleep mode AV_{DD} supply current	I_{AVDD}	Sleep mode (sleep pin high), CLK2 = 500 MHzx		1 typical		mA
Sleep mode DV_{DD} supply current	I_{DVDD}			2 typical		mA
Sleep mode $CLKV_{DD}$ supply current	I_{CLKVDD}			0.25 typical		mA
Sleep mode PLV_{DD} supply current	I_{PLLVDD}			0.6 typical		mA
Sleep mode IOV_{DD} supply current	I_{IOVDD}			0.6 typical		mA
Power dissipation	P_D	Mode 1 9/	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V	750 typical		mW
		Mode 2 9/		910 typical		
		Mode 3 9/		760 typical		
		Mode 4 9/		1250 typical		
		Mode 5 9/		1250 typical		
		Mode 6 9/		1410 typical		
		Mode 7 9/			1750	
		Sleep mode (sleep pin high), CLK2 = 500 MHzx			20	
Analog power supply rejection ratio	APSRR			-0.2	0.2	%FSR/V
Digital power supply rejection ratio	DPSRR			-0.2	0.2	%FSR/V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 10/ 11/	Limits		Unit
			Min	Max	
AC SPECIFICATIONS					
Analog Output					
Maximum output update rate	f_{clk}		500		MSPS
Output settling time to 0.1%	$t_{s(DAC)}$	Transition: Code 0x0000 to 0xFFFF	10.4 typical		ns
Output propagation delay	t_{pd}		3 typical		ns
Output rise time 10% to 90%	$t_{r(IOUT)}$		2 typical		ns
Output fall time 90% to 10%	$t_{f(IOUT)}$		2 typical		ns
AC performance					
Spurious free dynamic range 12/	SFDR	X2, PLL off, CLK2 = 250 MHz, DAC A and DAC B on, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$	78 typical		dBc
		X4, PLL off, CLK2 = 500 MHz, DAC A and DAC B on, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$	77 typical		
		X4, CLK2 = 500 MHz, DAC A and DAC B on, IF = 20.1 MHz, PLL on for Min, PLL off for TYP, First Nyquist Zone < $f_{DATA}/2$	68 13/		
Signal to noise ration	SNR	X4, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, Single tone, 0 dbFS, IF = 20.1 MHz	73 typical		dBc
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 70.1 MHz	65 typical		
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, Single tone, 0 dbFS, IF = 150.1 MHz	57 typical		
		X4 FMIX CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, Single tone, 0 dbFS, IF = 180.1 MHz	54 typical		
		X4, PLL off, CLK2 = 500 MSPS,DAC A and DAC B on, Four tone, each -12 dbFS, IF = 24.7, 24.9, 25.1, 25.3 MHz	73 typical		
Third order two tone intermodulation (each tone at -6 dBFS)	IMD3	X4, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 20.1 and 21.1 MHz	79 typical		dBc
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 70.1 and 71.1 MHz	73 typical		
		X4 CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 150.1 and 151.1 MHz	68 typical		
		X4 FMIX CMIX, PLL off, CLK2 = 500 MSPS, DAC A and DAC B on, IF = 180.1 and 181.1MHz	67 typical		
Four tone intermodulation to Nyquist (each tone at -12 dBFS)	IMD	X4 CMIX, CLK2 = 500 MHz, f_{OUT} = 149.2, 149.6, 150.4, and 150.8 MHz	66 typical		dBc

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 10/	Limits		Unit
			Min	Max	
AC SPECIFICATIONS					
AC performance – continued					
Adjacent channel leakage ratio	ACLR 14/	Single carrier, baseband, X4, PLL clock mode, CLK1 = 122.88 MHz	78.4 typical		dBc
		Single carrier, baseband, X4, PLL clock mode, CLK2 = 491.52 MHz	78.5 typical		
		Single carrier, IF = 153.6 MHz, X4 CMIX, External clock mode, CLK2 = 491.52 MHz	70.9 typical		
		Two carrier, , IF = 153.6 MHz, X4 CMIX, External clock mode, CLK2 = 491.52 MHz	67.8 typical		
		Four carrier, baseband, X4, External clock mode, CLK2 = 491.52 MHz	76.1 typical		
		Four carrier, IF = 92.16 MHz, X4L, External clock mode, CLK2 = 491.52 MHz	66.8 typical		
		Single carrier, IF = 153.6 MHz, X4 CMIX, External clock mode, CLK2 = 491.52 MHz, DV_{DD} = 2.1 V	72.2 typical		
		Two carrier, IF = 153.6 MHz, X4 CMIX, External clock mode, CLK2 = 491.52 MHz, DV_{DD} = 2.1 V	69.3 typical		
		Four carrier, baseband, X4, External clock mode, CLK2 = 491.52 MHz, DV_{DD} = 2.1 V	68.5 typical		
		Four carrier, IF = 92.16 MHz, X4L, External clock mode, CLK2 = 491.52 MHz, DV_{DD} = 2.1 V	66.3 typical		
Noise floor		50 MHz offset, 1 MHz BW, Single carrier, baseband, X4, External clock mode, CLK1 = 122.88 MHz	92 typical		dBc
		50 MHz offset, 1 MHz BW, Four carrier, baseband, X4, External clock mode, CLK1 = 122.88 MHz	81 typical		
		50 MHz offset, 1 MHz BW, Single carrier, baseband, X4, PLL clock mode, CLK2 = 491.52 MHz	88 typical		
		50 MHz offset, 1 MHz BW, Four carrier, baseband, X4, PLL clock mode, CLK2 = 491.52 MHz	81 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
CMOS interface					
High level input voltage	V_{IH}		2		V
Low level input voltage	V_{IL}		0	0.8	V
High level input current	I_{IH}		-40	40	µA
Low level input current	I_{IL}		-40	40	µA
Input capacitance			5 typical		pF
High level output voltage: PLLLOCK, SDO, SDIO	V_{OH}	I_{load} = -100 µA	IOV_{DD} – 0.2		V
		I_{load} = -8 mA	0.8 x IOV_{DD}		
Low level output voltage: PLLLOCK, SDO, SDIO	V_{OL}	I_{load} = -100 µA		0.2	V
		I_{load} = -8 mA		0.22 x IOV_{DD}	
Input data rate		External or dual clock modes	16	250	MSPS
		PLL clock mode	16	160	
PLL					
Phase noise		At 600 kHz offset, measured at DAC output, 25 MHz 0 dBFS tone, f_{DATA} = 125 MSPS, 4x interpolation, pll_freq = 1, pll_kv = 0	133 typical		dBc/Hz
		At 6 MHz offset, measured at DAC output, 25 MHz 0 dBFS tone, f_{DATA} = 125 MSPS, 4x interpolation, pll_freq = 1, pll_kv = 0	148.5 typical		
VCO maximum frequency		pll_fre = 0, pll_kv = 0	370		MHz
		pll_fre = 0, pll_kv = 1	480		
		pll_fre = 1, pll_kv = 0	495		
		pll_fre = 1, pll_kv = 1	520		
VCO minimum frequency		pll_fre = 0, pll_kv = 0		225	MHz
		pll_fre = 0, pll_kv = 1		200	
		pll_fre = 1, pll_kv = 0		480	
		pll_fre = 1, pll_kv = 1		480	
NCO and QMC blocks					
QMC clock rate				320	MHz
NCO clock rate				320	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Serial port timing					
Setup time, SDENB to rising edge of SCLK	$t_{s(SDENB)}$		20		ns
Setup time, SDIO valid to rising edge of SCLK	$t_{s(SDIO)}$		10		ns
Hold time, SDIO valid to rising edge of SCLK	$t_{h(SDIO)}$		5		ns
Period of SCLK	t_{SCLK}		100		ns
High time of SCLK	t_{SCLKH}		40		ns
Low time of SCLK	t_{SCLKL}		40		ns
Data output after falling edge of SCLK	$t_{d(DATA)}$		10 typical		ns
Clock input (CLK1/CLK1C, CLK2/CLK2C)					
Duty cycle			50% typical		
Differential voltage			0.5 typical		V
Timing parallel data input: CLK1 latching modes, PLL mode –See figure 5, Dual clock mode disabled-see figure 6, Dual clock mode with FIFO enabled – See figure 7)					
Setup time, DATA valid to rising edge of CLK1	$t_{s(DATA)}$		0.5		ns
Hold time, DATA valid after rising edge of CLK1	$t_{h(DATA)}$		1.5		ns
Maximum offset between CLK1 and CLK2 rising edges – Dual Clock mode with FIFO disabled	t_align		15/		ns
Timing parallel data input(External clock mode, Latch on PLLLock rising edge, CLK2 clock input, - See figure 8)					
Setup time, DATA valid to rising edge of PLLLOCK	$t_{s(DATA)}$	72 Ω load to PLLLOCK	0.5		ns
Hold time, DATA valid to rising edge of PLLLOCK	$t_{h(DATA)}$	72 Ω load to PLLLOCK	1.5		ns
Delay from CLK2 rising edge to PLLOCK rising edge	t_{delay} (Pllock)	72 Ω load to PLLLOCK. Note that PLLLOCK delay increases with a lower impedance load	4.5 typical		ns
Timing parallel data input(External clock mode, Latch on PLLLock falling edge, CLK2 clock input, - See figure 9)					
Setup time, DATA valid to falling edge of PLLLOCK	$t_{s(DATA)}$	High impedance load on PLLLOCK	0.5 typical		ns
Hold time, DATA valid to falling edge of PLLLOCK	$t_{h(DATA)}$	High impedance load on PLLLOCK	1.5 typical		ns
Delay from CLK2 rising edge to PLLOCK rising edge	t_{delay} (Pllock)	High impedance load on PLLLOCK. Note that PLLLOCK delay increases with a lower impedance load	4.5 typical		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating free air temperature range, AV_{DD} = $CLKV_{DD}$ = $PLLV_{DD}$ = IOV_{DD} = 3.3 V,DV_{DD} = 1.8 V, I_{OUTFS} = 19.2 mA, (unless otherwise noted)

3/ Measured differential across IOUTA1 and IOUTA2 or IUOTB1 and IOUTB2 with 25 Ω each to AV_{DD}.

4/ Nominal full scale current, I_{OUTFS}, equal 32x the I_{BIAS} current.

5/ The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

6/ Use an external buffet amplifier with high impedance input to drive any external load.

7/ ppm of FSR/°C

8/ MODE 1 – MODE 7:
- a. Mode 1: X2, PLL off, CLK2 = 320 MHz, DACA and DACB on, IF = 5 MHz.
- b. Mode 2: X4 QMC, PLL on,CLK1 = 125 MHz, DACA and DACB on, IF = 5 MHz.
- c. Mode 3: X4 CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz.
- d. Mode 4: X4L FMIX CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz.
- e. Mode 5: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA off and DACB on, IF = 150 MHz.
- f. Mode 6: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA on and DACB on, IF = 150 MHz.
- g. Mode 7: X8 FMIX CMIX, PLL on, CLK1 = 62.5 MHz, DACA and DACB on, IF = 150 MHz

9/ MODE 1 – MODE 7:
- h. Mode 1: X2, PLL off, CLK2 = 320 MHz, DACA and DACB on, IF = 5 MHz.
- i. Mode 2: X4 QMC, PLL on,CLK1 = 125 MHz, DACA and DACB on, IF = 5 MHz.
- j. Mode 3: X4 CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz.
- k. Mode 4: X4L FMIX CMIX, PLL off, CLK2 = 500 MHz, DACA off and DACB on, IF = 150 MHz.
- l. Mode 5: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA off and DACB on, IF = 150 MHz.
- m. Mode 6: X4L FMIX CMIX, PLL on, CLK1 = 125 MHz, DACA on and DACB on, IF = 150 MHz.
- n. Mode 7: X8 FMIX CMIX, PLL on, CLK1 = 62.5 MHz, DACA and DACB on, IF = 150 MHz

10/ Over operating free air temperature range, AV_{DD} = $CLKV_{DD}$ = IOV_{DD} = 3.3 V, PLV_{DD} = 0 V (=3.3 V for PLL clock mode), DV_{DD} = 1.8 V, I_{OUTFS} = 19.2 mA, External clock mode, 4:1 transformer output termination, 50 Ω doubly terminated load (unless otherwise noted).

11/ Measured single ended into 50 Ω load.

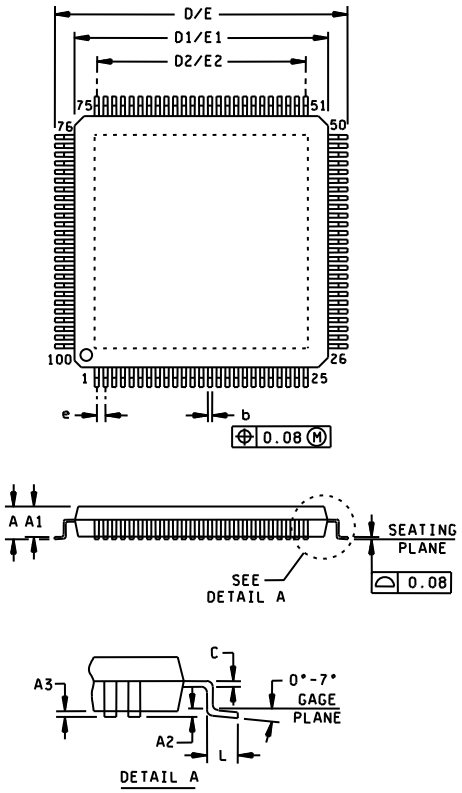
12/ See the Non Harmonic Clock related Spurious Signals from manufacturer data for information on spurious products out of band (<f_{DATA}/2).

13/ 1:1 transformer output termination.

14/ W-CDMA with 38.4 MHz BW, 5 MHz spacing, centered at IF. TESTMODEL 1, 10 ms.

15/ $\frac{1}{2F_{CLK2}}$ - 0.5 ns

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	15.80	16.20
A1	0.95	1.05	D1/E1	13.80	14.20
A2	0.25 TYP		D2/E2	12.00 TYP	
A3	0.05	0.15	e	0.50 NOM	
b	0.17	0.27	L	0.45	0.75
c	0.13 NOM				

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. See manufacturer data for more information.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	26	DVDD	51	DA4	76	DB5
2	AVDD	27	DGND	52	DA3	77	DB6
3	AVDD	28	SDENB	53	DA2	78	DB7
4	AGND	29	SCLK	54	DA1	79	IOGND
5	IUOTB1	30	SDIO	55	DA0(LSB or MSB)	80	IOVDD
6	IOUTB2	31	SDO	56	DVDD	81	DGND
7	AGND	32	DVDD	57	DGND	82	DVDD
8	AVDD	33	TXENABLE	58	CLKGND	83	DB8
9	AGND	34	DA15(MSB or LSB)	59	CLK1	84	DB9
10	AVDD	35	DA14	60	CLK1C	85	DB10
11	EXTIO	36	DA13	61	CLKVDD	86	DB11
12	AGND	37	DVDD	62	CLK2	87	DB12
13	BIASJ	38	DGND	63	CLK2C	88	DGND
14	AVDD	39	DA12	64	CLKGND	89	DVDD
15	EXTLO	40	DA11	65	PLLGND	90	DB13
16	AVDD	41	DA10	66	LPF	91	DB14
17	AGND	42	DA9	67	PLLVDD	92	DB15(MSB or LSB)
18	AVDD	43	DA8	68	DVDD	93	DGND
19	AGND	44	DVDD	69	DGND	94	PHSTR
20	IUOTA2	45	DGND	70	PLLCLOCK	95	RESETB
21	IOUTA1	46	IOVDD	71	DB0(LSB or MSB)	96	SLEEP
22	AGND	47	IOGND	72	DB1	97	TESTMODE
23	AVDD	48	DA7	73	DB2	98	QFLAG
24	AVDD	49	DA6	74	DB3	99	DGND
25	AGND	50	DA5	75	DB4	100	DVDD

FIGURE 2. Terminal connections.

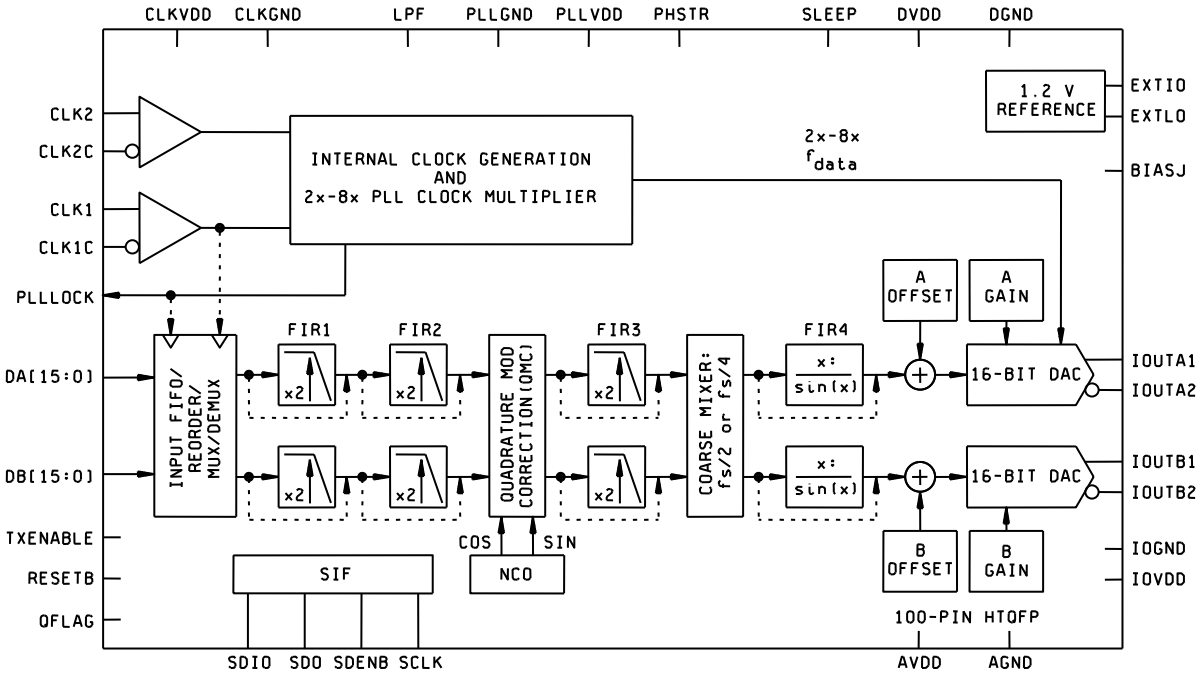


FIGURE 3. Functional block diagram.

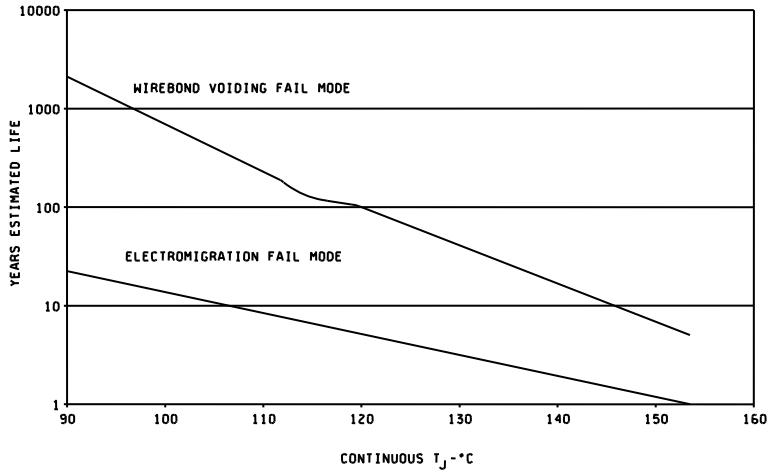


FIGURE 4. Operating life derating chart.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/06650
		REV B	PAGE 14

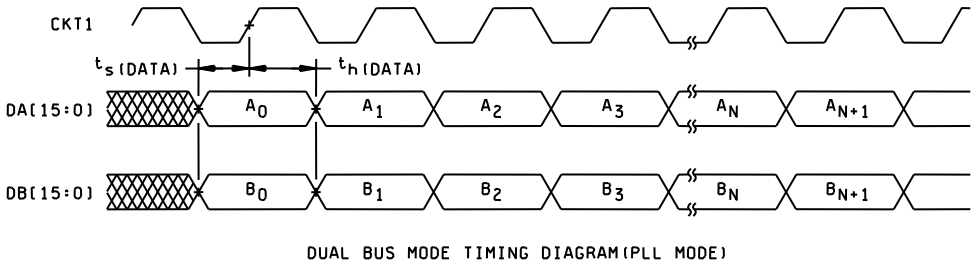


FIGURE 5. Timing diagram.

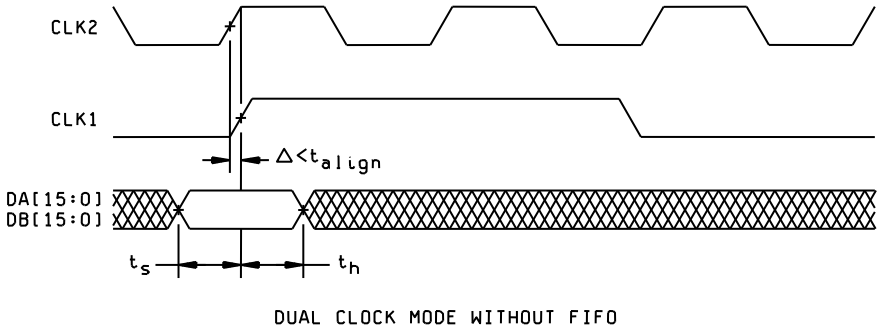


FIGURE 6. Timing diagram.

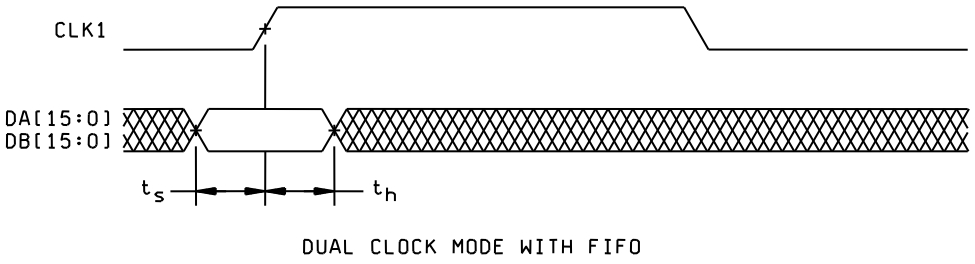


FIGURE 7. Timing diagram.

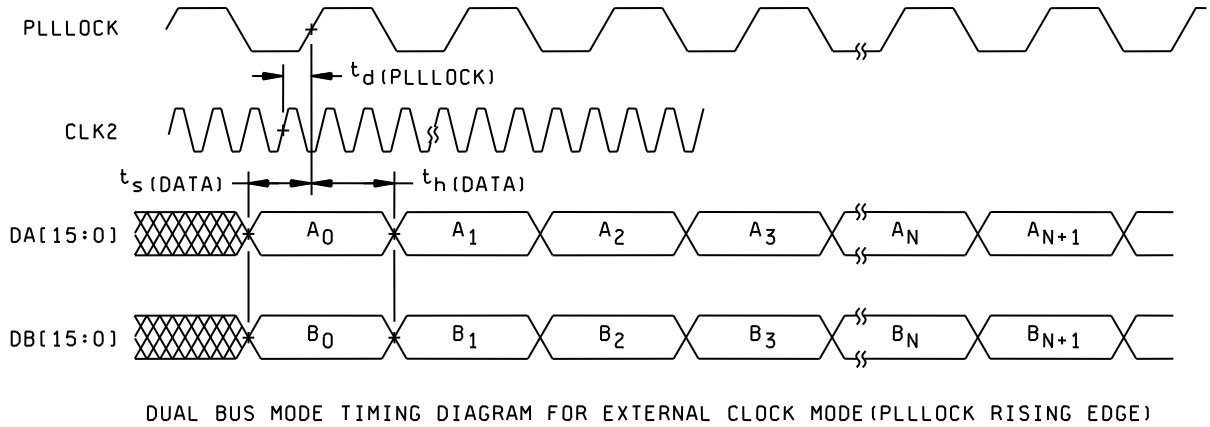


FIGURE 8. Timing diagram.

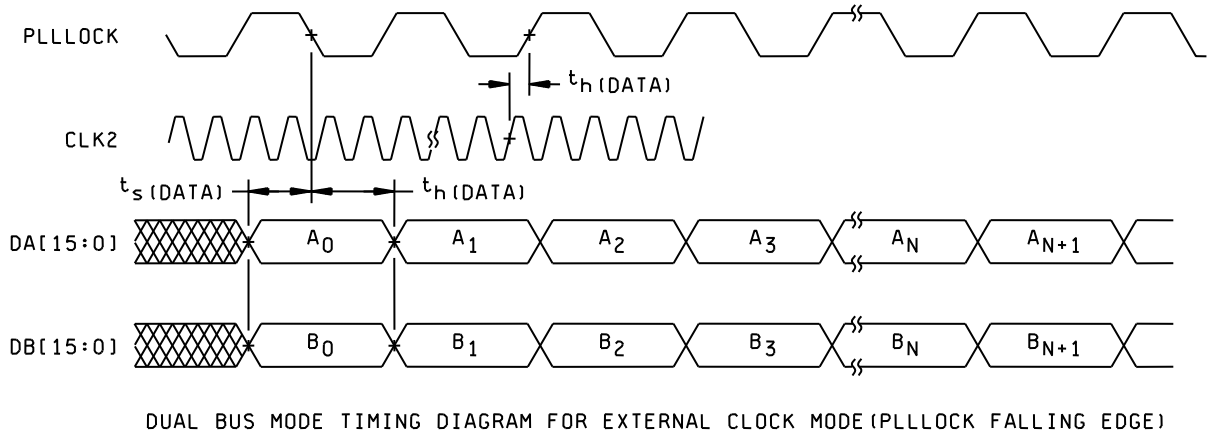


FIGURE 9. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/06650-01XE	01295	DAC5687MPZPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243