REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-02-18	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-09-20	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B								
	PAGE	1	2	3	4	5	6	7	8	9	10								

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 06-08-22	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, 16 BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06649**
	REV **B**	**PAGE** 1 **OF** 10

AMSC N/A

5962-V087-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 bit transparent D-type latch with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06649	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC16373A-EP	16 bit transparent D-type latch with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-118	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_I)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to V_{CC} + 0.5 V 2/ 3/
Maximum input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Maximum continuous output current (I_O)	±50 mA
Maximum continuous current through V_{CC} or GND	±100 mA
Package thermal impedance (θ_{JA}): 4/	63°C/W
Storage temperature range (T_{STG})	-65°C to 150°C 5/

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{CC}):	
Operating	1.65 V to 3.6 V
Data retention only	1.5 V minimum
Minimum high level input voltage (V_{IH}):	
V_{CC} = 1.65 V to 1.9 V	0.65 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	1.7 V
V_{CC} = 2.7 V to 3.6 V	2.0 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 1.65 V to 1.9 V	0.35 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	0.7 V
V_{CC} = 2.7 V to 3.6 V	0.8 V
Input voltage range (V_I)	0.0 V to 5.5 V
Maximum output voltage range (V_O):	
High or low state	0.0 V to V_{CC}
High impedance-state	0.0 V to 5.5 V
Maximum high level output current (I_{OH}):	
V_{CC} = 1.65 V	-4 mA
V_{CC} = 2.3 V	-8 mA
V_{CC} = 2.7 V	-12 mA
V_{CC} = 3.0 V	-24 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 1.65 V	4 mA
V_{CC} = 2.3 V	8 mA
V_{CC} = 2.7 V	12 mA
V_{CC} = 3.0 V	24 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	10 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The value of V_{CC} is provided in the recommended operating conditions table.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
6/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified		V_{CC}	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -100 µA		1.65 V to 3.6 V	V_{CC} – 0.2		V
		I_{OH} = -4 mA		1.65 V	1.2		
		I_{OH} = -8 mA		2.3 V	1.7		
		I_{OH} = -12 mA		2.7 V	2.2		
		I_{OH} = -12 mA		3.0 V	2.4		
		I_{OH} = -24 mA		3.0 V	2.2		
Low level output voltage	V_{OL}	I_{OL} = 100 µA		1.65 V to 3.6 V		0.2	V
		I_{OL} = 4 mA		1.65 V		0.45	
		I_{OL} = 8 mA		2.3 V		0.7	
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3.0 V		0.55	
Input current	I_I	V_I = o to 5.5 V		3.6 V		±5	µA
Off current	I_{off}	V_I or V_O = 5.5 V		0		±10	µA
Three-state output leakage current	I_{OZ}	VO = 0 to 5.5 V		3.6 V		±10	µA
Quiescent supply current	I_{CC}	V_I = VCC or GND	I_O = 0			20	µA
		3.6 V ≤ V_I ≤ 5.5 V 2/		1.65 V to 5.5V		20	
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other input at V_{CC} or GND		2.7 V to 3.6 V		500	µA
Input capacitance	C_i	V_I = VCC or GND, T_A = 25°C		3.3 V	5 Typ		pF
Output capacitance	C_o	VO = VCC or GND, T_A = 25°C		3.3 V	6.5 Typ		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

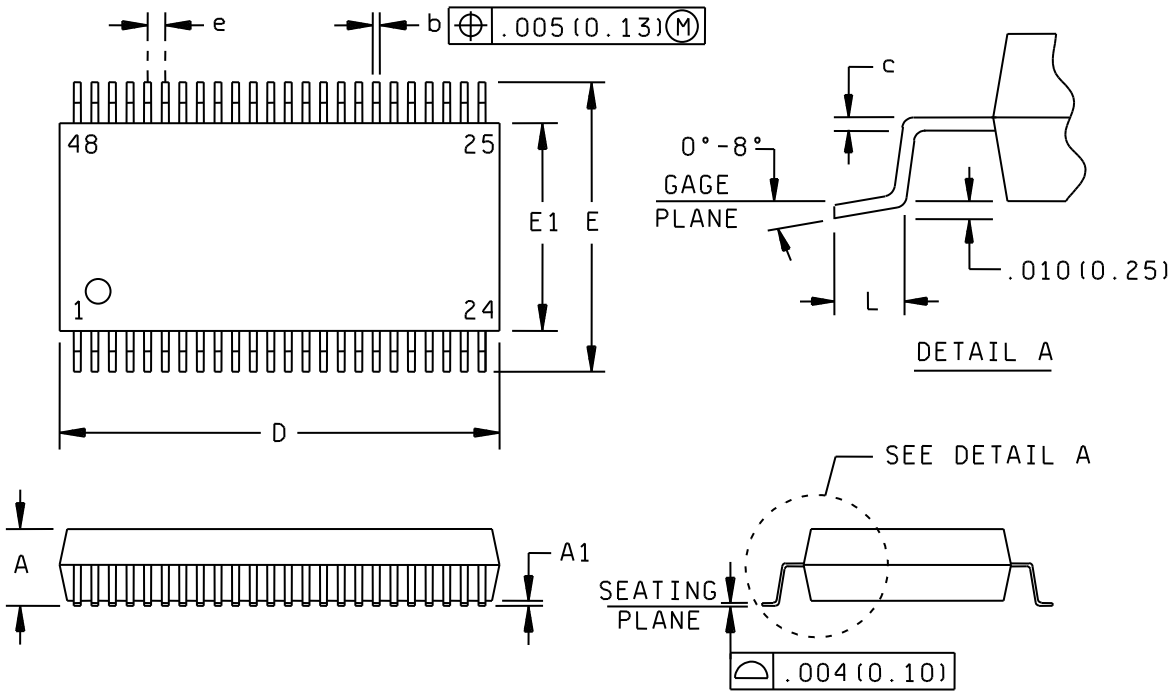
Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC} = 2.5 V ±0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ±0.3 V		
			Min	Max	Min	Max	Min	Max	
Timing requirements									
Pulse duration, LE high	t_w	See figure 5	3.3		3.3		3.3		ns
Setup time, data before LE↓	t_{su}		1.7		1.7		1.7		
Hold time, data after LE↓			1.6		1.6		1.6		
Switching characteristics									
Propagation delay time, from input D to Q	t_{pd}	See figure 5	1	5.2	1	4.9	1.6	4.2	ns
Propagation delay time, from input LE to Q	t_{pd}		1	5.2	1	5.3	1.3	4.6	
Enable time, from input $\overline{OE}$ to output Q	t_{en}		1	7.7	1	6.2	1.3	5.3	
Disable time, from input $\overline{OE}$ to output Q	t_{dis}		1	5.2	1	6.3	2.1	5.9	

Operating characteristics									
Test		Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC} = 1.8 V		V_{CC} = 2.5 V		V_{CC} = 3.3 V		Unit
				Min	Max	Min	Max	Min	Max	
Power dissipation capacitance per latch	Outputs enabled	C_{pd}	f = 10 MHz, T_A = 25°C	32 Typ		35 Typ		39 Typ		pF
	Outputs disabled			4 Typ		4 Typ		6 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This applies in the disabled state only.

Case X



Dimensions									
Symbol	Inch		Millimeter		Symbol	Inch		Millimeter	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.110		2.79	E	.291	.299	7.39	7.59
A1	.010 Typ		0.25 Typ		E1	.395	.420	10.03	10.67
b	.008	.013	0.20	0.34	e	.025 BSC		0.63 BSC	
c	.005	.010	0.13	0.25	L	.020	.040	0.51	1.02
D	.620	.630	15.75	16.00	Q	.008		0.20	

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 mm).
4. Falls within JEDEC MO-118.

FIGURE 1. Case outlines.

Inputs			Output
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	z

H = High voltage level X = Immaterial
L = Low voltage level Z = High-impedance state
Q_0 = Level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

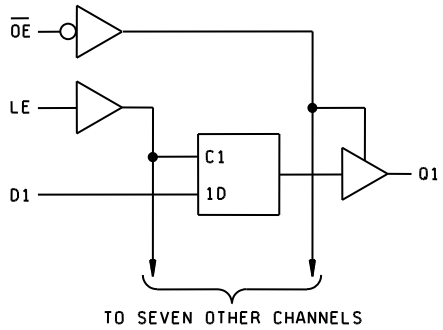
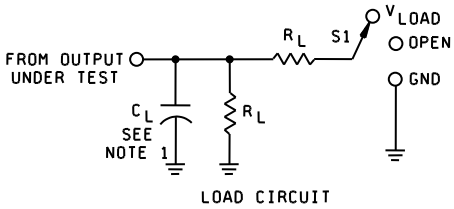


FIGURE 3. Logic diagram.

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	1 $\overline{OE}$	13	2Q1	25	2LE	37	1D8
2	1Q1	14	2Q2	26	2D8	38	1D7
3	1Q2	15	GND	27	2D7	39	GND
4	GND	16	2Q3	28	GND	40	1D6
5	1Q3	17	2Q4	29	2D6	41	1D5
6	1Q4	18	V_{CC}	30	2D5	42	V_{CC}
7	V_{CC}	19	2Q5	31	V_{CC}	43	1D4
8	1Q5	20	2Q6	32	2D4	44	1D3
9	1Q6	21	GND	33	2D3	45	GND
10	GND	22	2Q7	34	GND	46	1D2
11	1Q7	23	2Q8	35	2D2	47	1D1
12	1Q8	24	2 $\overline{OE}$	36	2D1	48	1LE

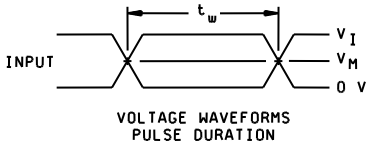
FIGURE 4. Terminal connections.



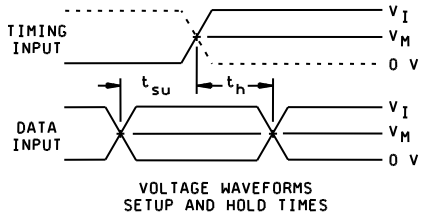
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

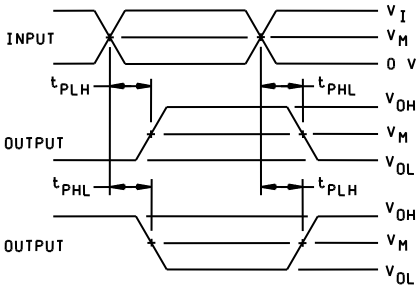
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2xV_{CC}	50 pF	500Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3.3 V ±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V



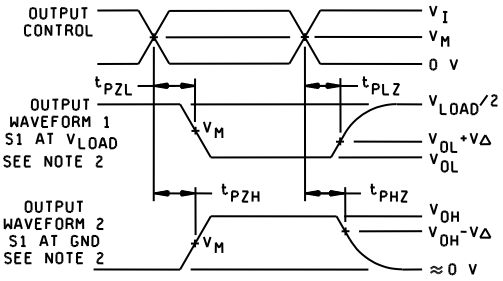
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06649-01XE	01295	CLVC16373AMDLREP	LVC16373AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243