

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make limit changes to all three ICC tests under Table I. Make change to the Input resistance (ri) maximum test limit under Table I. Update document paragraphs to current requirements. - ro	14-10-02	C. SAFFLE
B	Make change to figure 5 Receiver Enable and Disable Times voltage waveforms. Update document paragraphs to current requirements. - ro	21-06-03	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD  06-07-26	CHECKED BY TOM HESS	TITLE MICROCIRCUIT, DIGITAL-LINEAR, 3 V TO 5.5 V SINGLE CHANNEL RS-232 LINE DRIVER / RECEIVER, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/06642</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3 V to 5.5 V single channel RS-232 line driver / receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06642</u>   Drawing number	-	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>E</u>   Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	MAX3221-EP	3 V to 5.5 V single channel RS-232 line driver / receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MO-150	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (VCC) .....	-0.3 V to 6 V 2/
Positive output supply voltage range (V+) .....	-0.3 V to 7 V 2/
Negative output supply voltage range (V-) .....	0.3 V to -7 V 2/
Supply voltage difference (V+ - V-) .....	13 V 2/
Input voltage range (Vi):	
Driver (FORCEOFF, FORCEON, EN) .....	-0.3 V to 6 V
Receiver .....	-25 V to 25 V
Output voltage range (Vo):	
Driver .....	-13.2 V to 13.2 V
Receiver (INVALID) .....	-0.3 V to VCC + 0.3 V
Package thermal impedance (θJA): 3/ 4/	
Case X .....	82°C/W
Operating virtual junction temperature (TJ) .....	+150°C
Storage temperature range (Tstg) .....	-65°C to +150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range (VCC):	
VCC = 3.3 V .....	3 V to 3.6 V
VCC = 5 V .....	4.5 V to 5.5 V
Driver and control high level input voltage (VIH) at DIN, FORCEOFF, FORCEON, EN pins :	
VCC = 3.3 V .....	2 V minimum
VCC = 5 V .....	2.4 V minimum
Driver and control low level input voltage (VIL) at DIN, FORCEOFF, FORCEON, EN pins .....	0.8 V maximum
Driver and control input voltage (Vi) at DIN, FORCEOFF, FORCEON pins .....	0 V to 5.5 V
Receiver input voltage (Vi) .....	-25 V to 25 V
Operating free air temperature (TA) .....	-55°C to +125°C

- 
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ All voltages are with respect to network GND.
- 3/ Maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A) / \theta_{JA}$ . Operating at the absolute maximum TJ of 150°C can affect reliability.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ Test conditions are C1 – C4 = 0.1 μF at VCC = 3.3 V ±0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at VCC 5 V ±0.5 V. See figure 6.
- 6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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## 2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

3.5.6 Typical operating circuit. The typical operating circuit shall be as shown in figure 6.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Input leakage current $\overline{\text{FORCEOFF}}$ , $\overline{\text{FORCEON}}$ , $\overline{\text{EN}}$	I <sub>I</sub>	See figure 6	-55°C to +125°C	01		±1	μA
Supply current, auto powerdown disabled	I <sub>CC</sub>	No load, $\overline{\text{FORCEOFF}}$ and $\overline{\text{FORCEON}}$ at V <sub>CC</sub> , see figure 6, V <sub>CC</sub> = 3.3 V or 5 V	+25°C	01		2	mA
Supply current, powered off	I <sub>CC</sub>	No load, $\overline{\text{FORCEOFF}}$ at GND, V <sub>CC</sub> = 3.3 V or 5 V, see figure 6	+25°C	01		20	μA
Supply current, auto powerdown enabled	I <sub>CC</sub>	No load, $\overline{\text{FORCEOFF}}$ at V <sub>CC</sub> , $\overline{\text{FORCEON}}$ at GND, all RIN are open or grounded, V <sub>CC</sub> = 3.3 V or 5 V, see figure 6	+25°C	01		20	μA
Driver section (see figure 6)							
High level output voltage	V <sub>OH</sub>	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND	-55°C to +125°C	01	5		V
Low level output voltage	V <sub>OL</sub>	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>	-55°C to +125°C	01	-5		V
High level input current	I <sub>IH</sub>	V <sub>I</sub> = V <sub>CC</sub>	-55°C to +125°C	01		±1	μA
Low level input current	I <sub>IL</sub>	V <sub>I</sub> at GND	-55°C to +125°C	01		±1	μA
Short circuit output 3/ current	I <sub>OS</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V	-55°C to +125°C	01		±60	mA
		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V				±60	
Output resistance	r <sub>o</sub>	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>-</sub> = 0 V, V <sub>O</sub> = ±2 V	-55°C to +125°C	01	300		Ω
Output leakage current	I <sub>off</sub>	V <sub>O</sub> = ±12 V, V <sub>CC</sub> = 3 V to 3.6 V, $\overline{\text{FORCEOFF}}$ = GND	-55°C to +125°C	01		±25	μA
		V <sub>O</sub> = ±10 V, V <sub>CC</sub> = 4.5 V to 5.5 V, $\overline{\text{FORCEOFF}}$ = GND				±25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Driver section switching characteristics (see figure 6)							
Maximum data rate		C <sub>L</sub> = 1000 pF, R <sub>L</sub> = 3 kΩ, see figure 5	-55°C to +125°C	01	150		kbits/s
Pulse skew <u>5/</u>	t <sub>sk(p)</sub>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, see figure 5	+25°C	01	100 typical <u>4/</u>		ns
Slew rate, transition region (see figure 5)	SR(tr)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 150 pF to 1000 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ	-55°C to +125°C	01	6	30	V/μs
Electrostatic discharge (ESD) section							
DOUT pin ESD protection		Human body model		01	±15 typical		kV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Receiver section (see figure 6)							
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	-55°C to +125°C	01	V <sub>CC</sub> - 0.6		V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA	-55°C to +125°C	01		0.4	V
Positive going input threshold voltage	V <sub>IT+</sub>	V <sub>CC</sub> = 3.3 V	-55°C to +125°C	01		2.4	V
		V <sub>CC</sub> = 5 V				2.4	
Negative going input threshold voltage	V <sub>IT+</sub>	V <sub>CC</sub> = 3.3 V	-55°C to +125°C	01	0.6		V
		V <sub>CC</sub> = 5 V			0.8		
Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )	V <sub>hys</sub>		+25°C	01	0.5 typical <u>4/</u>		V
Output leakage current	I <sub>off</sub>	FORCEOFF = 0 V	-55°C to +125°C	01		±10	μA
Input resistance	r <sub>i</sub>	V <sub>I</sub> = ±3 V or ±25 V	-55°C to +125°C	01	3	11	kΩ
Switching characteristics section							
Propagation delay time, low to high level output	t <sub>PLH</sub>	C <sub>L</sub> = 150 pF, see figure 5	+25°C	01	150 typical <u>4/</u>		ns
Propagation delay time, high to low level output	t <sub>PHL</sub>	C <sub>L</sub> = 150 pF, see figure 5	+25°C	01	150 typical <u>4/</u>		ns
Output enable time	t <sub>en</sub>	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, see figure 5	+25°C	01	200 typical <u>4/</u>		ns
Output disable time	t <sub>dis</sub>	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, see figure 5	+25°C	01	200 typical <u>4/</u>		ns
Pulse skew <u>5/</u>	t <sub>sk(p)</sub>	See figure 5	+25°C	01	50 typical <u>4/</u>		ns
Electrostatic discharge (ESD) section							
RIN pin ESD protection		Human body model		01	±15 typical		kV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Auto powerdown section (see figure 5)							
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	V <sub>IT+(valid)</sub>	FORCEON = GND, $\overline{\text{FORCEOFF}} = \text{VCC}$	-55°C to +125°C	01		2.7	V
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	V <sub>IT-(valid)</sub>	FORCEON = GND, $\overline{\text{FORCEOFF}} = \text{VCC}$	-55°C to +125°C	01	-2.7		V
Receiver input threshold for $\overline{\text{INVALID}}$ low level output voltage	V <sub>T(invalid)</sub>	FORCEON = GND, $\overline{\text{FORCEOFF}} = \text{VCC}$	-55°C to +125°C	01	-0.2	0.3	V
$\overline{\text{INVALID}}$ high level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = \text{VCC}$	-55°C to +125°C	01	V <sub>CC</sub> - 0.6		V
$\overline{\text{INVALID}}$ low level output voltage	V <sub>OL</sub>	I <sub>OH</sub> = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = \text{VCC}$	-55°C to +125°C	01		0.4	V
Switching characteristics section (see figure 5)							
Propagation delay time, low to high level output	t <sub>valid</sub>		+25°C	01	1 typical <u>4/</u>		μs
Propagation delay time, high to low level output	t <sub>invalid</sub>		+25°C	01	30 typical <u>4/</u>		μs
Supply enable time	t <sub>en</sub>		+25°C	01	100 typical <u>4/</u>		μs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Test conditions are C1 - C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ±0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V<sub>CC</sub> = 5 V ±0.5 V.

3/ Short circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

4/ All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = +25°C.

5/ Pulse skew is defined as | t<sub>PLH</sub> – t<sub>PHL</sub> | of each channel of the same device.

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Case X

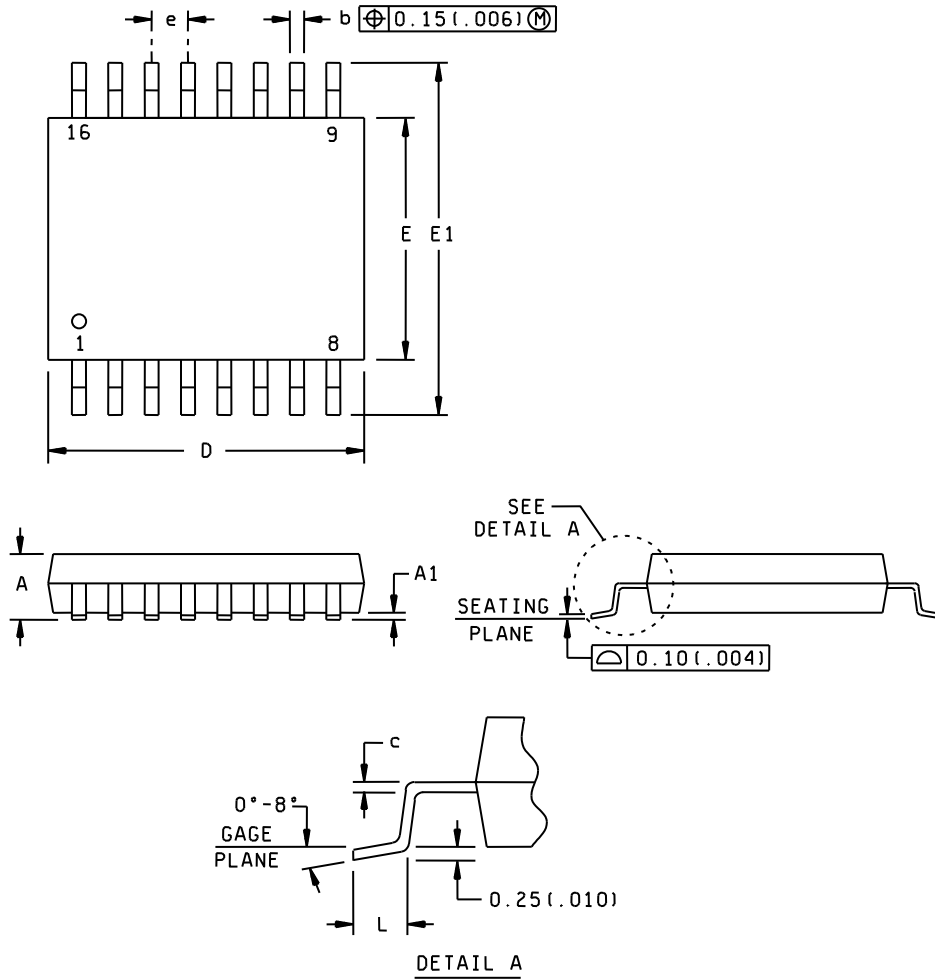


FIGURE 1. Case outline.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/06642</b></p>
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Case X - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.078	---	2.00
A1	.001	---	0.05	---
b	.008	.014	0.22	0.38
c	.003	.009	0.09	0.25
D	.232	.255	5.90	6.50
E	.196	.220	5.00	5.60
E1	.291	.322	7.40	8.20
e	.025 BSC		0.65 BSC	
L	.021	.037	0.55	0.95

NOTES:

1. All linear dimensions are in millimeters, inch equivalents are given for general information only.
2. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeter ( .006 inch )
3. Fall within JEDEC MO-150.

FIGURE 1. Case outline – Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$\overline{EN}$
2	C1+
3	V+
4	C1-
5	C2+
6	C2-
7	V-
8	RIN
9	ROUT
10	$\overline{INVALID}$
11	DIN
12	FORCEON
13	DOUT
14	GND
15	Vcc
16	$\overline{FORCEOFF}$

FIGURE 2. Terminal connections.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06642</b>
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Each driver

Inputs				Output	Driver status
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	Valid RIN RS-232 level	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto powerdown disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with auto powerdown enabled
H	L	H	YES	L	
L	L	H	NO	Z	Power off by auto powerdown feature
H	L	H	NO	Z	

H = High level  
 L = Low level  
 X = Irrelevant  
 Z = High impedance

Each receiver

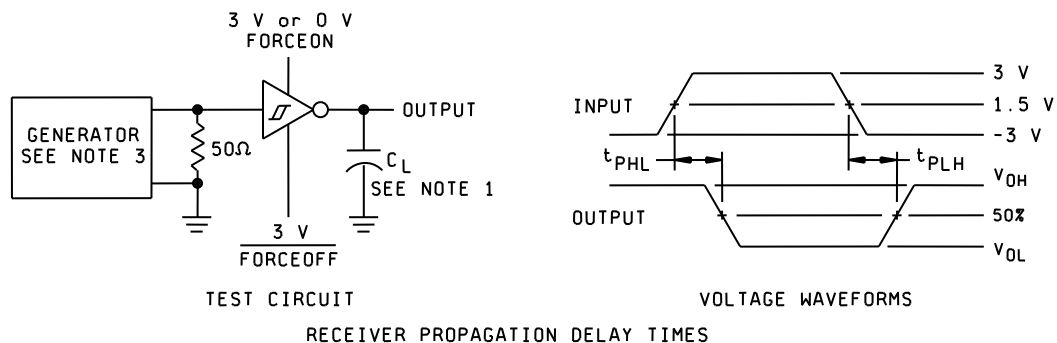
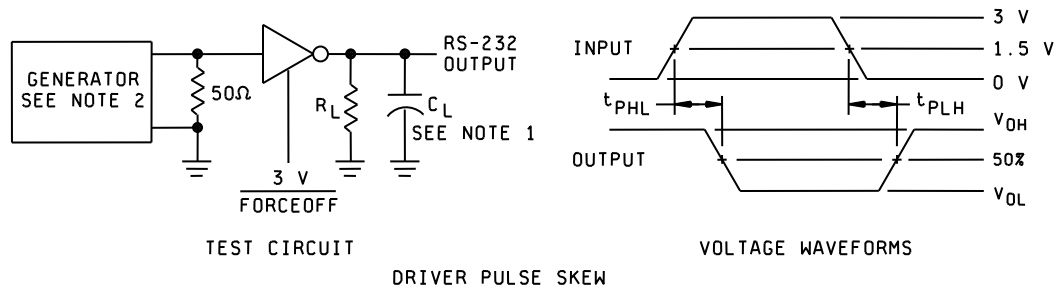
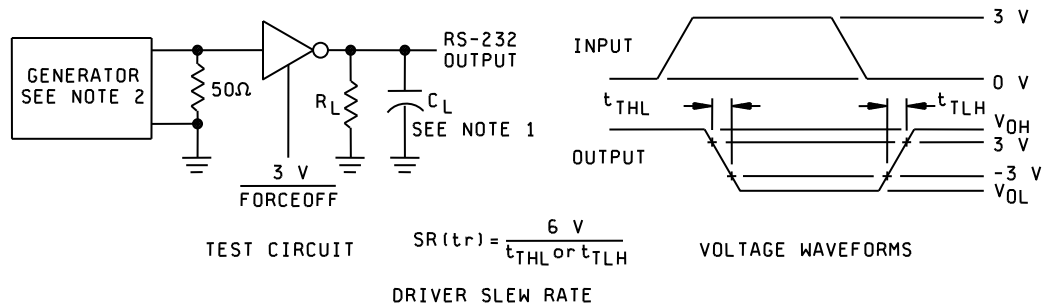
Inputs			Output
RIN	$\overline{\text{EN}}$	Valid RIN RS-232 level	ROUT
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = High level  
 L = Low level  
 X = Irrelevant  
 Z = High impedance (off)  
 Open = Disconnected input or connected driver off

FIGURE 3. Truth table.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06642</b>
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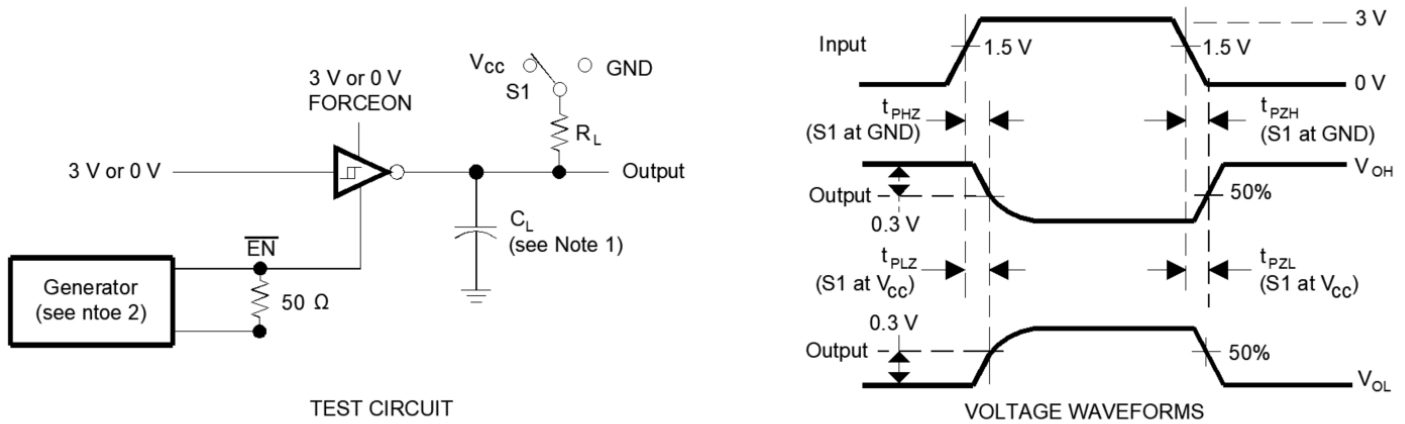


NOTES:

1. CL includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_0 = 50\ \Omega$ , 50 % duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .
3. The pulse generator has the following characteristics:  $Z_0 = 50\ \Omega$ , 50 % duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

FIGURE 5. Timing waveforms and test circuit.

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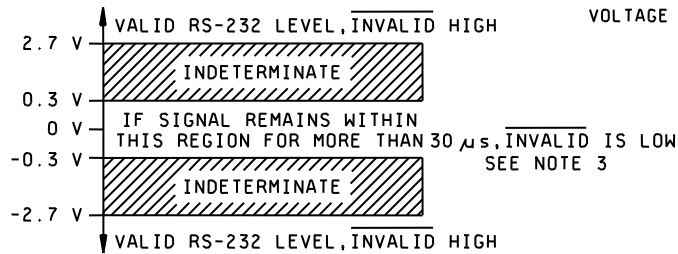
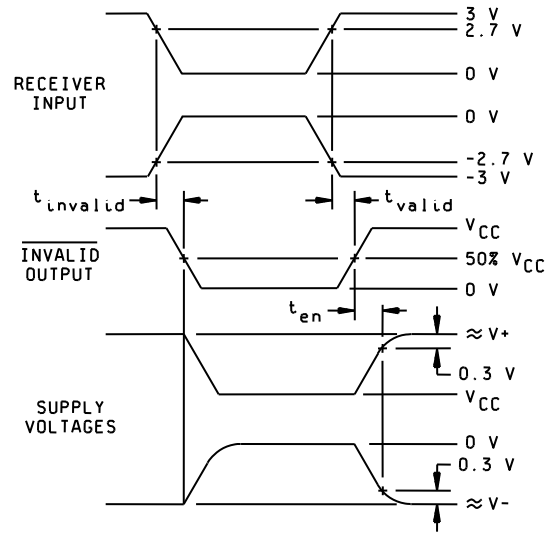
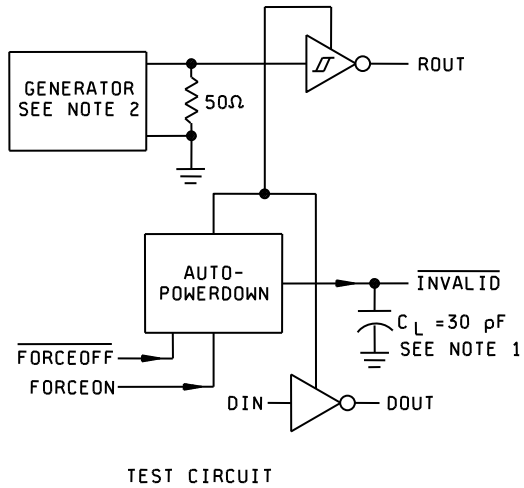
### RECEIVER ENABLE AND DISABLE TIMES

#### NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50 % duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.
3.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
4.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

FIGURE 5. Timing waveforms and test circuit – Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06642</b>
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INVALID PROPAGATION DELAY TIMES AND SUPPLY ENABLING TIME

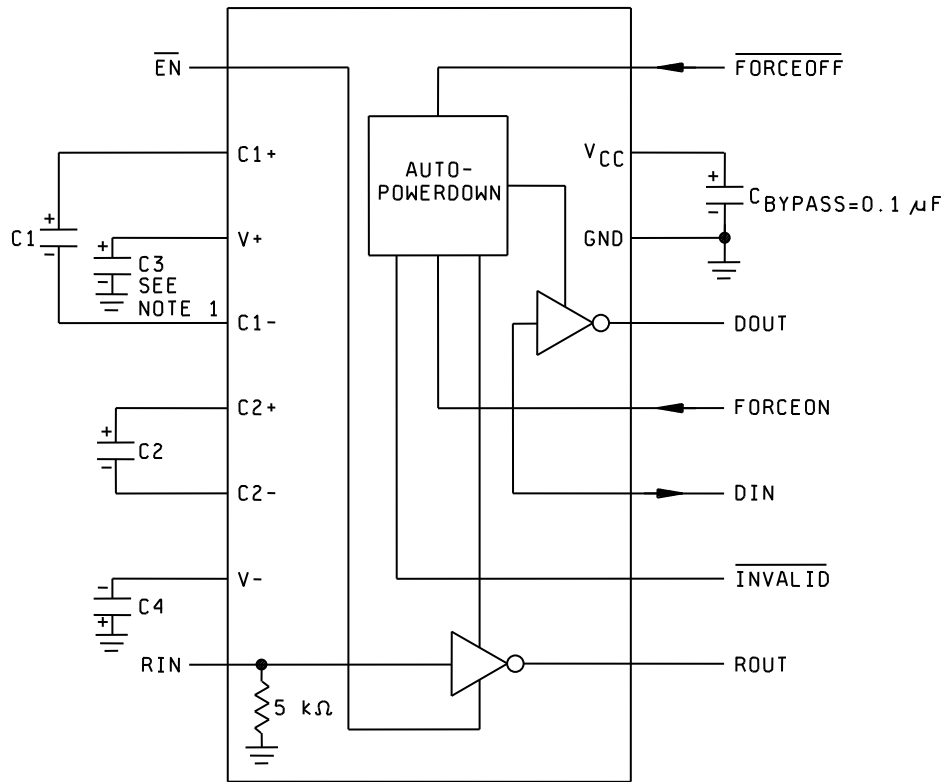
NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_0 = 50 \Omega$ , 50 % duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.
3. Auto powerdown disables drivers and reduces supply current to  $1 \mu\text{A}$ .

FIGURE 5. Timing waveforms and test circuit – Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/06642</b>
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NOTES:

1. C3 can be connected to VCC or GND.
2. Resistor values shown are nominal.
3. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

VCC versus capacitor values		
VCC	C1	C2, C3, C4
3.3 V ±0.3 V	0.1 μF	0.1 μF
5 V ±0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

FIGURE 6. Typical operating circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package <u>2/</u>	Top side marking	Vendor part number
V62/06642-01XE	01295	Reel of 2000	MB3221M	MAX3221MDBREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln.  
PO Box 660199  
Dallas, TX 75243

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