

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	14/07/10	C. SAFFLE

**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV		A	A	A	A	A	A	A	A	A	A	A	A						
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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 06-06-29	CHECKED BY TOM HESS	TITLE MICROCIRCUIT, DIGITAL, DUAL INVERTER BUFFER / DRIVER WITH OPEN DRAIN OUTPUTS, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/06640
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual inverter buffer/driver with open drain outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06640</u>	-	<u>01</u>	X	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC2G06-EP	Dual inverter buffer/driver with open drain outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	MO-203-AB	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +6.5 V
Input voltage range (V_I)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to +6.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Continuous output current (I_O)	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance (θ_{JA})	+259°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The value of V_{CC} is provided in the recommended operating conditions table.

4/ The package terminal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 5/

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V _{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
High level input voltage	V _{IH}	V _{CC} = 1.65 V to 1.95 V	0.65 x V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 x V _{CC}		
Low level input voltage	V _{IL}	V _{CC} = 1.65 V to 1.95 V		0.35 x V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 x V _{CC}	
Input voltage	V _I		0	5.5	V
Output voltage	V _O		0	5.5	V
Low level output current	I _{OL}	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3.0 V		16	
				24	
		V _{CC} = 4.5 V		32	
Input transition rise or fall rate	$\Delta t / \Delta v$	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
Operating free air ambient temperature	T _A		-55	+125	°C

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the manufacturer application report, Implications of Slow or Floating CMOS inputs, literature number SCBA004.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Low level output voltage	V _{OL}	I _{OL} = 100 μA, V _{CC} = 1.65 V to 5.5 V	-55°C to +125°C	01		0.1	V
		I _{OL} = 4 mA, V _{CC} = 1.65 V				0.45	
		I _{OL} = 8 mA, V _{CC} = 2.3 V				0.3	
		I _{OL} = 16 mA, V _{CC} = 3 V				0.4	
		I _{OL} = 24 mA, V _{CC} = 3 V				0.55	
		I _{OL} = 32 mA, V _{CC} = 4.5 V				0.55	
Input current A inputs	I _I	V _I = 5.5 V or GND, V _{CC} = 0 V to 5.5 V	-55°C to +125°C	01		±5	μA
Off state leakage current	I _{off}	V _I or V _O = 5.5 V, V _{CC} = 0 V	-55°C to +125°C	01		±10	μA
Quiescent supply current	I _{CC}	V _I = 5.5 V or GND, I _O = 0, V _{CC} = 1.65 V to 5.5 V	-55°C to +125°C	01		10	μA
Delta quiescent supply current	ΔI _{CC}	One input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND, V _{CC} = 3 V to 5.5 V	-55°C to +125°C	01		500	μA
Input capacitance	C _i	V _I = V _{CC} or GND, V _{CC} = 3.3 V	T _A = +25°C	01	3.5 typical		pF
From input A to output Y	t _{pd}	V _{CC} = 1.8 V ±0.15 V	-55°C to +125°C	01	1.8	9.1	ns
		V _{CC} = 2.5 V ±0.2 V			0.9	5.7	
		V _{CC} = 3.3 V ±0.3 V			0.9	4.6	
		V _{CC} = 5 V ±0.5 V			0.7	3.9	
Power dissipation capacitance	C _{pd}	V _{CC} = 1.8 V, f = 10 MHz	T _A = +25°C	01	2 typical		pF
		V _{CC} = 2.5 V, f = 10 MHz			2 typical		
		V _{CC} = 3.3 V, f = 10 MHz			3 typical		
		V _{CC} = 5 V, f = 10 MHz			4 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X

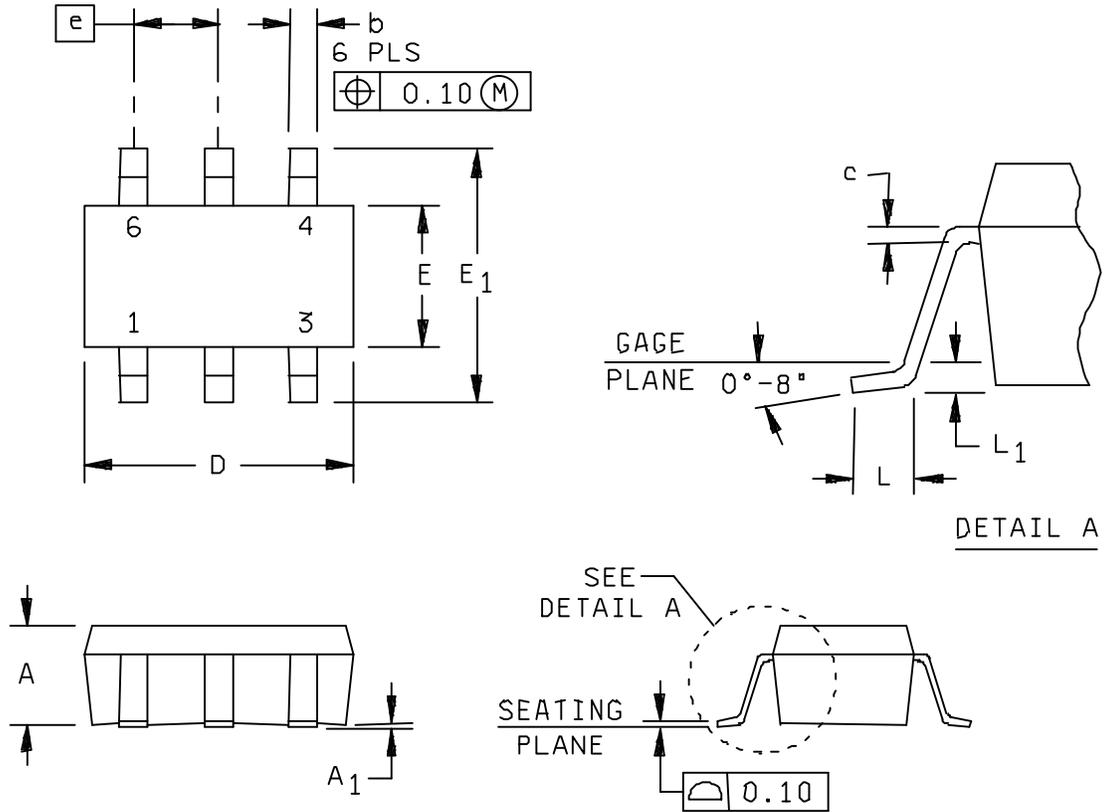


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/06640</p>
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Case X – continued

Symbol	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
A	.031	.043	0.80	1.10
A1	.000	.003	0.00	0.10
b	.005	.011	0.15	0.30
c	.003	.008	0.08	0.22
D	.072	.084	1.85	2.15
E	.043	.055	1.10	1.40
E1	.070	.094	1.80	2.40
e	.025 BSC		0.65 BSC	
L	.010	.018	0.26	0.46
L1	.005 BSC		0.15 BSC	
n	6 leads		6 leads	

Notes:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per side.
3. Falls with JEDEC MO-203-AB.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	INPUT 1A
2	GND
3	INPUT 2A
4	OUTPUT 2Y
5	V _{CC}
6	OUTPUT 1Y

FIGURE 2. Terminal connections.

(Each inverter)

Input	Output
A	Y
H	L
L	H

FIGURE 3. Truth table.

(Positive logic)

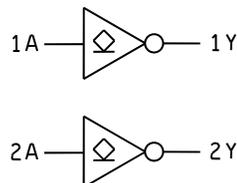
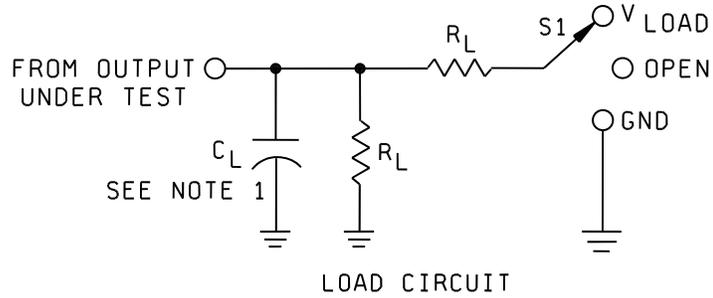


FIGURE 4. Logic diagram.

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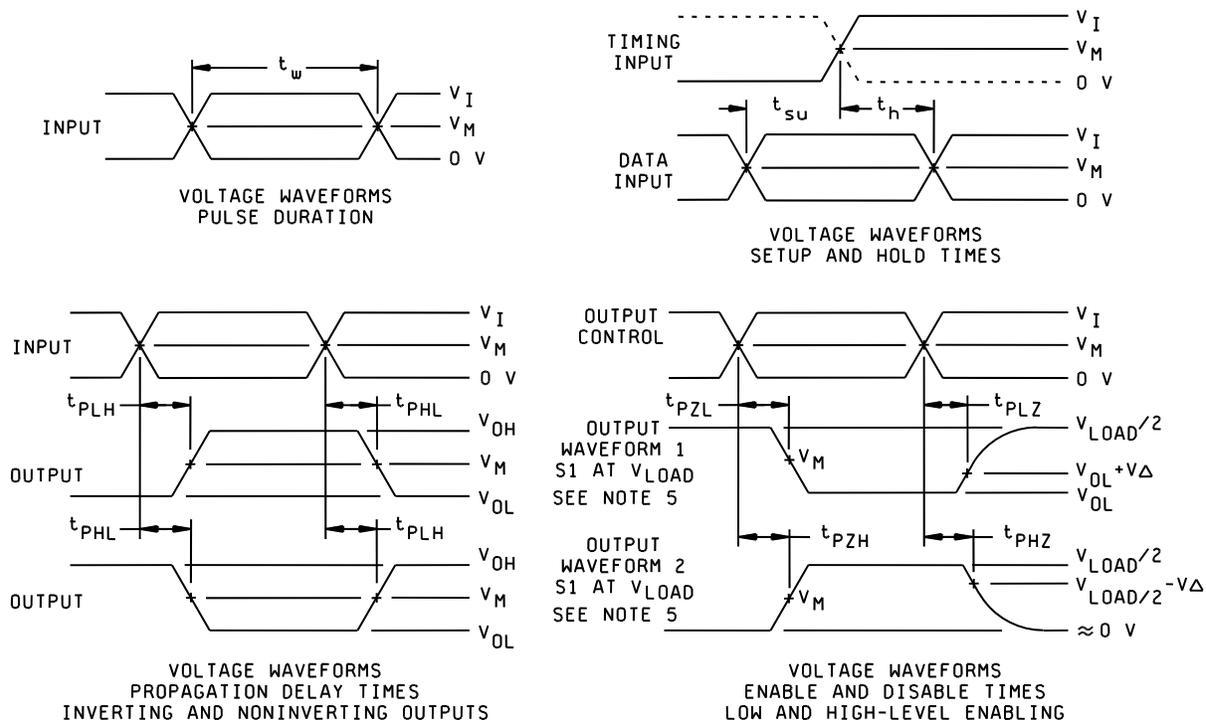


Test	S1
t _{PZL} (see notes 2 and 3)	V _{LOAD}
t _{PLZ} (see notes 2 and 4)	V _{LOAD}
t _{PHZ} / t _{PZH}	V _{LOAD}

V _{CC}	Inputs		V _M	V _{LOAD}	C _L	R _L	V _Δ
	V _I	t _r / t _f					
1.8 V ±0.15 V	V _{CC}	≤ 2 ns	V _{CC} / 2	2 x V _{CC}	30 pF	1 kΩ	0.15 V
2.5 V ±0.20 V	V _{CC}	≤ 2 ns	V _{CC} / 2	2 x V _{CC}	30 pF	500 Ω	0.15 V
3.3 V ±0.30 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.0 V ±0.50V	V _{CC}	≤ 2.5 ns	V _{CC} / 2	2 x V _{CC}	50 pF	500 Ω	0.3 V

FIGURE 5. Load circuit and timing waveforms.

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NOTES:

1. C_L includes probe and jig capacitance.
2. Since this device has open drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
3. t_{PZL} is measured at V_M .
4. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
6. All input pulses are supplied by generators having following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
7. The outputs are measured one at a time with one transaction per measurement.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms – Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/06640-01XE	01295	CTO	SN74LVC2G06MDCKREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Ln.
 PO Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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