

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual 14-bit 200 MSPS digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| | | | | |
|-------------------|---|----------------------------|-----------------------------|----------------------------|
| <u>V62/06639</u> | - | <u>01</u> | <u>X</u> | <u>E</u> |
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| <u>Device type</u> | <u>Generic</u> | <u>Circuit function</u> |
|--------------------|----------------|--|
| 01 | DAC5672-EP | Dual 14-bit 200 MSPS digital to analog converter |
| 02 | DAC5672-EP | Dual 14-bit 200 MSPS digital to analog converter |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| <u>Outline letter</u> | <u>Number of pins</u> | <u>JEDEC PUB 95</u> | <u>Package style</u> |
|-----------------------|-----------------------|---------------------|-----------------------|
| X | 48 | MS-026 | Plastic quad flatpack |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

| <u>Finish designator</u> | <u>Material</u> |
|--------------------------|--------------------------|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

| | | | |
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| | | REV C | PAGE 2 |

1.3 Absolute maximum ratings. 1/

Supply voltage range:

- (AVDD) -0.5 V to 4.0 V 2/
- (DVDD) -0.5 V to 4.0 V 3/
- Voltage between AGND and DGND -0.5 V to 0.5 V
- Voltage between AVDD and DVDD -0.5 V to 0.5 V

Supply voltage range:

- DA[13:0] and DB[13:0] -0.5 V to DVDD + 0.5 V 3/
 - MODE, CLKA, CLKB, WRTA, WRTB -0.5 V to DVDD + 0.5 V 3/
 - IOUTA1, IOUTA2, IOUTB1, IOUTB2 -1.0 V to AVDD + 0.5 V 2/
 - EXTIO, BIASJ_A, BIASJ_B, SLEEP -0.5 V to AVDD + 0.5 V 2/
 - Peak input current (any input) 20 mA
 - Peak total input current (all inputs) -30 mA
 - Operating free-air temperature range (TA) -55°C to +125°C
 - Storage temperature range (TSTG) -65°C to 150°C
 - Lead temperature (1.6 mm (1/16 in) from the case for 10 seconds) 260°C
- Package thermal characteristics, case X:

| Parameter | Thermal pad connected to PCB thermal plane |
|---|--|
| Thermal resistance, junction to ambient | 63.7°C/W |
| Thermal resistance, junction to case | 19.6°C/W |

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Measured with respect to AGND.

3/ Measured with respect to DGND.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 3 |

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating life derating chart. The operating life derating chart shall be as shown in figure 4.

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|---|-------------------|---------------------------------|------------------------------|
| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 4 |

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions 2/ | Limits | | Unit | |
|--------------------------------------|--------|--------------------------------------|----------------------|------|------|-----|
| | | | Min | Max | | |
| DC Specifications | | | | | | |
| Resolution | | | 14 | | Bits | |
| DC Accuracy 3/ | | | | | | |
| Integral nonlinearity | INL | 1 LSB = IOUTFS/2 ¹⁴ | TA = 25°C | -4 | 4 | LSB |
| | | | TA = -55°C and 125°C | -5 | 5 | |
| Differential nonlinearity | DNL | 1 LSB = IOUTFS/2 ¹⁴ | TA = 25°C | -3 | 3 | LSB |
| | | | TA = -55°C and 125°C | -4 | 4 | |
| Analog output | | | | | | |
| Offset error | | Mid-scale value (internal reference) | ±0.03 typical | | %FSR | |
| Offset mismatch | | Mid-scale value (internal reference) | ±0.03 typical | | %FSR | |
| Gain error | | With external reference at 1.25 V | ±0.25 typical | | %FSR | |
| | | With internal reference | ±0.25 typical | | | |
| Minimum full scale output current 4/ | | | 2 typical | | mA | |
| Maximum full scale output current 4/ | | | 20 typical | | mA | |
| Gain mismatch | | With external reference | -2 | 2 | %FSR | |
| | | With internal reference | -2 | 2 | | |
| Output voltage compliance range 5/ | | | -0.8 | 1.25 | V | |
| Output resistance | RO | | 300 typical | | kΩ | |
| Output capacitance | CO | | 5 typical | | pF | |
| Reference Output | | | | | | |
| Reference voltage | | | 1.14 | 1.26 | V | |
| Reference output current 6/ | | | 100 typical | | nA | |
| Reference Input | | | | | | |
| Input voltage | VEXTIO | | 0.1 | 1.25 | V | |
| Input resistance | RI | | 1 typical | | MΩ | |
| Small signal bandwidth | | | 300 typical | | kHz | |
| Input capacitance | CI | | 100 typical | | pF | |

See footnotes at end of table.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 5 |

TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions <u>2/</u> | Limits | | Unit |
|--------------------------|--------|-------------------------|-------------|-----|-----------|
| | | | Min | Max | |
| Temperature Coefficients | | | | | |
| Offset drift | | | 2 typical | | <u>7/</u> |
| Gain drift | | With external reference | ±20 typical | | <u>7/</u> |
| | | With internal reference | ±40 typical | | |
| Reference voltage drift | | | ±20 typical | | ppm/°C |

| Test | Symbol | Conditions <u>8/</u> | Limits | | Unit |
|--------------------------------------|--------|--|-------------|-----|--------|
| | | | Min | Max | |
| Power Supply | | | | | |
| Analog supply voltage | AVDD | | 3.0 | 3.6 | V |
| Digital supply voltage | DVDD | | 3.0 | 3.6 | V |
| Supply current, analog | IAVDD | Including output current through load resistor | | 90 | mA |
| | | Sleep mode with clock | | 6 | |
| | | Sleep mode without clock | 2.5 typical | | |
| Supply current, digital | IDVDD | | | 38 | mA |
| | | Sleep mode with clock | | 18 | |
| | | Sleep mode without clock | 0.6 typical | | |
| Power dissipation | | | | 390 | mW |
| | | Sleep mode with clock | 53 typical | | |
| | | Sleep mode without clock | 9.2 typical | | |
| | | fDATA = 200 MSPS, fOUT = 20 MHz | 350 typical | | |
| Analog power supply rejection ratio | APSRR | | -0.2 | 0.2 | %FSR/V |
| Digital power supply rejection ratio | DPSRR | | -0.2 | 0.2 | %FSR/V |
| Operating free air temperature | TA | | -55 | 125 | °C |

See footnotes at end of table.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 6 |

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 9/ | Limits | | Unit |
|---|------------------|--|-------------|-----|--------|
| | | | Min | Max | |
| Analog Output | | | | | |
| Maximum output update rate | f _{clk} | | 200 | | MSPS |
| Output settling time to 0.1% (DAC) | t _s | Mid scale transition | 20 typical | | ns |
| Output rise time 10% to 90% (OUT) | t _r | | 1.4 typical | | ns |
| Output fall time 90% to 10% (OUT) | t _f | | 1.5 typical | | ns |
| Output noise | | I _{OUTFS} = 20 mA | 55 typical | | pA/√Hz |
| | | I _{OUTFS} = 2 mA | 30 typical | | |
| AC Linearity (estimates based on measurements of preliminary parts) | | | | | |
| Spurious free dynamic range | SFDR | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 50 MSPS, f _{OUT} = 1 MHz, I _{OUTFS} = 0 dB | 83 typical | | dBc |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 50 MSPS, f _{OUT} = 1 MHz, I _{OUTFS} = -6 dB | 80 typical | | |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 50 MSPS, f _{OUT} = 1 MHz, I _{OUTFS} = -12 dB | 79 typical | | |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 100 MSPS, f _{OUT} = 5 MHz | 84 typical | | |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 100 MSPS, f _{OUT} = 20 MHz | 79 typical | | |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 200 MSPS, f _{OUT} = 20 MHz | 68 | | |
| | | 1st Nyquist zone, T _A = -55°C to 125°C, f _{DATA} = 200 MSPS, f _{OUT} = 20 MHz | 65 | | |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 200 MSPS, f _{OUT} = 41 MHz | 72 typical | | |
| Signal to noise ratio | SNR | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 100 MSPS, f _{OUT} = 5 MHz | 77 typical | | dB |
| | | 1st Nyquist zone, T _A = 25°C, f _{DATA} = 160 MSPS, f _{OUT} = 20 MHz | 70 typical | | |

See footnotes at end of table.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 7 |

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 9/ | Limits | | Unit |
|--------------------------------------|--------|---|------------|-----|------|
| | | | Min | Max | |
| Adjacent channel leakage ratio | ACLR | W-CDMA signal with 3.84 MHz bandwidth, fDATA = 61.44 MSPS, IF = 15.360 MHz | 75 typical | | dB |
| | | W-CDMA signal with 3.84 MHz bandwidth, fDATA = 122.88 MSPS, IF = 30.72 MHz | 73 typical | | |
| | | W-CDMA signal with 3.84 MHz bandwidth, fDATA = 61.44 MSPS, baseband | 78 typical | | |
| | | W-CDMA signal with 3.84 MHz bandwidth, fDATA = 122.88 MSPS, baseband | 78 typical | | |
| Third order two tone intermodulation | IMD3 | Each tone at -6 dBFS, TA = 25°C, fDATA = 200 MSPS, fOUT = 45.4 MHz and 46.4 MHz | 65 typical | | dBc |
| | | Each tone at -6 dBFS, TA = 25°C, fDATA = 100 MSPS, fOUT = 15.1 MHz and 16.1 MHz | 79 typical | | |
| Four tone intermodulation | IMD | Each tone at -12 dBFS, TA = 25°C, fDATA = 100 MSPS, fOUT = 15.6, 15.8, 16.2, and 16.4 MHz | 79 typical | | dBc |
| | | Each tone at -12 dBFS, TA = 25°C, fDATA = 165 MSPS, fOUT = 68.8, 69.6, 71.2, and 72 MHz | 61 typical | | |
| | | Each tone at -12 dBFS, TA = 25°C, fDATA = 165 MSPS, fOUT = 19, 19.1, 19.3, and 19.4 MHz | 73 typical | | |
| Channel isolation | | TA = 25°C, fDATA = 165 MSPS, fOUT(CH1) = 20 MHz, fOUT(CH2) = 21 MHz | 95 typical | | dBc |

| Test | Symbol | Conditions 10/ | Limits | | Unit |
|-------------------------------------|------------------------|-------------------|-------------|-----|------|
| | | | Min | Max | |
| Digital Input | | | | | |
| High level input voltage | V _{IH} | | 2.0 | 3.3 | V |
| Low level input voltage | V _{IL} | | 0 | 0.8 | V |
| High level input current | I _{IH} | | ±50 typical | | µA |
| Low level input current | I _{IL} | | ±10 typical | | µA |
| High level input current. GSET pin | I _{IH} (GSET) | | 7 typical | | µA |
| Low level input current, . GSET pin | I _{IL} (GSET) | | -80 typical | | µA |

See footnotes at end of table.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 8 |

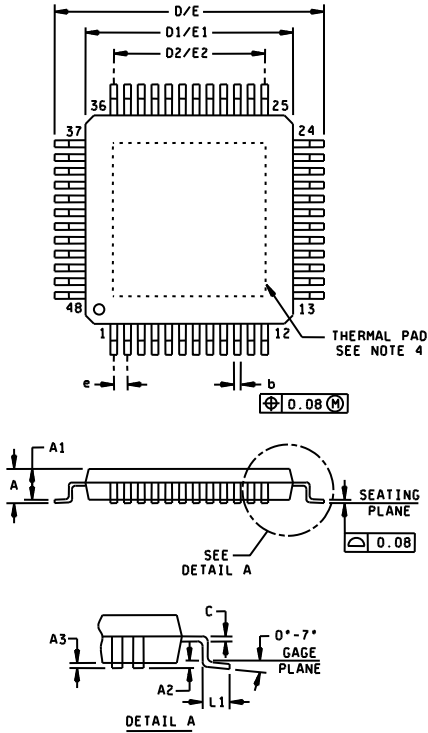
TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions <u>10/</u> | Limits | | Unit |
|--|------------------------|--------------------------|-------------|-----|------|
| | | | Min | Max | |
| Digital Input – continued. | | | | | |
| High level input current. MODE pin | I _{IH} (MODE) | | -30 typical | | μA |
| Low level input current, . MODE pin | I _{IL} (MODE) | | -80 typical | | μA |
| Input capacitance | C _I | | 5 typical | | pF |
| Switching Characteristics | | | | | |
| Timing-Dual Bus Mode | | | | | |
| Input setup time | t _{su} | | 1 | | ns |
| Input hold time | t _h | | 1 | | ns |
| Input clock pulse high time | t _{LPH} | | 1 typical | | ns |
| Clock latency (WRTA/B to outputs) <u>11/</u> | t _{LAT} | | 4 | 4 | clk |
| Propagation delay time | t _{PD} | | 1.5 typical | | ns |
| Timing- Single Bus Interleaved Mode | | | | | |
| Input setup time | t _{su} | | 0.5 typical | | ns |
| Input hold time | t _h | | 0.5 typical | | ns |
| Clock latency (WRTA/B to outputs) <u>11/</u> | t _{LAT} | | 4 | 4 | clk |
| Propagation delay time | t _{PD} | | 1.5 typical | | ns |

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating free air temperature range, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode (unless otherwise noted).
- 3/ Measured differentially through 50 Ω to AGND.
- 4/ Nominal full scale current, I_{OUTFS}, equal 32x the I_{BIAS} current.
- 5/ The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
- 6/ Use an external buffer amplifier with high impedance input to drive any external load.
- 7/ ppm of FSR/°C
- 8/ Over operating free air temperature range, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, independent gain set mode (unless otherwise noted).
- 9/ AC specifications over operating free air temperature range, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode, differential 1:1 impedance ration transformer coupled output, 50 Ω doubly terminated load (unless otherwise noted).
- 10/ Digital specifications over operating free air temperature range, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, (unless otherwise noted).
- 11/ Specified by design.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 9 |

Case X



| Dimension | | | | | |
|-----------|-------------|------|--------|-------------|------|
| Symbol | Millimeters | | Symbol | Millimeters | |
| | Min | Max | | Min | Max |
| A | | 1.20 | D/E | 8.80 | 9.20 |
| A1 | 0.95 | 1.05 | D1/E1 | 6.80 | 7.20 |
| A2 | 0.25 TYP | | D2/E2 | 5.50 TYP | |
| A3 | 0.05 | | e | 0.50 NOM | |
| b | 0.17 | 0.27 | L1 | 0.45 | 0.75 |
| c | 0.13 NOM | | | | |

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

| | | | |
|---|------------------|--------------------------------|-----------------------------|
| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 10 |

Case X

| Terminal number | Terminal symbol | Terminal number | Terminal symbol | Terminal number | Terminal symbol | Terminal number | Terminal symbol |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 1 | DA13(MSB) | 13 | DA1 | 25 | DB11 | 37 | SLEEP |
| 2 | DA12 | 14 | DA0(LSB) | 26 | DB10 | 38 | AGND |
| 3 | DA11 | 15 | DGND | 27 | DB9 | 39 | IOUTB1 |
| 4 | DA10 | 16 | DVDD | 28 | DB8 | 40 | IOUTB2 |
| 5 | DA9 | 17 | WRTA/WRTIQ | 29 | DB7 | 41 | BIASJ_B |
| 6 | DA8 | 18 | CLKA/CLKIQ | 30 | DB6 | 42 | GSET |
| 7 | DA7 | 19 | CLKB/RESETIQ | 31 | DB5 | 43 | EXTIO |
| 8 | DA6 | 20 | WRTB/SELECTIQ | 32 | DB4 | 44 | BIASJ_A |
| 9 | DA5 | 21 | DGND | 33 | DB3 | 45 | IOUTA2 |
| 10 | DA4 | 22 | DVDD | 34 | DB2 | 46 | IOUTA1 |
| 11 | DA3 | 23 | DB13(MSB) | 35 | DB1 | 47 | AVDD |
| 12 | DA2 | 24 | DB12 | 36 | DB0(LSB) | 48 | MODE |

FIGURE 2. Terminal connections.

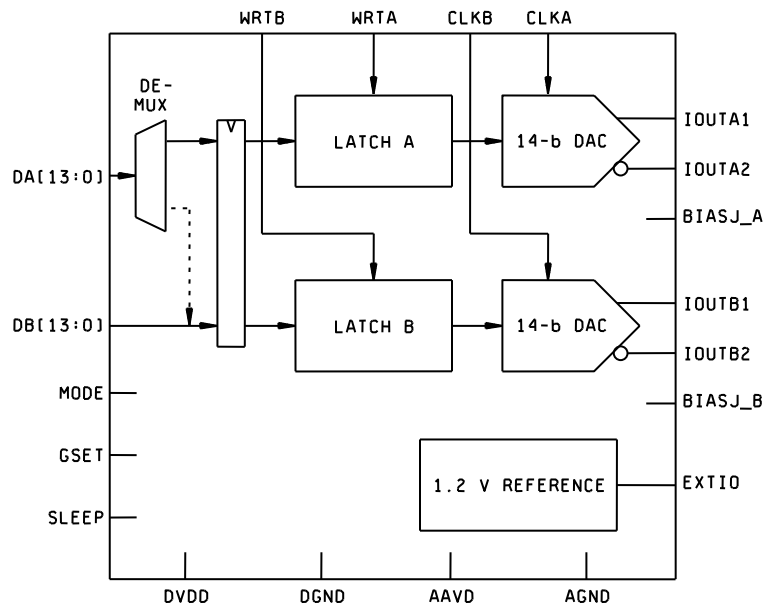


FIGURE 3. Functional block diagram.

| | | | |
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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 11 |

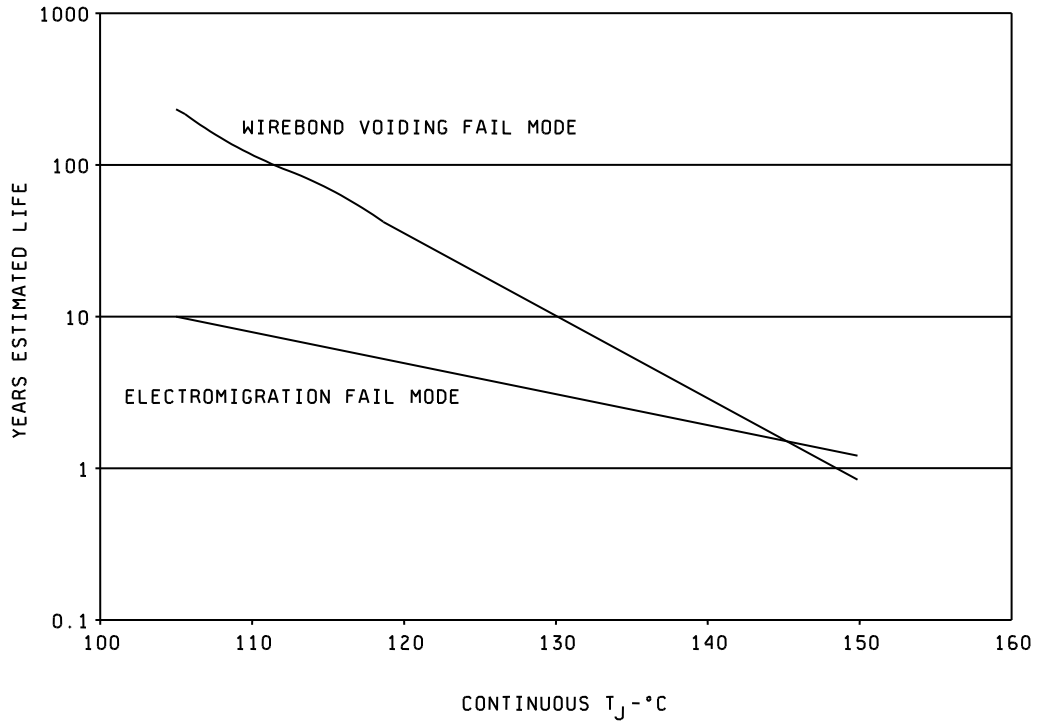


FIGURE 4. Operating life derating chart.

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| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 12 |

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

| Vendor item drawing administrative control number <u>1/</u> | Device manufacturer CAGE code | Top side marking | Vendor part number |
|---|-------------------------------|------------------|--------------------|
| V62/06639-01XE | 01295 | DAC5672EP | DAC5672MPFBREP |
| V62/06639-02XE | 01295 | DAC5672EP | DAC5672MPFBEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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|---|-------------------|---------------------------------|------------------------------|
| DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO | SIZE A | CODE IDENT NO. 16236 | DWG NO. V62/06639 |
| | | REV C | PAGE 13 |