REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. Update boilerplate to current revision. - CFS	06-12-15	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-01-27	Thomas M. Hess
C	Add terminal symbol descriptions to Figure 1. Update document paragraphs to current requirements. - ro	20-01-09	James R. Eschmeyer
D	Delete thermal pad references from paragraph 1.3 and from case outline X JEDEC MS-026 as specified under figure 1. Add Top side marking and Mode of transportation and quantity columns to paragraph 6.3. - ro	21-01-06	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D		
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-07-12	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, DUAL 10-BIT 200 MSPS DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06638**
	REV **D**	**PAGE** 1 **OF** 15

AMSC N/A

5962-V098-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual 10-bit 200 MSPS digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06638	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DAC5652-EP	Dual 10-bit 200 MSPS digital to analog converter
02	DAC5652-EP	Dual 10-bit 200 MSPS digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:	
(AV_{DD})	-0.5 V to 4.0 V 2/
(DV_{DD})	-0.5 V to 4.0 V 3/
Voltage between AGND and DGND	-0.5 V to 0.5 V
Voltage between AV_{DD} and DV_{DD}	-0.5 V to 0.5 V
Supply voltage range:	
DA[9:0] and DB[9:0]	-0.5 V to DV_{DD} + 0.5 V 3/
MODE, CLKA, CLKB, WRTA, WRTB	-0.5 V to DV_{DD} + 0.5 V 3/
IOUTA1, IOUTA2, IOUTB1, IOUTB2	-1.0 V to AV_{DD} + 0.5 V 2/
EXTIO, BIASJ_A, BIASJ_B, SLEEP	-0.5 V to AV_{DD} + 0.5 V 2/
Peak input current (any input)	20 mA
Peak total input current (all inputs)	-30 mA
Operating free-air temperature range (T_A)	-55°C to +125°C 4/ 5/
Storage temperature range (T_{STG})	-65°C to 150°C
Lead temperature (1.6 mm (1/16 in) from the case for 10 seconds)	260°C
Thermal resistance, junction to ambient (θ_{JA})	65.3°C/W
Thermal resistance, junction to case (θ_{JC})	16.4°C/W

_____

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Measured with respect to AGND.

3/ Measured with respect to DGND.

4/ Airflow or heatsinking required for sustained operation at 85°C.

5/ Airflow or heatsinking reduces θ_{JA} and is highly recommended.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating life derating chart. The operating life derating chart shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
DC Specifications					
Resolution			10		Bits
DC Accuracy 3/					
Integral nonlinearity	INL	1 LSB = $I_{OUTFS}/2^{10}$, T_{MIN} to T_{MAX}	-1	1	LSB
Differential nonlinearity	DNL		-0.5	0.5	LSB
Analog output					
Offset error		Mid-scale value (internal reference)	±0.05 typical		%FSR
Offset mismatch			±0.03 typical		%FSR
Gain error		With internal reference	±0.75 typical		%FSR
Minimum full scale output current 4/			2 typical		mA
Maximum full scale output current 4/			20 typical		mA
Gain Mismatch		With internal reference	-2	2	%FSR
Output voltage compliance range 5/			-0.8	1.25	V
Output resistance	R_O		300 typical		kΩ
Output capacitance	C_O		5 typical		pF
Reference Output					
Reference voltage			1.14	1.26	V
Reference output current 6/			100 typical		nA
Reference Input					
Input voltage	V_{EXTIO}		0.1	1.25	V
Input resistance	R_I		1 typical		MΩ
Small signal bandwidth			300 typical		kHz
Input capacitance	C_I		100 typical		pF
Temperature Coefficients					
Offset drift			2 typical		7/
Gain drift		With external reference	±20 typical		
		With internal reference	±40 typical		
Reference voltage drift			±20 typical		ppm/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 8/	Limits		Unit
			Min	Max	
Power Supply					
Analog supply voltage	AV_{DD}		3.0	3.6	V
Digital supply voltage	DV_{DD}		3.0	3.6	V
Supply current, analog	I_{AVDD}	Including output current through load resistor		90	mA
		Sleep mode with clock	2.5 typical		
		Sleep mode without clock	2.5 typical		
Supply current, digital	I_{DVDD}			20	mA
		Sleep mode with clock		18	
		Sleep mode without clock	0.6 typical		
Power dissipation				360	mW
		Sleep mode with clock	45.5 typical		
		Sleep mode without clock	9.2 typical		
		f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz	310 typical		
Analog power supply rejection ratio	APSRR		-0.2	0.2	%FSR/V
Digital power supply rejection ratio	DPSRR		-0.2	0.2	%FSR/V
Operating free air temperature	T_A		-55	125	°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 9/	Limits		Unit
			Min	Max	
Analog Output					
Maximum output update rate	f_{clk}		200		MSPS
Output settling time to 0.1% (DAC)	t_s	Mid scale transition	20 typical		ns
Output rise time 10% to 90% (OUT)	t_r		1.4 typical		ns
Output fall time 90% to 10% (OUT)	t_f		1.5 typical		ns
Output noise		I_{OUTFS} = 20 mA	55 typical		pA/$\sqrt{\text{Hz}}$
		I_{OUTFS} = 2 mA	30 typical		
AC Linearity					
Spurious free dynamic range	SFDR	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = 0 dB	79 typical		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = -6 dB	78 typical		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = -12 dB	73 typical		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB	80 typical		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	76 typical		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	61		
		1st Nyquist zone, T_A = -55°C to 125°C, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	58		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz, I_{OUTFS} = 0 dB	67 typical		
Signal to noise ratio	SNR	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB	63 typical		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	62 typical		
Third order two tone intermodulation	IMD3	Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz	61 typical		dBc
		Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz	78 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
AC Linearity – continued. 9/					
Four tone intermodulation	IMD	Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz	76 typical		dBc
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 19, 19.1, 19.3, and 19.4 MHz	55 typical		
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72 MHz	70 typical		
Channel isolation		T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT}(CH1) = 20 MHz, f_{OUT}(CH2) = 21 MHz	90 typical		dBc
Digital Input 10/					
High level input voltage	V_{IH}		0.2	3.3	V
Low level input voltage	V_{IL}		0	0.8	V
High level input current	I_{IH}		±50 typical		µA
Low level input current	I_{IL}		±10 typical		µA
High level input current. GSET pin	$I_{IH(GSET)}$		7 typical		µA
Low level input current, . GSET pin	$I_{IL(GSET)}$		-80 typical		µA
High level input current. MODE pin	$I_{IH(MODE)}$		-30 typical		µA
Low level input current, . MODE pin	$I_{IL(MODE}$		-80 typical		µA
Input capacitance	C_I		5 typical		pF
		Switching Characteristics			
Timing-Dual Bus Mode 10/					
Input setup time	t_{su}		1		ns
Input hold time	t_h		1		ns
Input clock pulse high time	t_{LPH}		1 typical		ns
Clock latency 11/ (WRTA/B to outputs)	t_{LAT}		4	4	clk
Propagation delay time	t_{PD}		1.5 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
Timing- Single Bus Interleaved Mode 10/					
Input setup time	t_{su}		0.5 typical		ns
Input hold time	t_h		0.5 typical		ns
Clock latency (WRTA/B to outputs) 11/	t_{LAT}		4	4	clk
Propagation delay time	t_{PD}		1.5 typical		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, independent gain set mode (unless otherwise noted)

3/ Measured differentially through 50 Ω to AGND.

4/ Nominal full scale current, I_{OUTFS}, equal 32x the I_{BIAS} current.

5/ The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

6/ Use an external buffet amplifier with high impedance input to drive any external load.

7/ ppm of FSR/°C.

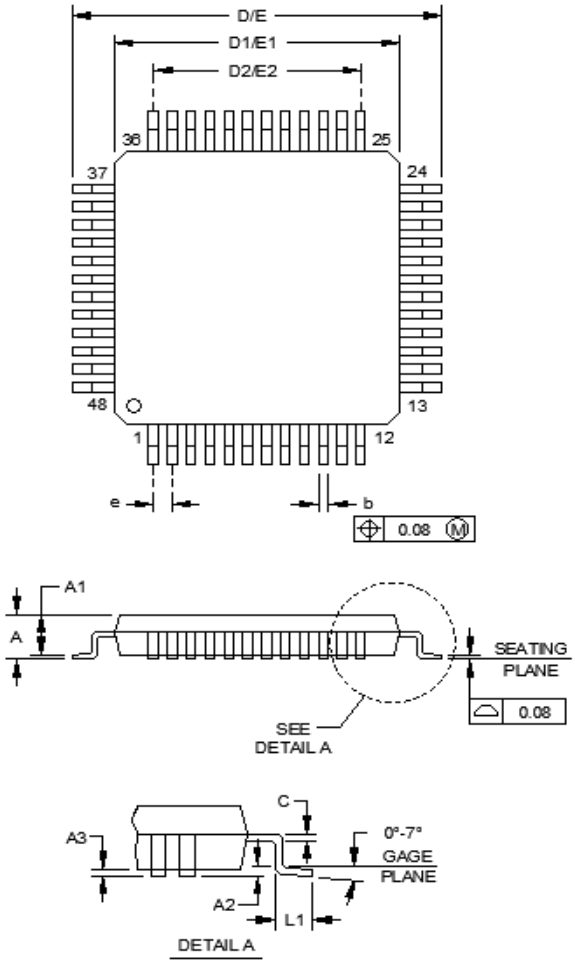
8/ Over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, $f_{DATA} = 200$ MSPS, $f_{OUT} = 1$ MHz, independent gain set mode (unless otherwise noted).

9/ AC specifications over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, independent gain set mode, differential 1:1 impedance ration transformer coupled output, 50 Ω doubly terminated load (unless otherwise noted).

10/ Digital specifications over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, (unless otherwise noted).

11/ Specified by design.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	8.80	9.20
A1	0.95	1.05	D1/E1	6.80	7.20
A2	0.25 Typ		D2/E2	5.50 Typ	
A3	0.05		e	0.50 NOM	
b	0.17	0.27	L1	0.45	0.75
c	0.13 NOM				

NOTES:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

Device types	01 and 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DA9(MSB)	25	DB7
2	DA8	26	DB6
3	DA7	27	DB5
4	DA6	28	DB4
5	DA5	29	DB3
6	DA4	30	DB2
7	DA3	31	DB1
8	DA2	32	DB0(LSB)
9	DA1	33	NC
10	DA0(LSB)	34	NC
11	NC	35	NC
12	NC	36	NC
13	NC	37	SLEEP
14	NC	38	AGND
15	DGND	39	IOUTB1
16	DVDD	40	IOUTB2
17	WRTA/WRTIQ	41	BIASJ_B
18	CLKA/CLKIQ	42	GSET
19	CLKB/RESETIQ	43	EXTIO
20	WRTB/SELECTIQ	44	BIASJ_A
21	DGND	45	IOUTA2
22	DVDD	46	IOUTA1
23	DB9(MSB)	47	AVDD
24	DB8	48	MODE

NC: Not connected

FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
AGND	I	Analog ground.
AVDD	I	Analog supply voltage.
BIASJ_A	O	Full-scale output current bias for DACA.
BIASJ_B	O	Full-scale output current bias for DACB.
CLKA/CLKIQ	I	Clock input for DACA, CLKIQ in interleaved mode.
CLKB/RESETIQ	I	Clock input for DACB, RESETIQ in interleaved mode.
DA[9:0]	I	Data port A. DA9 is MSB and DA0 is LSB.
DB[9:0]	I	Data port B. DB9 is MSB and DB0 is LSB.
DGND	I	Digital ground.
DVDD	I	Digital supply voltage.
EXTIO	I/O	Internal reference output (bypass with 0.1 µF to AGND) or external reference input.
GSET	I	Gain-setting mode: H = 1 resistor, L = 2 resistors. Internal pullup.
IOUTA1	O	DACA current output. Full scale with all bits of DA high.
IOUTA2	O	DACA complementary current output. Full scale with all bits of DA low.
IOUTB1	O	DACB current output. Full scale with all bits of DB high.
IOUTB2	O	DACB complementary current output. Full scale with all bits of DB low.
MODE	I	Mode select: H – dual bus, L – interleaved. Internal pullup.
NC		Factory use only. Pins must be connected to DGND or left unconnected.
SLEEP	I	Sleep function control input: H = DAC in power-down mode, L = DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	I	Input write signal for PORT A (WRTIQ in interleaving mode).
WRTB/SELECTIQ	I	Input write signal for PORT B (SELECTIQ in interleaving mode).

FIGURE 2. Terminal connections - Continued.

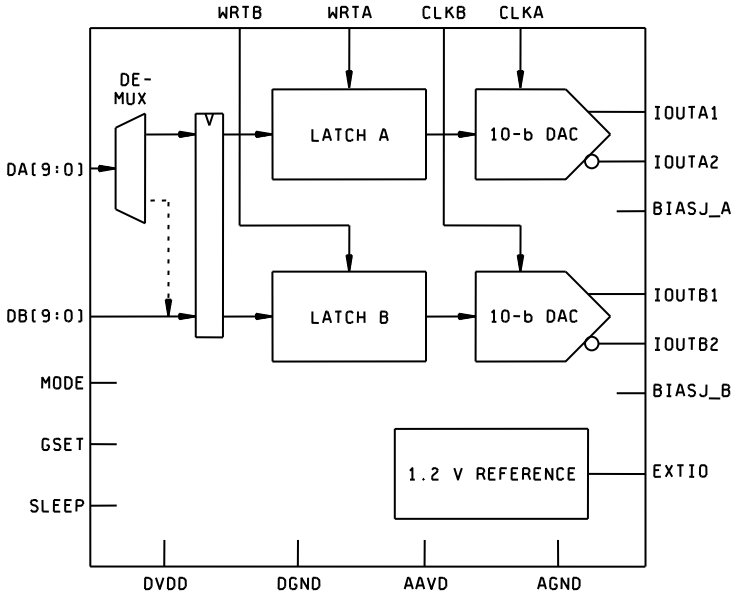


FIGURE 3. Functional block diagram.

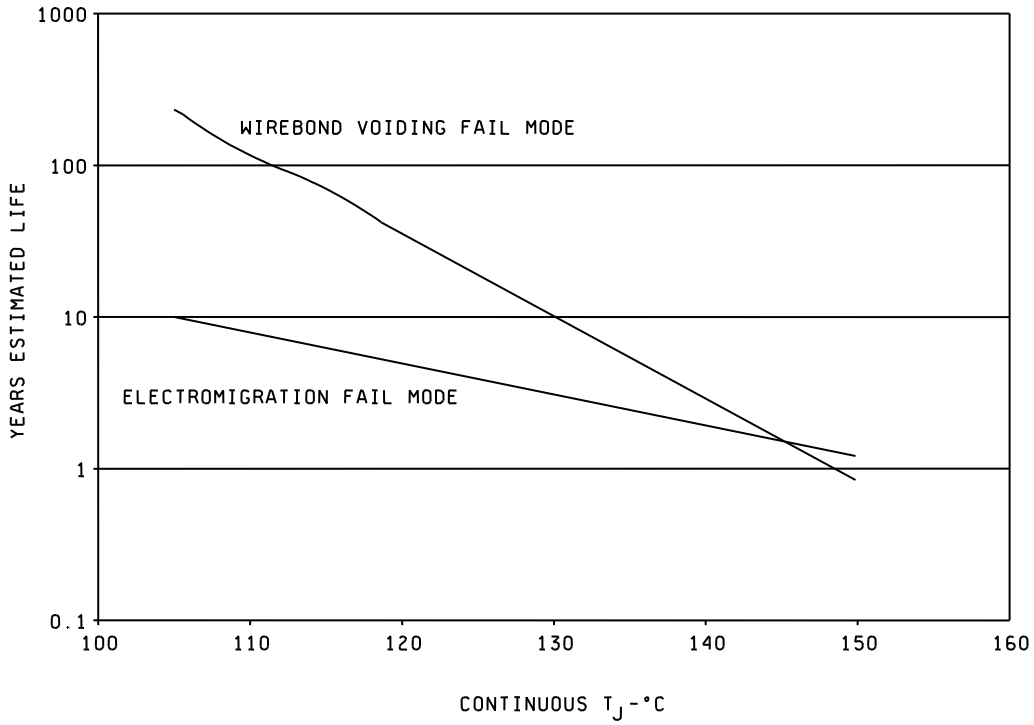


FIGURE 4. Operating life derating chart.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/06638-01XE	01295	Tape and reel, 1000	DAC5652EP	DAC5652MPFBREP
V62/06638-02XE	01295	Tape, 250	DAC5652EP	DAC5652MPFBEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243