REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 02. Update boilerplate to current revision. - CFS	06-12-15	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-01-27	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B					
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12					

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 06-07-12	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, DUAL 10-BIT 200 MSPS DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06638**
	REV B	**PAGE** 1 **OF** 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual 10-bit 200 MSPS digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06638	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DAC5652-EP	Dual 10-bit 200 MSPS digital to analog converter
02	DAC5652-EP	Dual 10-bit 200 MSPS digital to analog converter

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:

(AV_{DD}) ..... -0.5 V to 4.0 V 2/

(DV_{DD}) ..... -0.5 V to 4.0 V 3/

Voltage between AGND and DGND ..... -0.5 V to 0.5 V

Voltage between AV_{DD} and DV_{DD} ..... -0.5 V to 0.5 V

Supply voltage range:

DA[9:0] and DB[9:0] ..... -0.5 V to DV_{DD} + 0.5 V 3/

MODE, CLKA, CLKB, WRTA, WRTB ..... -0.5 V to DV_{DD} + 0.5 V 3/

IOUTA1, IOUTA2, IOUTB1, IOUTB2 ..... -1.0 V to AV_{DD} + 0.5 V 2/

EXTIO, BIASJ_A, BIASJ_B, SLEEP ..... -0.5 V to AV_{DD} + 0.5 V 2/

Peak input current (any input) ..... 20 mA

Peak total input current (all inputs) ..... -30 mA

Operating free-air temperature range (T_A) ..... -55°C to +125°C

Storage temperature range (T_{STG}) ..... -65°C to 150°C

Lead temperature (1.6 mm (1/16 in) from the case for 10 s) ..... 260°C

Junction temperature (T_J) ..... 105°C 4/

Junction to ambient temperature (θ_{JA}): 5/

Still air ..... 19.88°C/W

150 lfm ..... 14.37°C/W

Junction to case temperature (θ_{JC}) ..... 0.12°C/W

Package thermal characteristics, case X:

Parameter	Powerpad connected to PCB thermal plane
Thermal resistance, junction to ambient	63.7°C/W
Thermal resistance, junction to case	19.6°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Measured with respect to AGND.

3/ Measured with respect to DGND.

4/ Airflow or heatsinking required for sustained operation at 85°C and maximum operating conditions to maintain junction temperature.

5/ Airflow or heatsinking reduces θ_{JA} and is highly recommended.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating life derating chart. The operating life derating chart shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
DC Specifications					
Resolution			10		Bits
DC Accuracy 3/					
Integral nonlinearity	INL	1 LSB = $I_{OUTFS}/2^{10}$, T_{MIN} to T_{MAX}	-1	1	LSB
Differential nonlinearity	DNL		-0.5	0.5	
Analog output					
Offset error		Mid-scale value (internal reference)	±0.05 Typ		%FSR
Offset mismatch			±0.03 Typ		
Gain error		With internal reference	±0.75 Typ		
Minimum full scale output current 4/			2 Typ		mA
Maximum full scale output current 4/			20 Typ		
Gain Mismatch		With internal reference	-2	2	%FSR
Output voltage compliance range 5/			-0.8	1.25	
Output resistance	R_O		300 Typ		kΩ
Output capacitance	C_O		5 Typ		pF
Reference Output					
Reference voltage			1.14	1.26	V
Reference output current 6/			100 Typ		nA
Reference Input					
Input voltage	V_{EXTIO}		0.1	1.25	V
Input resistance	R_I		1 Typ		MΩ
Small signal bandwidth			300 Typ		kHz
Input capacitance	C_I		100 Typ		pF
Temperature Coefficients					
Offset drift			2 Typ		7/
Gain drift		With external reference	±20 Typ		
		With internal reference	±40 Typ		
Reference voltage drift			±20 Typ		ppm/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 8/	Limits		Unit
			Min	Max	
Power Supply					
Analog supply voltage	AV_{DD}		3.0	3.6	V
Digital supply voltage	DV_{DD}		3.0	3.6	
Supply current, analog	I_{AVDD}	Including output current through load resistor		90	mA
		Sleep mode with clock	2.5 Typ		
		Sleep mode without clock	2.5 Typ		
Supply current, digital	I_{DVDD}			20	
		Sleep mode with clock		18	
		Sleep mode without clock	0.6 Typ		
Power dissipation				360	mW
		Sleep mode with clock	45.5 Typ		
		Sleep mode without clock	9.2 Typ		
		f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz	310 Typ		
Analog power supply rejection ratio	APSRR		-0.2	0.2	%FSR/V
Digital power supply rejection ratio	DPSRR		-0.2	0.2	
Operating free air temperature	T_A		-55	125	°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 9/	Limits Min	Limits Max	Unit
Analog Output					
Maximum output update rate	f_{clk}		200		MSPS
Output settling time to 0.1% (DAC)	t_s	Mid scale transition	20 Typ		ns
Output rise time 10% to 90% (OUT)	t_r		1.4 Typ		
Output fall time 90% to 10% (OUT)	t_f		1.5 Typ		
Output noise		I_{OUTFS} = 20 mA	55 Typ		pA/√Hz
		I_{OUTFS} = 2 mA	30 Typ		
AC Linearity					
Spurious free dynamic range	SFDR	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = 0 dB	79 Typ		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = -6 dB	78 Typ		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = -12 dB	73 Typ		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB	80 Typ		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	76 Typ		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	61		
		1st Nyquist zone, T_A = -55°C to 125°C, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	58		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz, I_{OUTFS} = 0 dB	67 Typ		
Signal to noise ratio	SNR	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB	63 Typ		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	62 Typ		
Third order two tone intermodulation	IMD3	Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz	61 Typ		dBc
		Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz	78 Typ		
Four tone intermodulation	IMD	Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz	76 Typ		dBc
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 19, 19.1, 19.3, and 19.4 MHz	55 Typ		
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72 MHz	70 Typ		
Channel isolation		T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT}(CH1) = 20 MHz, f_{OUT}(CH2) = 21 MHz	90 Typ		dBc

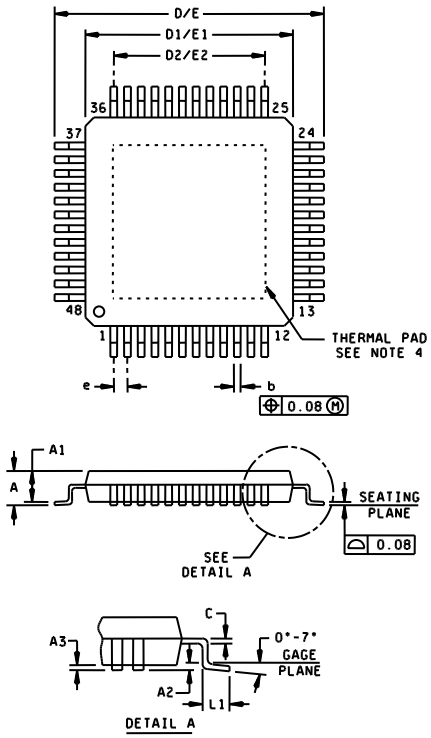
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 10/	Limits		Unit
			Min	Max	
Digital Input					
High level input voltage	V_{IH}		0.2	3.3	V
Low level input voltage	V_{IL}		0	0.8	
High level input current	I_{IH}		±50 Typ		µA
Low level input current	I_{IL}		±10 Typ		
High level input current. GSET pin	$I_{IH(GSET)}$		7 Typ		
Low level input current, . GSET pin	$I_{IL(GSET)}$		-80 Typ		
High level input current. MODE pin	$I_{IH(MODE)}$		-30 Typ		
Low level input current, . MODE pin	$I_{IL(MODE}$		-80 Typ		
Input capacitance	C_I		5 Typ		pF
Switching Characteristics					
Timing-Dual Bus Mode					
Input setup time	t_{su}		1		ns
Input hold time	t_h		1		
Input clock pulse high time	t_{LPH}		1 Typ		
Clock latency (WRTA/B to outputs) 11/	t_{LAT}		4	4	clk
Propagation delay time	t_{PD}		1.5 Typ		ns
Timing- Single Bus Interleaved Mode					
Input setup time	t_{su}		0.5 Typ		ns
Input hold time	t_h		0.5 Typ		
Clock latency (WRTA/B to outputs) 11/	t_{LAT}		4	4	clk
Propagation delay time	t_{PD}		1.5 Typ		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, independent gain set mode (unless otherwise noted)
3/ Measured differentially through 50 Ω to AGND.
4/ Nominal full scale current, I_{OUTFS}, equal 32x the I_{BIAS} current.
5/ The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
6/ Use an external buffet amplifier with high impedance input to drive any external load.
7/ ppm of FSR/°C
8/ Over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, $f_{DATA} = 200$ MSPS, $f_{OUT} = 1$ MHz, independent gain set mode (unless otherwise noted)
9/ AC specifications over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, independent gain set mode, differential 1:1impedance ration transformer coupled output, 50 Ω doubly terminated load (unless otherwise noted).
10/ Digital specifications over operating free air temperature range, $AV_{DD} = DV_{DD} = 3.3$ V, $I_{OUTFS} = 20$ mA, (unless otherwise noted).
11/ Specified by design.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	8.80	9.20
A1	0.95	1.05	D1/E1	6.80	7.20
A2	0.25 Typ		D2/E2	5.50 Typ	
A3	0.05		e	0.50 NOM	
b	0.17	0.27	L1	0.45	0.75
c	0.13 NOM				

NOTES:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DA9(MSB)	13	NC	25	DB7	37	SLEEP
2	DA8	14	NC	26	DB6	38	AGND
3	DA7	15	DGND	27	DB5	39	IOUTB1
4	DA6	16	DVDD	28	DB4	40	IOUTB2
5	DA5	17	WRTA/WRTIQ	29	DB3	41	BIASJ_B
6	DA4	18	CLKA/CLKIQ	30	DB2	42	GSET
7	DA3	19	CLKB/RESETIQ	31	DB1	43	EXTIO
8	DA2	20	WRTB/SELECTIQ	32	DB0(LSB)	44	BIASJ_A
9	DA1	21	DGND	33	NC	45	IOUTA2
10	DA0(LSB)	22	DVDD	34	NC	46	IOUTA1
11	NC	23	DB9(MSB)	35	NC	47	AVDD
12	NC	24	DB8	36	NC	48	MODE

NC: Not connected

FIGURE 2. Terminal connections.

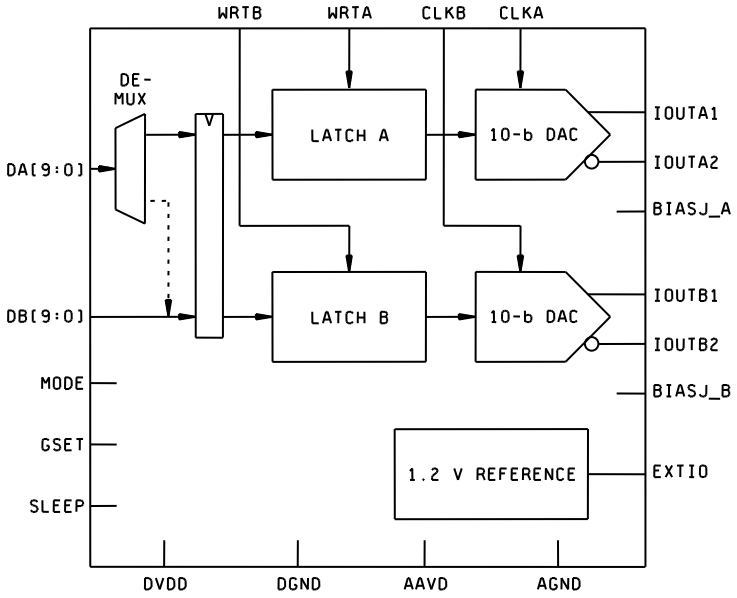


FIGURE 3. Functional block diagram.

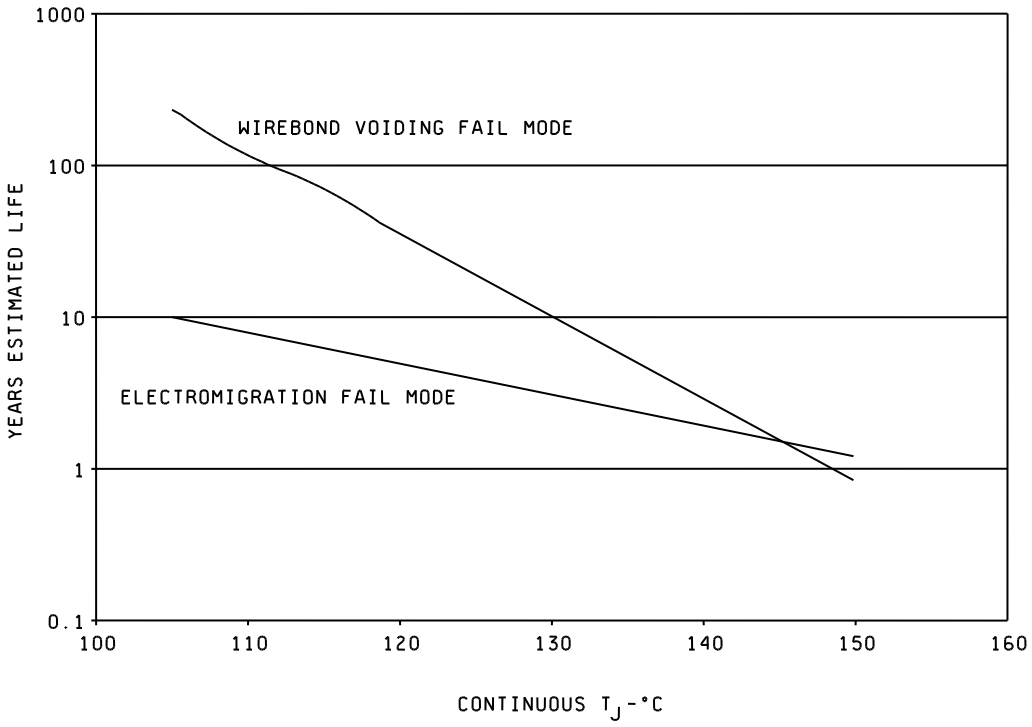


FIGURE 4. Operating life derating chart.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/06638-01XE	01295	DAC5652MPFBREP
V62/06638-02XE	01295	DAC5652MPFBEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493