REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. ro	14-09-24	C. SAFFLE
B	Under Table I, Auto powerdown section, V_{OL} test conditions column, delete I_{OH} and replace with I_{OL}. Update document paragraphs to current requirements. - ro	20-05-20	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B																				
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-10-03	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 3 V TO 5.5 V MULTICHANNEL RS-232 LINE DRIVER / RECEIVER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06635**
	REV B	**PAGE** 1 **OF** 18

AMSC N/A

5962-V024-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3 V to 5.5 V multichannel RS-232 line driver / receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06635	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MAX3223-EP	3 V to 5.5 V multichannel RS-232 line driver / receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-150	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.3 V to 6 V
Positive output supply voltage range (V+) ..... -0.3 V to 7 V 2/
Negative output supply voltage range (V-) ..... 0.3 V to -7 V 2/
Supply voltage difference (V+ - V-) ..... 13 V 2/
Input voltage range (V_I):
Driver ($\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$) ..... -0.3 V to 6 V
Receiver ..... -25 V to 25 V
Output voltage range (V_O):
Driver ..... -13.2 V to 13.2 V
Receiver ($\overline{\text{INVALID}}$) ..... -0.3 V to V_{CC} + 0.3 V
Package thermal impedance (θ_{JA}): 3/ 4/
Case X ..... 70°C/W
Operating virtual junction temperature (T_J) ..... +150°C
Storage temperature range (T_{stg}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range (V_{CC}):
V_{CC} = 3.3 V ..... 3 V to 3.6 V
V_{CC} = 5 V ..... 4.5 V to 5.5 V
Driver and control high level input voltage (V_{IH}) at DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$ pins :
V_{CC} = 3.3 V ..... 2 V minimum
V_{CC} = 5 V ..... 2.4 V minimum
Driver and control low level input voltage (V_{IL}) at DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$ pins ..... 0.8 V maximum
Driver and control input voltage (V_I) at DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$ pins ..... 0 V to 5.5 V
Receiver input voltage (V_I) ..... -25 V to 25 V
Operating free air temperature (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are with respect to network GND.
3/ Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ±0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} 5 V ±0.5 V. See figure 6.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

3.5.6 Typical operating circuit. The typical operating circuit shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input leakage current $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	I_I	See figure 6	-55°C to +125°C	01		±1	µA
Supply current, auto powerdown disabled	I_{CC}	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}, see figure 6, V_{CC} = 3.3 V or 5 V	+25°C	01		2	mA
Supply current, powered off	I_{CC}	No load, $\overline{\text{FORCEOFF}}$ at GND, V_{CC} = 3.3 V or 5 V, see figure 6	+25°C	01		20	µA
Supply current, auto powerdown enabled	I_{CC}	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, all RIN are open or grounded, V_{CC} = 3.3 V or 5 V, see figure 6	+25°C	01		20	µA
Driver section		(see figure 6)					
High level output voltage	V_{OH}	DOUT at R_L = 3 kΩ to GND	-55°C to +125°C	01	5		V
Low level output voltage	V_{OL}	DOUT at R_L = 3 kΩ to GND, V_{CC} = 5 V	-55°C to +125°C	01	-5		V
		DOUT at R_L = 3 kΩ to GND, V_{CC} = 3.3 V			-4.9 3/		
High level input current	I_{IH}	$V_I = V_{CC}$	-55°C to +125°C	01		±1	µA
Low level input current	I_{IL}	V_I at GND	-55°C to +125°C	01		±1	µA
Short circuit output 4/ current	I_{OS}	V_{CC} = 3.6 V, V_O = 0 V	-55°C to +125°C	01		±60	mA
		V_{CC} = 5.5 V, V_O = 0 V				±60	
Output resistance	r_o	V_{CC}, V+, and V- = 0 V, V_O = ±2 V	-55°C to +125°C	01	300		Ω
Output leakage current	I_{OZ}	V_O = ±12 V, V_{CC} = 3 V to 3.6 V, $\overline{\text{FORCEOFF}}$ = GND	-55°C to +125°C	01		±25	µA
		V_O = ±10 V, V_{CC} = 4.5 V to 5.5 V, $\overline{\text{FORCEOFF}}$ = GND				±25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section switching characteristics (see figure 6)							
Maximum data rate		C_L = 1000 pF, R_L = 3 kΩ, one DOUT switching, see figure 5	-55°C to +125°C	01	250		kbits/s
Pulse skew 5/	$t_{sk(p)}$	C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, see figure 5	+25°C	01	100 typical 6/		ns
Slew rate, transition region (see figure 5)	SR(tr)	V_{CC} = 3.3 V, C_L = 150 pF to 1000 pF, R_L = 3 kΩ to 7 kΩ	-55°C to +125°C	01	6	30	V/μs
		V_{CC} = 3.3 V, C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ			4	30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver section		(see figure 6)					
High level output voltage	V_{OH}	I_{OH} = -1 mA	-55°C to +125°C	01	V_{CC} – 0.6		V
Low level output voltage	V_{OL}	I_{OL} = 1.6 mA	-55°C to +125°C	01		0.4	V
Positive going input threshold voltage	V_{IT+}	V_{CC} = 3.3 V	-55°C to +125°C	01		2.4	V
		V_{CC} = 5 V				2.4	
Negative going input threshold voltage	V_{IT-}	V_{CC} = 3.3 V	-55°C to +125°C	01	0.6		V
		V_{CC} = 5 V			0.8		
Input hysteresis (V_{IT+} - V_{IT-})	V_{hys}		+25°C	01	0.5 typical 6/		V
Output leakage current	I_{OZ}	$\overline{EN}$ = V_{CC}	-55°C to +125°C	01		±10	µA
Input resistance	r_i	V_I = ±3 V or ±16 V	-55°C to +125°C	01	3	8.3	kΩ
Switching characteristics section							
Propagation delay time, low to high level output	t_{PLH}	C_L = 150 pF, see figure 5	+25°C	01	150 typical 6/		ns
Propagation delay time, high to low level output	t_{PHL}	C_L = 150 pF, see figure 5	+25°C	01	150 typical 6/		ns
Output enable time	t_{en}	C_L = 150 pF, R_L = 3 kΩ, see figure 5	+25°C	01	200 typical 6/		ns
Output disable time	t_{dis}	C_L = 150 pF, R_L = 3 kΩ, see figure 5	+25°C	01	200 typical 6/		ns
Pulse skew 5/	$t_{sk(p)}$	See figure 5	+25°C	01	50 typical 6/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Auto powerdown section		(see figure 5)					
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	$V_{IT+(valid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	-55°C to +125°C	01		2.7	V
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	$V_{IT-(valid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	-55°C to +125°C	01	-2.7		V
Receiver input threshold for $\overline{\text{INVALID}}$ low level output voltage	$V_{T(invalid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	-55°C to +125°C	01	-0.2	0.3	V
$\overline{\text{INVALID}}$ high level output voltage	V_{OH}	I_{OH} = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	-55°C to +125°C	01	V_{CC} – 0.6		V
$\overline{\text{INVALID}}$ low level output voltage	V_{OL}	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	-55°C to +125°C	01		0.4	V
Switching characteristics section		(see figure 5)					
Propagation delay time, low to high level output	t_{valid}		+25°C	01	1 typical 6/		µs
Propagation delay time, high to low level output	$t_{invalid}$		+25°C	01	30 typical 6/		µs
Supply enable time	t_{en}		+25°C	01	100 typical 6/		µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Test conditions are C1 - C4 = 0.1 µF at V_{CC} = 3.3 V ±0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ±0.5 V.

3/ The minimum reading of -4.9 V at V_{CC} = 3.3 V fall outside the TIA/EIA-232 standard.

4/ Short circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5/ Pulse skew is defined as | t_{PLH} – t_{PHL} | of each channel of the same device.

6/ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = +25°C.

Case X

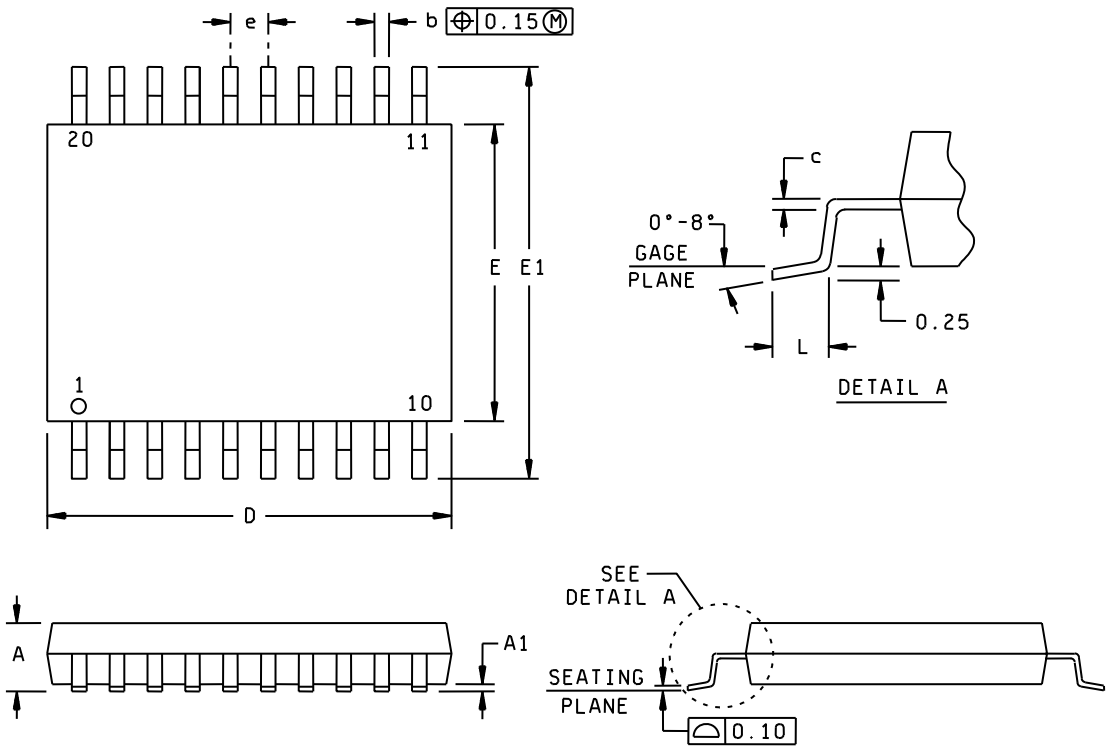

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/06635
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.078	---	2.00
A1	.001	---	0.05	---
b	.008	.014	0.22	0.38
c	.003	.009	0.09	0.25
D	.271	.295	6.90	7.50
E	.196	.220	5.00	5.60
E1	.291	.322	7.40	8.20
e	.025 BSC		0.65 BSC	
L	.021	.037	0.55	0.95

NOTES:
1. All linear dimensions are in millimeters, inch equivalents are given for general information only.
2. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeter (.006 inch).
3. Fall within JEDEC MO-150.

FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$\overline{EN}$
2	C1+
3	V+
4	C1-
5	C2+
6	C2-
7	V-
8	DOUT2
9	RIN2
10	ROUT2
11	$\overline{INVALID}$
12	DIN2
13	DIN1
14	FORCEON
15	ROUT1
16	RIN1
17	DOUT1
18	GND
19	V_{CC}
20	$\overline{FORCEOFF}$

FIGURE 2. Terminal connections.

Each driver

Inputs				Output	Driver status
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	Valid RIN RS-232 level	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto powerdown disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with auto powerdown enabled
H	L	H	YES	L	
L	L	H	NO	Z	Power off by auto powerdown feature
H	L	H	NO	Z	

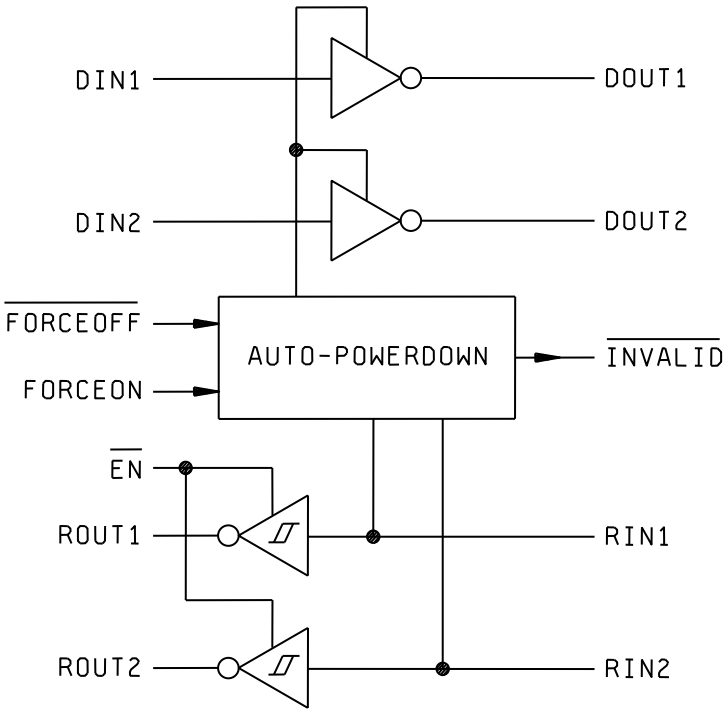
H = High level
L = Low level
X = Irrelevant
Z = High impedance

Each receiver

Inputs			Output
RIN	$\overline{\text{EN}}$	Valid RIN RS-232 level	ROUT
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

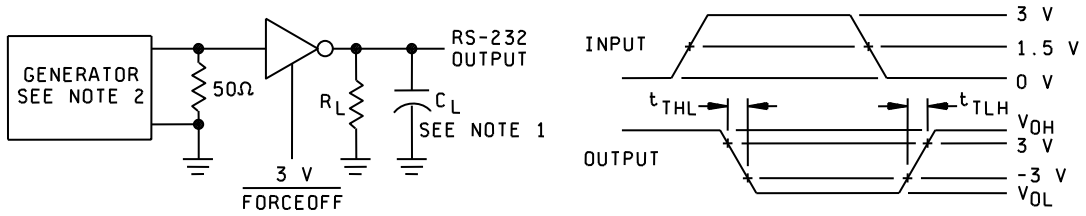
H = High level
L = Low level
X = Irrelevant
Z = High impedance (off)
Open = Disconnected input or connected driver off

FIGURE 3. Truth table.



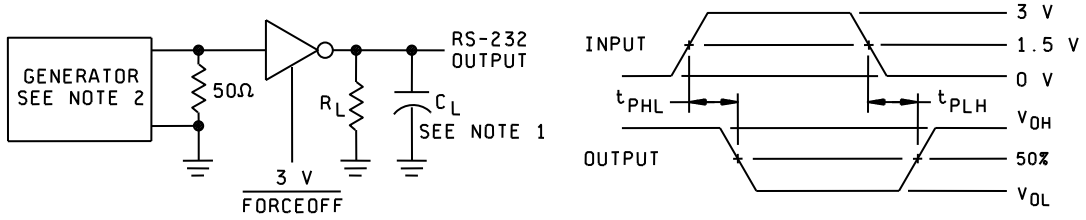
(Positive logic)

FIGURE 4. Logic diagram.



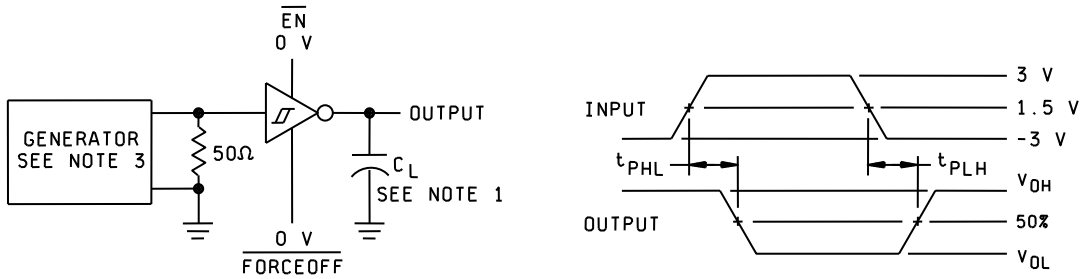
TEST CIRCUIT VOLTAGE WAVEFORMS

DRIVER SLEW RATE



TEST CIRCUIT VOLTAGE WAVEFORMS

DRIVER PULSE SKEW



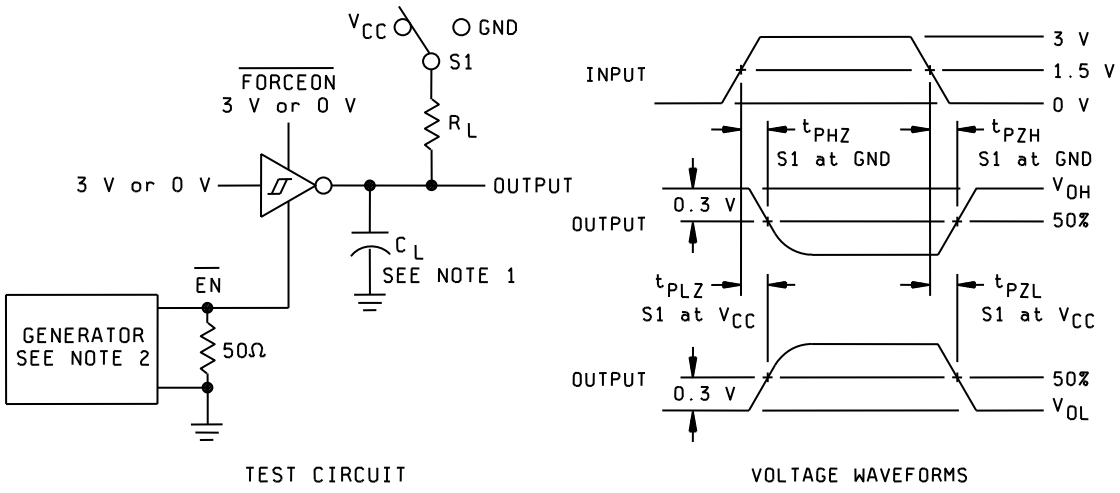
TEST CIRCUIT VOLTAGE WAVEFORMS

RECEIVER PROPAGATION DELAY TIMES

NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
3. The pulse generator has the following characteristics: Z_O = 50 Ω, 50 % duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 5. Timing waveforms and test circuit.



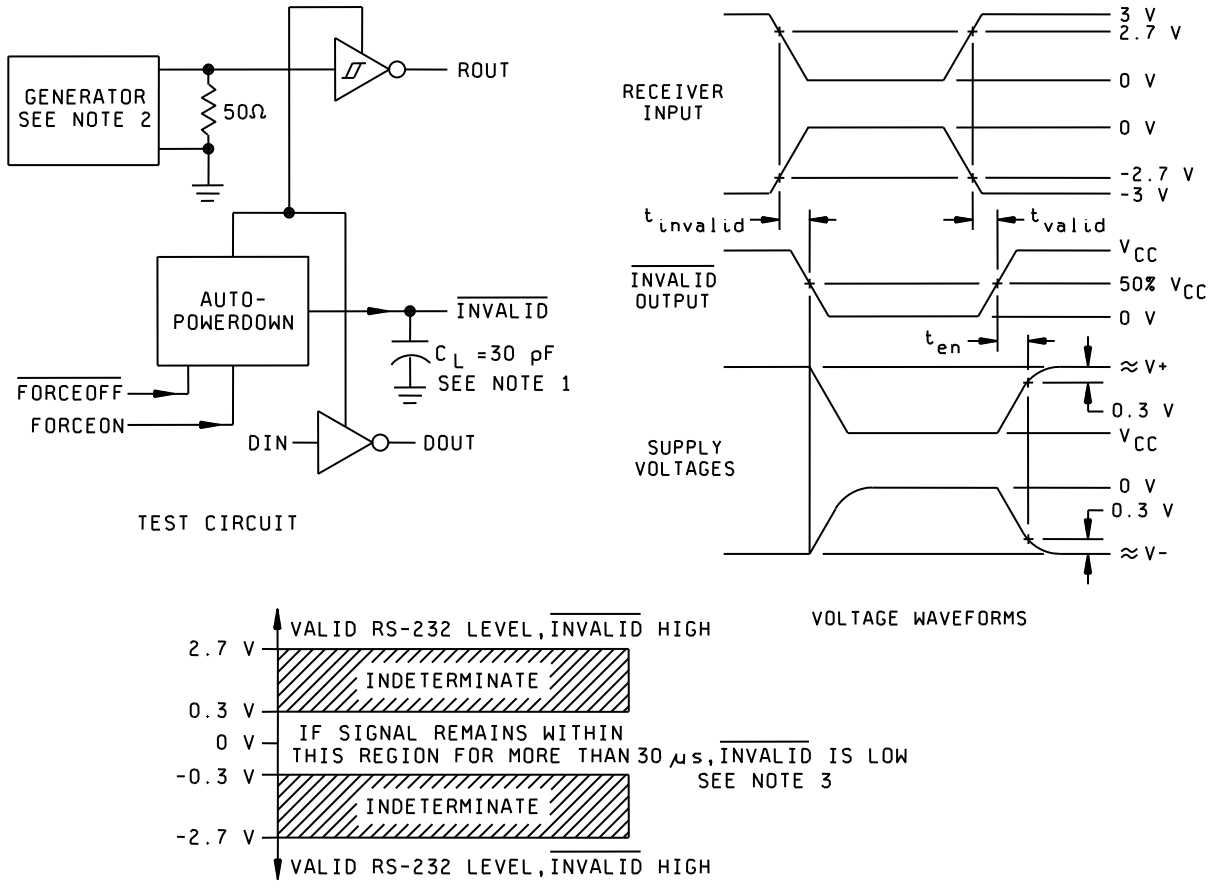
TEST CIRCUIT VOLTAGE WAVEFORMS

RECEIVER ENABLE AND DISABLE TIMES

NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: Z_O = 50 Ω, 50 % duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
4. t_{PZL} and t_{PZH} are the same as t_{en}.

FIGURE 5. Timing waveforms and test circuit – Continued.

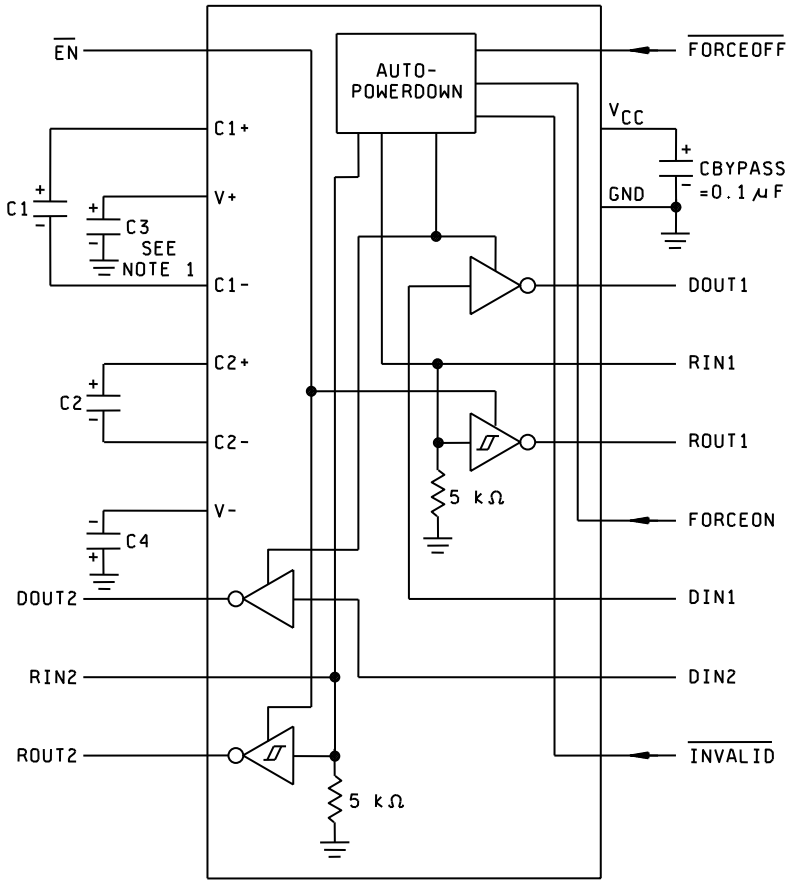


INVALID propagation delay times and supply enabling time

NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
3. Auto powerdown disables drivers and reduces supply current to 1 µA.

FIGURE 5. Timing waveforms and test circuit – Continued.



NOTES:

1. C3 can be connected to V_{CC} or GND.
2. Resistor values shown are nominal.
3. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} versus capacitor values		
V_{CC}	C1	C2, C3, C4
3.3 V ±0.3 V	0.1 µF	0.1 µF
5 V ±0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

FIGURE 6. Typical operating circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity 2/	Top side marking	Vendor part number
V62/06635-01XE	01295	Reel of 2000	MB223M	MAX3223MDBREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243