REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add a note to figure 1 for both case outlines X and Y. Add JEDEC references to paragraph 2. Update document paragraph to current requirements. - ro	14-08-06	C. SAFFLE
B	Make change to both c dimension minimum limits as specified in Figure 1. Delete last sentence in note 3 under case outline X as specified under Figure 1. Update document paragraph to current requirements. - ro	21-04-08	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																		
PAGE																		
REV	B	B	B	B	B	B	B	B										
PAGE	18	19	20	21	22	23	24	25										

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-10-10	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 3.3 V, FULL DUPLEX RS-485 DRIVERS AND RECEIVERS, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/06634
	REV B	**PAGE** 1 **OF** 25

AMSC N/A

5962-V015-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3 V, full duplex RS-485 drivers and receivers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06634	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Signaling rate	Circuit function
01	SN65HVD30-EP	25 Mpbs	3.3 V full duplex RS-485 drivers and receivers
02	SN65HVD31-EP	5 Mpbs	3.3 V full duplex RS-485 drivers and receivers
03	SN65HVD32-EP	1 Mpbs	3.3 V full duplex RS-485 drivers and receivers
04	SN65HVD33-EP	25 Mpbs	3.3 V full duplex RS-485 drivers and receivers
05	SN65HVD34-EP	5 Mpbs	3.3 V full duplex RS-485 drivers and receivers
06	SN65HVD35-EP	1 Mpbs	3.3 V full duplex RS-485 drivers and receivers
07	SN65HVD36-EP	25 Mpbs	3.3 V full duplex RS-485 drivers and receivers
08	SN65HVD37-EP	5 Mpbs	3.3 V full duplex RS-485 drivers and receivers
09	SN65HVD38-EP	25 Mpbs	3.3 V full duplex RS-485 drivers and receivers
10	SN65HVD39-EP	5 Mpbs	3.3 V full duplex RS-485 drivers and receivers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline
Y	14	MS-012-AB	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.3 V to 6 V
Voltage range at any bus terminal (A, B, Y, Z pins) (V_A, V_B, V_Y, V_Z)	-9 V to 14 V
Voltage input, transient pulse through 100 Ω (A, B, Y, Z pins) (V_{TRANS})	-50 V to +50 V 3/
Input voltage range (D, DE, $\overline{RE}$ pins) (V_I)	-0.5 V to 7 V
Continuous total power dissipation (P_D)	Internally limited 4/
Output current (receiver output only, R pin) (I_O)	11 mA
Junction temperature range (T_J)	+165°C
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	3 V to 3.6 V
Voltage at any bus terminal (separately or common mode) (V_I or V_{IC})	-7 V to 12 V 6/
Signaling rate ($1/t_{UI}$):	
Device types 01, 04, 07, 09	25 Mbps maximum
Device types 02, 05, 08, 10	5 Mbps maximum
Device types 03, 06	1 Mbps maximum
Differential load resistance (R_L)	54 Ω
High level input voltage (V_{IH}) (D, DE, $\overline{RE}$ pins)	2 V to V_{CC}
Low level input voltage (V_{IL}) (D, DE, $\overline{RE}$ pins)	0 V to 0.8 V
Differential input voltage	-12 V to 12 V
High level output current (I_{OH}):	
Driver	-60 mA minimum
Receiver	-8 mA minimum
Low level output current (I_{OL}):	
Driver	60 mA maximum
Receiver	8 mA maximum
Operating free-air temperature range (T_A)	-55°C to +125°C 7/
Electrostatic discharge protection: 8/	
Human body model (HBM) (Bus terminals and GND)	±16 kV typical
Human body model (HBM) (all pins)	±4 kV typical 9/
Charged device model (CDM) (all pins)	±1 kV typical 10/

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ This tests survivability only and the output state of the receiver is not specified.
4/ The thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C. See device power dissipation section under Table I.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
7/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer for additional information on enhanced plastic packaging.
8/ All typical values at 25°C with 3.3 V supply.
9/ Tested in accordance with JEDEC standard 22, test method A114-A.
10/ Tested in accordance with JEDEC standard 22, test method C101.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	–	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 5 through 15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Driver electrical characteristics section							
Input clamp voltage	$V_{I(K)}$	I_I = -18 mA	-55°C to +125°C	All	-1.5		V
Steady state differential output voltage	$\|V_{OD(SS)}\|$	I_O = 0	-55°C to +125°C	All	2.3	V_{CC} + 0.1	V
		R_L = 54 Ω, see figure 5 (RS-485)			1.5		
		R_L = 100 Ω, see figure 5 (RS-422)			2		
		V_{test} = -7 V to 12 V, see figure 6			1.5		
Change in magnitude of steady state differential output voltage between states	$\Delta\|V_{OD(SS)}\|$	See figure 5 and figure 6, R_L = 54 Ω	-55°C to +125°C	All	-0.2	0.2	V
Differential output voltage overshoot and undershoot	$V_{OD(RING)}$	See figure 7 and figure 8, R_L = 54 Ω, C_L = 50 pF	-55°C to +125°C	All		10% 2/	V
Peak-to-peak common mode output voltage	$V_{OC(PP)}$	See figure 9	+25°C	01, 04, 07, 09	0.5 typical 3/		V
				02, 03, 05, 06, 08, 10	0.25 typical 3/		
Steady state common mode output voltage	$V_{OC(SS)}$	See figure 9	-55°C to +125°C	All	1.6	2.3	V
Change in steady state common mode output voltage	$\Delta V_{OC(SS)}$	See figure 9	-55°C to +125°C	All	-0.05	0.05	V
High impedance state output current	$I_{Z(Z)}$ or $I_{Y(Z)}$	V_{CC} = 0 V, V_Z or V_Y = 12 V, other input at 0 V	-55°C to +125°C	01, 02, 03, 07, 08		90	µA
		V_{CC} = 0 V, V_Z or V_Y = -7 V, other input at 0 V			-10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Driver electrical characteristics section - continued							
High impedance state output current	$I_{Z(Z)}$ or $I_{Y(Z)}$	V_{CC} = 3 V or 0 V, DE = 0 V, V_Z or V_Y = 12 V, other input at 0 V	-55°C to +125°C	04, 05, 06, 09, 10		90	μA
		V_{CC} = 3 V or 0 V, DE = 0 V, V_Z or V_Y = -7 V, other input at 0 V			-10		
Short circuit output current	$I_{Z(S)}$ or $I_{Y(S)}$	V_Z or V_Y = -7 V, other input at 0 V	+25°C	All	±250 typical 3/		mA
		V_Z or V_Y = 12 V, other input at 0 V			±250 typical 3/		
Input current (D, DE pins)	I_I		-55°C to +125°C	All	0	100	μA
Differential output capacitance	$C_{(OD)}$	V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V	25°C	All	16 typical 3/		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Driver switching characteristics section							
Propagation delay time, low to high level output	t_{PLH}	See figure 7, R_L = 54 Ω, C_L = 50 pF	-55°C to +125°C	01, 04, 07, 09	4	23	ns
				02, 05, 08, 10	25	65	
				03, 06	120	305	
Propagation delay time, high to low level output	t_{PHL}	See figure 7, R_L = 54 Ω, C_L = 50 pF	-55°C to +125°C	01, 04, 07, 09	4	23	ns
				02, 05, 08, 10	25	65	
				03, 06	120	305	
Differential output signal rise time	t_r	See figure 7, R_L = 54 Ω, C_L = 50 pF	-55°C to +125°C	01, 04, 07, 09	2.5	18	ns
				02, 05, 08, 10	20	60	
				03, 06	120	300	
Differential output signal fall time	t_f	See figure 7, R_L = 54 Ω, C_L = 50 pF	-55°C to +125°C	01, 04, 07, 09	2.5	18	ns
				02, 05, 08, 10	20	60	
				03, 06	120	300	
Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	$t_{sk(p)}$	See figure 7, R_L = 54 Ω, C_L = 50 pF	+25°C	01, 04, 07, 09	0.6 typical 3/		ns
				02, 05, 08, 10	2.0 typical 3/		
				03, 06	5.1 typical 3/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section - continued							
Propagation delay time, high impedance to high level output	t_{PZH1}	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z, see figure 10	-55°C to +125°C	04, 09		45	ns
				05, 10		235	
				06		490	
Propagation delay time, high level to high impedance output	t_{PHZ}	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z, see figure 10	-55°C to +125°C	04, 09		25	ns
				05, 10		65	
				06		165	
Propagation delay time, high impedance to low level output	t_{PZL1}	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y, see figure 11	-55°C to +125°C	04, 09		35	ns
				05, 10		190	
				06		490	
Propagation delay time, low level to high impedance output	t_{PLZ}	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y, see figure 11	-55°C to +125°C	04, 09		30	ns
				05, 10		120	
				06		290	
Propagation delay time, standby to high level output	t_{PZH2}	R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z, see figure 10	-55°C to +125°C	01-03, 05-09		4000	ns
				04		5000	
Propagation delay time, standby to low level output	t_{PZL2}	R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y, see figure 11	-55°C to +125°C	01-03, 05-09		4000	ns
				04		5000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Receiver electrical characteristics							
Positive going differential input threshold voltage	V_{IT+}	I_O = -8 mA	-55°C to +125°C	All		-0.02	V
Negative going differential input threshold voltage	V_{IT-}	I_O = 8 mA	-55°C to +125°C	01-03, 05-09	-0.15		V
				04	-0.2		
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{hys}		+25°C	All	50 typical 3/		mV
Enable input clamp voltage	V_{IK}	I_I = -18 mA	-55°C to +125°C	All	-1.5		V
Output voltage	V_O	V_{ID} = 200 mV, I_O = -8 mA, see figure 12	-55°C to +125°C	All	2.4		V
		V_{ID} = -200 mV, I_O = 8 mA, see figure 12				0.4	
High impedance state output current	$I_{O(Z)}$	V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}	-55°C to +125°C	All	-1	1	μA
Bus input current	I_A or I_B	V_A or V_B = 12 V, other input at 0 V	-55°C to +125°C	02, 03, 05, 06, 08, 10		0.1	mA
		V_A or V_B = 12 V, V_{CC} = 0 V, other input at 0 V				0.1	
		V_A or V_B = -7 V, other input at 0 V			-0.10		
		V_A or V_B = -7 V, V_{CC} = 0 V, other input at 0 V			-0.10		
		V_A or V_B = 12 V, other input at 0 V		01, 04, 07, 09		0.35	
		V_A or V_B = 12 V, V_{CC} = 0 V, other input at 0 V				0.4	
		V_A or V_B = -7 V, other input at 0 V			-0.35		
		V_A or V_B = -7 V, V_{CC} = 0 V, other input at 0 V			-0.25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Receiver electrical characteristics - continued							
Input current, $\overline{RE}$	I_{IH}	V_{IH} = 0.8 V or 2 V	-55°C to +125°C	All	-60		µA
Differential input capacitance	C_{ID}	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V	+25°C	All	15 typical 3/		pF
Supply current section							
Supply current	I_{CC}	D at 0 V or V_{CC} and no load	-55°C to +125°C	01		2.1	mA
				02, 03		6.4	
				07, 08		7.9	
		$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, no load (receiver enabled and driver disabled)		04		1.8	
				05, 06		2.2	
				09, 10		3.8	
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, no load (receiver disabled and driver disabled)	+25°C	04, 05, 06		1.5	µA
				09, 10		1	
		$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, no load (receiver enabled and driver enabled)	-55°C to +125°C	04		2.1	mA
				05, 06		6.5	
				09		3.5	
				10		8	
		$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC}, no load (receiver disabled and driver enabled)	-55°C to +125°C	04		1.8	
				05, 06		6.2	
				09		2.5	
				10		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Receiver switching characteristics							
Propagation delay time, low to high level output	t_{PLH}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 13	-55°C to +125°C	01, 04, 07, 09		60	ns
				02, 03, 05, 06, 08, 10		70	
Propagation delay time, high to low level output	t_{PHL}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 13	-55°C to +125°C	01, 04, 07, 09		60	ns
				02, 03, 05, 06, 08, 10		70	
Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$t_{sk(p)}$	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 13	-55°C to +125°C	01, 04, 07, 08, 09, 10		12	ns
				02, 03, 05, 06		10	
Output signal rise time	t_r	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 13	-55°C to +125°C	01-03, 05-09		10	ns
				04		18	
Output signal fall time	t_f	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 13	-55°C to +125°C	All		12.5	ns
Output disable time from high level	t_{PHZ}	DE at 3 V, C_L = 15 pF, see figure 14	-55°C to +125°C	All		20	ns
Output enable time to high level	t_{PZH1}	DE at 3 V, C_L = 15 pF, see figure 14	-55°C to +125°C	All		20	ns
Propagation delay time, standby to high level output	t_{PZH2}	DE at 0 V, C_L = 15 pF, see figure 14	-55°C to +125°C	01-03, 05-09		4000	ns
				04		5000	
Output disable time from low level	t_{PLZ}	DE at 3 V, C_L = 15 pF, see figure 15	-55°C to +125°C	All		20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Receiver switching characteristics – continued.							
Output enable time to low level	t_{PZL1}	DE at 3 V, C_L = 15 pF, see figure 15	-55°C to +125°C	All		20	ns
Propagation delay time, standby to low level output	t_{PZL2}	DE at 0 V, C_L = 15 pF, see figure 15	-55°C to +125°C	01-03, 05-09		4000	ns
				04		5000	
Device power dissipation	P_D	Input to D a 50 % duty cycle square wave at indicated signaling rate, T_A = +85°C, R_L = 60 Ω, C_L = 50 pF	-55°C to +125°C	01, 07		197	mW
				02, 08		213	
				03		193	
		Input to D a 50 % duty cycle square wave at indicated signaling rate, T_A = +85°C, R_L = 60 Ω, C_L = 50 pF, DE at V_{CC}, $\overline{RE}$ at 0 V		04, 09		197	
				05, 10		193	
				06		248	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ 10% of the peak to peak differential output voltage swing, per TIA/EIA-485.

3/ All typical values at 25°C with 3.3 V supply.

Case X

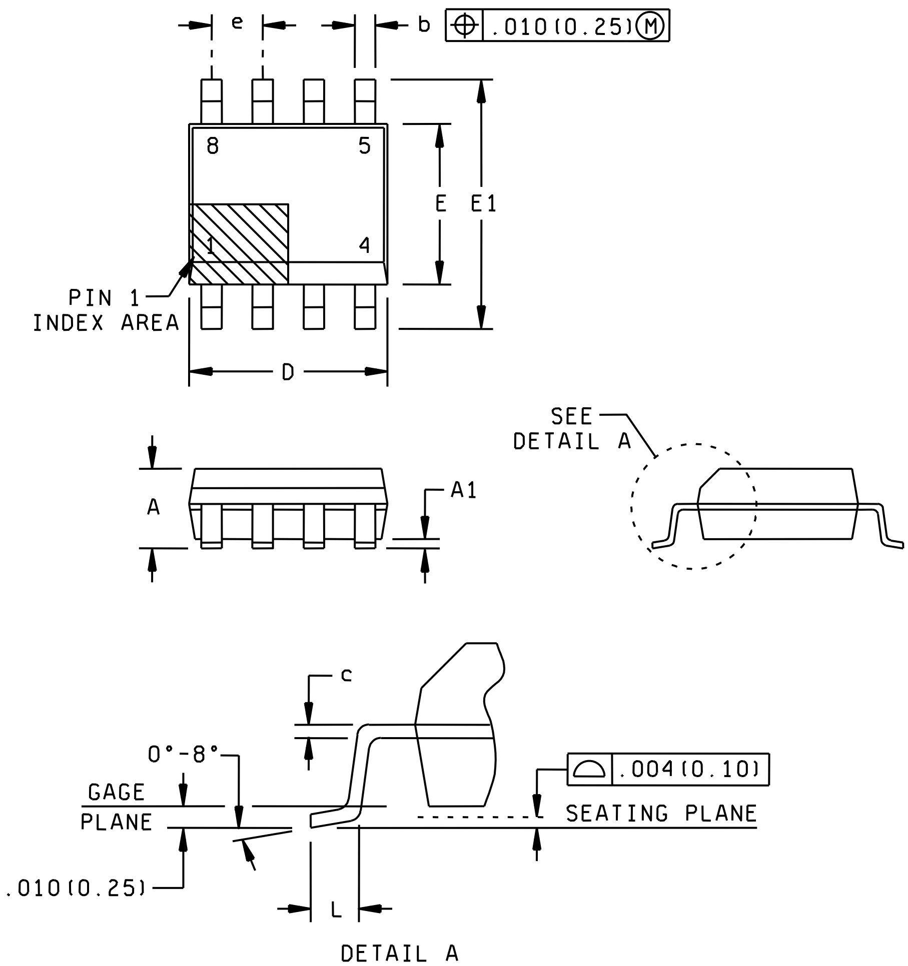


FIGURE 1. Case outlines.

Case X - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outlines – Continued.

Case Y

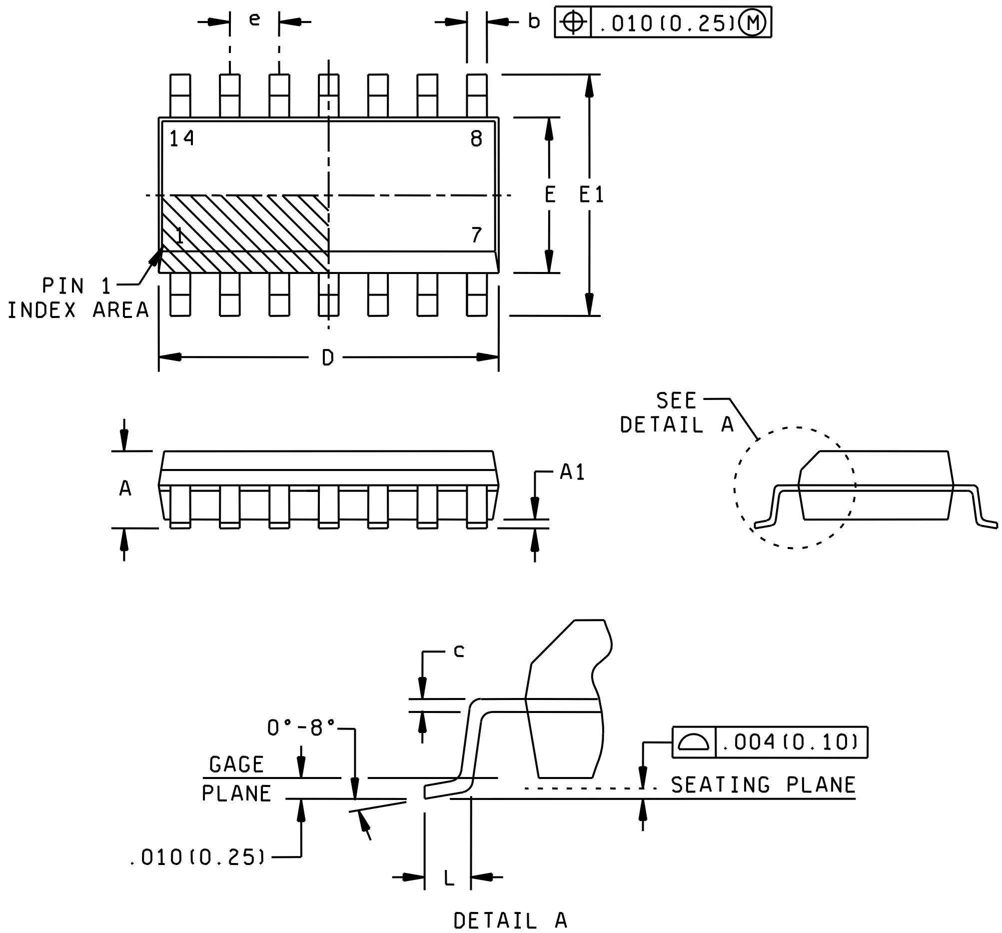


FIGURE 1. Case outlines – Continued.

Case Y - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.337	.344	8.55	8.75
e	.050 BSC		1.27 BSC	
E	.150	.157	3.80	4.00
E1	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
n	14 leads		14 leads	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012-AB.

FIGURE 1. Case outlines - Continued.

Device types	01, 02, 03, 07, 08	04, 05, 06, 09, 10
Case outlines	X	Y
Terminal number	Terminal symbol	
1	V_{CC}	NC
2	R	R
3	D	$\overline{RE}$
4	GND	DE
5	Y	D
6	Z	GND
7	B	GND
8	A	NC
9	---	Y
10	---	Z
11	---	B
12	---	A
13	---	V_{CC}
14	---	V_{CC}

FIGURE 2. Terminal connections.

Driver		
Device types 01, 02, 03, 07, 08		
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

H = High voltage level, L = Low voltage level

Receiver	
Device types 01, 02, 03, 07, 08	
DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} – V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.15$ V	L
-0.15 V $< V_{ID} <$ -0.02 V	?
-0.02 V $\leq V_{ID}$	H
Open circuit	H
Idle circuit	H
Short circuit, $V_{(A)} = V_{(B)}$	H

H = High voltage level, L = Low voltage level, ? = Indeterminate

FIGURE 3. Truth table.

Driver			
Device types 04, 05, 06, 09, and 10			
INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

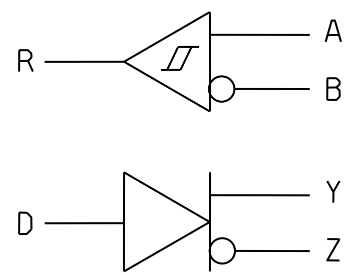
H = High voltage level, L = Low voltage level, Z = High impedance, X = Irrelevant

Receivers		
Device types 04, 05, 06, 09, 10		
DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} – V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V < V_{ID} < -0.02 V	L	?
-0.02 V ≤ V_{ID}	L	H
X	H or open	Z
Open circuit	L	H
Idle circuit	L	H
Short circuit, $V_{(A)} = V_{(B)}$	L	H

H = High voltage level, L = Low voltage level, Z = High impedance, X = Irrelevant, ? = Indeterminate

FIGURE 3. Truth table – Continued.

Device types 01, 02, 03, 07, 08



Device types 04, 05, 06, 09, 10

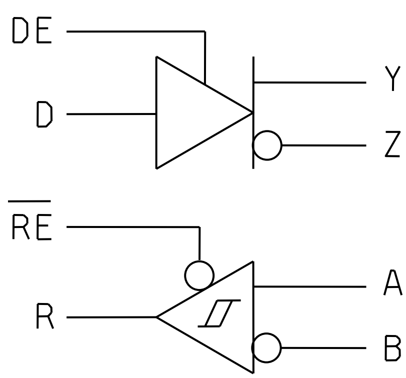


FIGURE 4. Logic diagram.

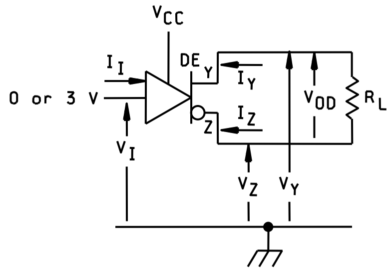


FIGURE 5. Driver V_{OD} test circuit and voltage and current definitions.

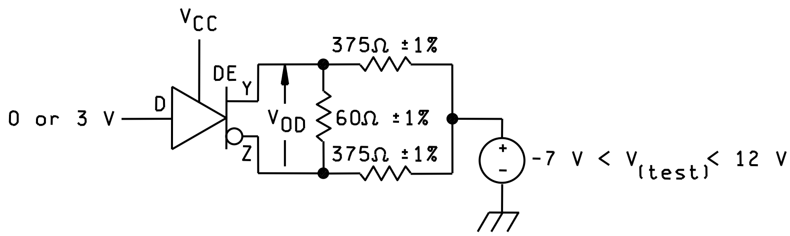
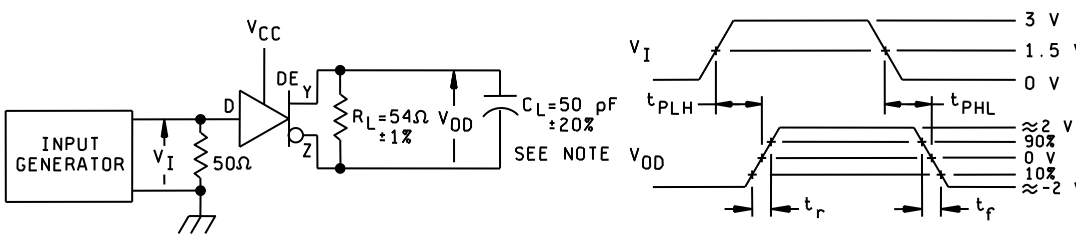
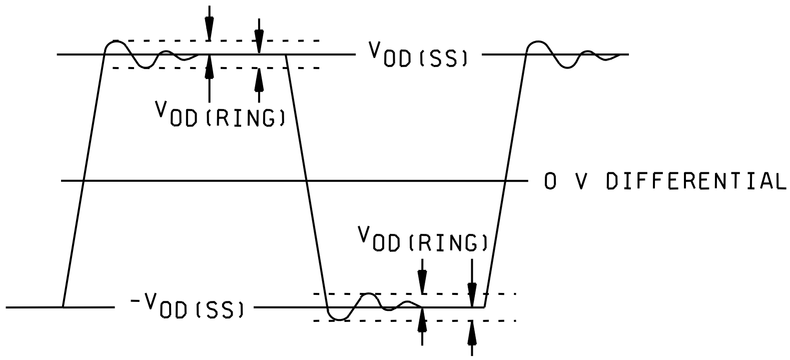


FIGURE 6. Driver V_{OD} with common mode loading test circuit.



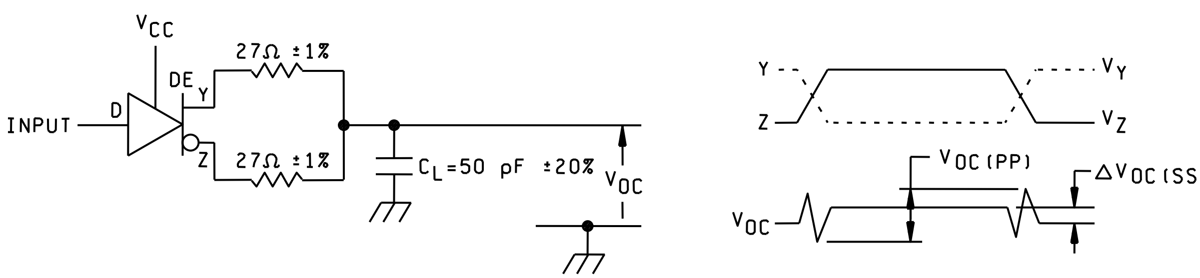
NOTES: 1. Generator: PRR = 500 kHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω.
2. C_L includes fixture and instrumentation capacitance.

FIGURE 7. Driver switching test circuit and voltage waveforms.



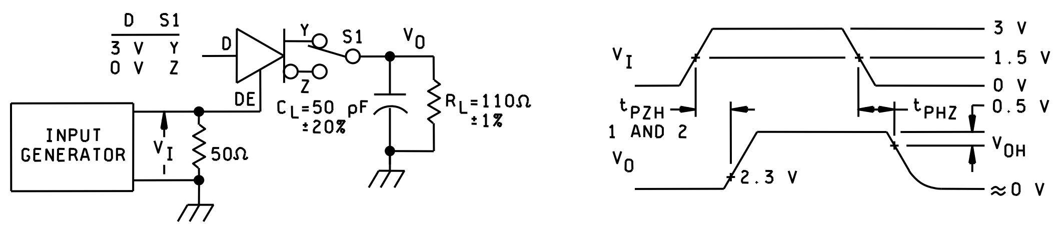
$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

FIGURE 8. $V_{OD(RING)}$ waveform and definitions.



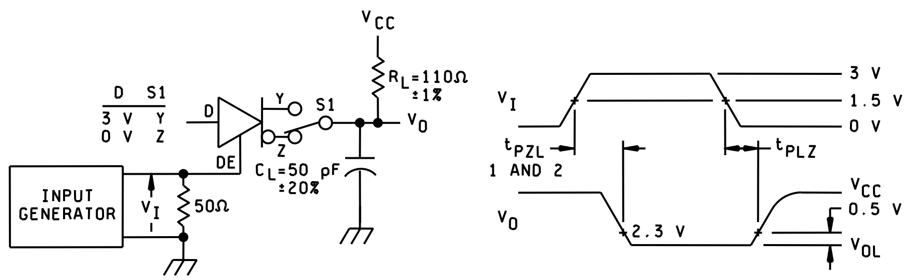
Input PRR = 500 kHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω.

FIGURE 9. Test circuit and definitions for driver common mode output voltage.



NOTES: 1. Generator: PRR = 500 kHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$.
2. C_L includes fixture and instrumentation capacitance.

FIGURE 10. Driver high level output enable and disable time test circuit and voltage waveforms.



NOTES: 1. Generator: PRR = 500 kHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$.
2. C_L includes fixture and instrumentation capacitance.

FIGURE 11. Driver low level output enable and disable and disable time test circuit and voltage waveforms.

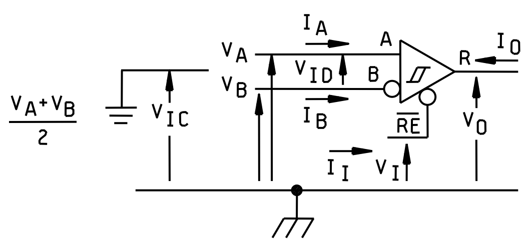
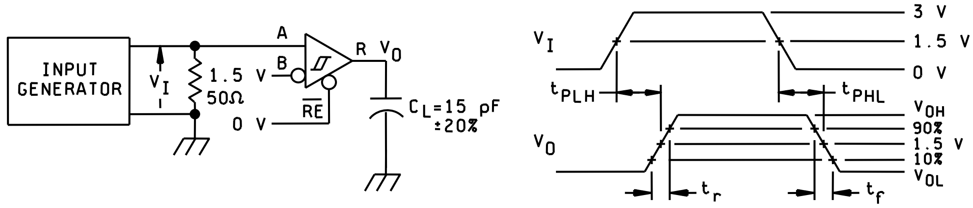


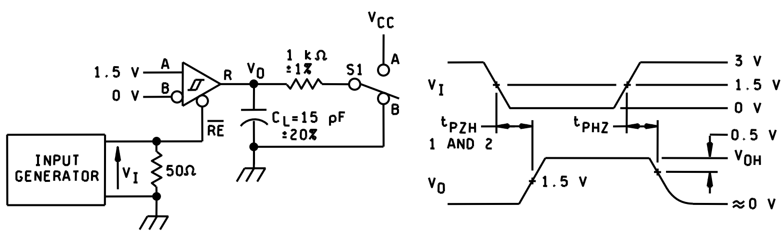
FIGURE 12. Receiver voltage and current definitions.



NOTES: 1. C_L includes fixture and instrumentation capacitance.

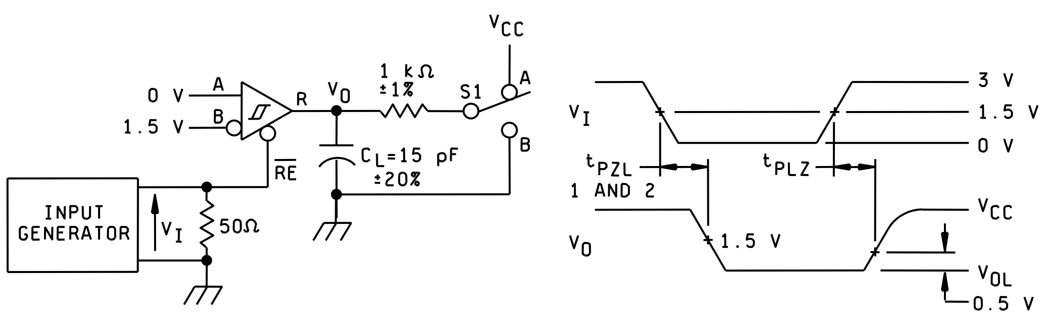
2. Generator: PRR = 500 kHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$.

FIGURE 13. Receiver switching test circuit and voltage waveforms.



NOTE: 1. Generator: PRR = 500 kHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$.

FIGURE 14. Receiver high level enable and disable time test circuit and voltage waveforms.



NOTE: 1. Generator: PRR = 500 kHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$.

FIGURE 15. Receiver enable time from standby (driver disabled).

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Signaling rate	Unit loads	SOIC marking	Vendor part number
V62/06634-01XE	01295	25 Mbps	1/2	HVD30EP	SN65HVD30MDREP
V62/06634-02XE	2/	5 Mbps	1/8	65HVD31	SN65HVD31
V62/06634-03XE	2/	1 Mbps	1/8	65HVD32	SN65HVD32
V62/06634-04YE	01295	25 Mbps	1/2	65HVD33	SN65HVD33MDREP
V62/06634-05YE	2/	5 Mbps	1/8	65HVD34	SN65HVD34
V62/06634-06YE	2/	1 Mbps	1/8	65HVD35	SN65HVD35
V62/06634-07XE	2/	25 Mbps	1/2	---	SN65HVD36
V62/06634-08XE	2/	5 Mbps	1/8	---	SN65HVD37
V62/06634-09YE	2/	25 Mbps	1/2	---	SN65HVD38
V62/06634-10YE	2/	5 Mbps	1/8	---	SN65HVD39

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Product preview.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243