REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-01-27	Thomas M. Hess
B	Correct the Top Side Marking in last page. - PHN	17-08-21	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-05-22	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** http://www.landandmaritime.dla.mil/
Original date of drawing YY MM DD 06-10-10	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CAGE CODE** 16236	**DWG NO.** V62/06633
	REV C	**PAGE** 1 OF 12

AMSC N/A

5962-V089--23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single D type Flip-Flop with asynchronous clear microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06633	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC1G175-EP	Single D-type flip-flop with asynchronous clear

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	MO-203	Plastic small outline
Y	6	MO-178	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_I)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to V_{CC} +0.5 V 2/ 3/
Maximum input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Maximum continuous output current (I_O)	±50 mA
Maximum continuous current through V_{CC} or GND	±100 mA
Maximum package thermal impedance (θ_{JA}): 4/	
Case X	259°C/W
Case Y	165°C/W
Storage temperature range (T_{STG})	-65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}):	
Operating	1.65 V to 5.5 V
Data retention only	1.5 V minimum
Minimum high level input voltage	
V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	1.7 V
V_{CC} = 3 V to 3.6 V	2.0 V
V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}
Maximum high level input voltage	
V_{CC} = 1.65 V to 1.95 V	0.35 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	0.7 V
V_{CC} = 3 V to 3.6 V	0.8 V
V_{CC} = 4.5 V to 5.5 V	0.3 x V_{CC}
Input voltage (V_I)	0 V to 5.5 V
Output voltage (V_O)	0 to V_{CC}
Maximum high level output current (I_{OH}):	
V_{CC} = 1.65 V	-4 mA
V_{CC} = 2.3 V	-8 mA
V_{CC} = 3 V	-16 mA
V_{CC} = 3 V	-24 mA
V_{CC} = 4.5 V	-32 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 1.65 V	4 mA
V_{CC} = 2.3 V	8 mA
V_{CC} = 3 V	16 mA
V_{CC} = 3 V	24 mA
V_{CC} = 4.5 V	32 mA

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value of V_{CC} is provided in the recommended operating conditions stable.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

1.4 Recommended operating conditions - Continued.

Maximum input transition rise or fall rate (Δt/Δv) :
V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2V ..... 20 ns/V
V_{CC} = 3.3 V ±0.3 V ..... 10 ns/V
V_{CC} = 5.0 V ±0.5 V ..... 10 ns/V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices
JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figures 5-6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	I_{OH} = -100 µA	1.65 V to 5.5 V	V_{CC} – 0.1		V
		I_{OH} = -4 mA	1.65V	1.2		
		I_{OH} = -8 mA	2.3 V	1.9		
		I_{OH} = -16 mA	3.0 V	2.4		
		I_{OH} = -24 mA		2.3		
		I_{OH} = -32 mA	4.5 V	3.8		
Low level output voltage	V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V		0.1	V
		I_{OL} = 4 mA	1.65V		0.45	
		I_{OL} = 8 mA	2.3 V		0.3	
		I_{OL} = 16 mA	3.0 V		0.4	
		I_{OL} = 24 mA			0.55	
		I_{OL} = 32 mA	4.5 V		0.55	
Input current A inputs	I_I	V_I = 5.5 V or GND	0 to 5.5 V		±1	µA
Off current	I_{off}	V_I or V_O = 5.5 V	0		±10	µA
Supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0,	1.65 V to 5.5V		10	µA
Quiescent supply current	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other input at V_{CC} or GND	3.0 V to 5.5V		500	µA
Input capacitance	C_i	V_I = V_{CC} or GND, T_A = 25°C	3.3 V	3 Typ		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

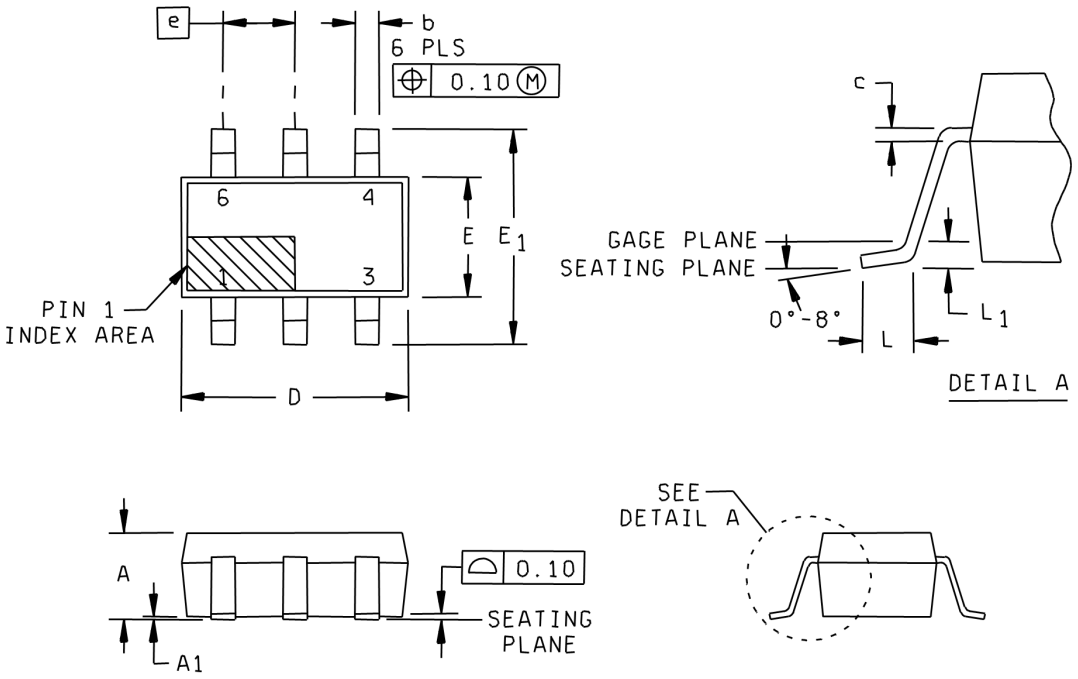
Test		Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC} = 1.8 V ±0.15 V		V_{CC} = 2.5 V ±0.2 V		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 5.0 V ±0.5 V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Switching characteristics												
Clock frequency		f_{clock}	See figure 5		100		125		150		175	MHz
Pulse duration	$\overline{CLR}$ Low	t_w		6.0		3.5		3.2		3.0		ns
	CLK High or low			4.0		3.5		3.2		3.0		
Setup time, before CLK↑	Data	t_{su}		3.0		2.5		2.0		1.5		
	$\overline{CLR}$ inactive			0.7		0.7		0.7		0.7		
Hold time, data after CLK↑		t_h		0.7		0.7		0.7		0.7		
Switching characteristics												
Maximum frequency		f_{max}	See figure 6	100		125		150		175		MHz
Propagation from input CLK to output Q				2.7	16	2.2	9	1.6	8	1.5	5	ns
Propagation from input $\overline{CLR}$ to output Q				2.7	16	2.2	9	1.6	8	1.3	5	

Operating characteristics

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC} = 1.8 V		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Power dissipation capacitance	C_{pd}	f = 10 MHz, T_A = 25°C	18	Typ	19	Typ	19	Typ	21	Typ	pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



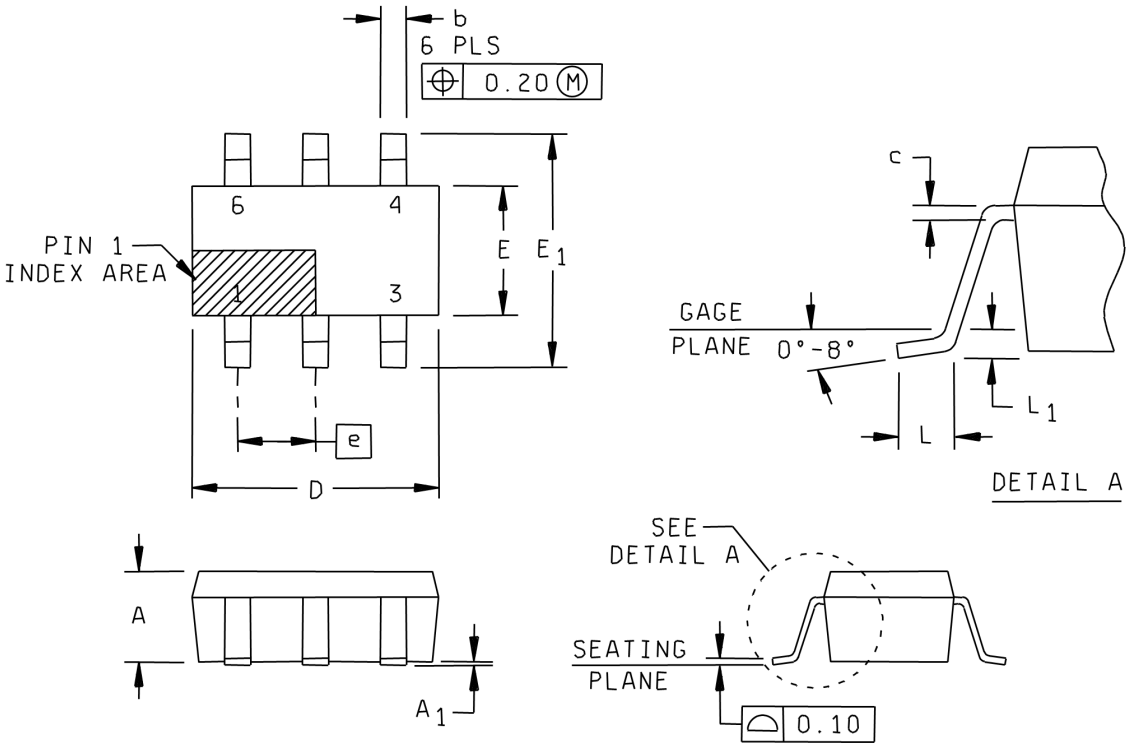
Dimensions

Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 BSC	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15	L1	0.15 TYP	

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
3. Falls within JEDEC MO-203 variation AB.

FIGURE 1. Case outline.

Case Y



Dimensions

Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A		1.45	E	1.45	1.75
A1	0.00	0.15	E1	2.60	3.00
b	0.25	0.50	e	0.95 TYP	
c	0.08	0.22	L	0.26	0.46
D	2.75	3.05	L1	0.25 TYP	

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
3. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
4. Falls within JEDEC MO-178 variation AB, except minimum lead width.

FIGURE 1. Case outline - Continued.

Case X, Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CLK	4	Q
2	GND	5	V_{CC}
3	D	6	$\overline{CLR}$

FIGURE 2. Terminal connections.

Input S			Output Q
$\overline{CLR}$	CLK	D	
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_O
L	X	X	L

FIGURE 3. Function table.

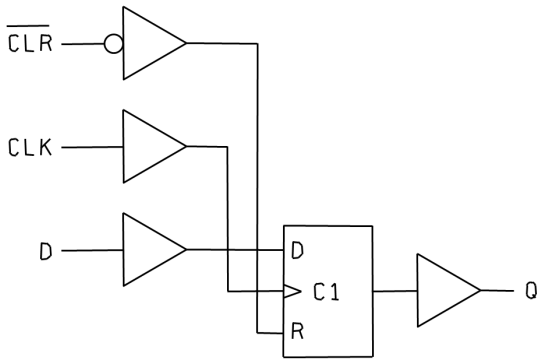
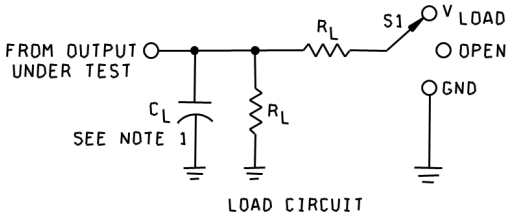


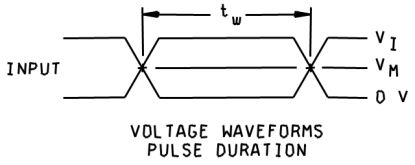
FIGURE 4. Logic diagram.



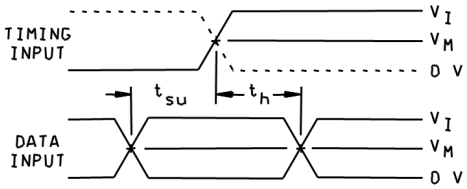
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

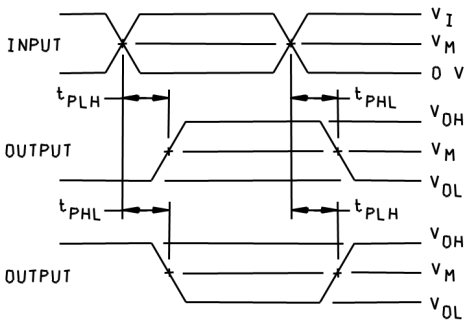
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.3 V



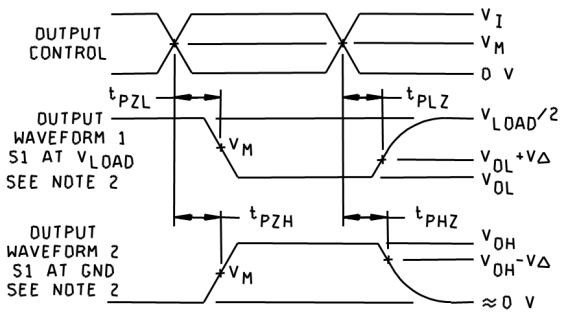
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



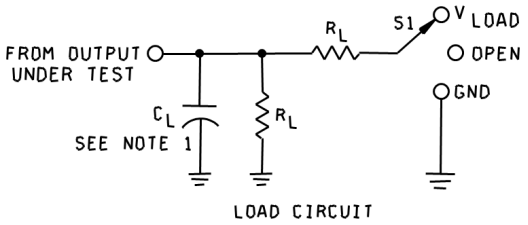
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

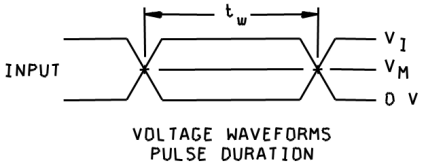
NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PHL} and t_{PLH} are the same as t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

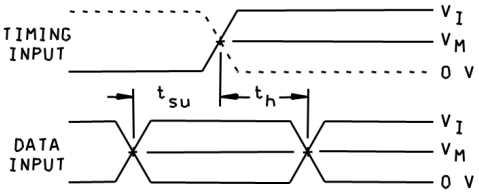


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

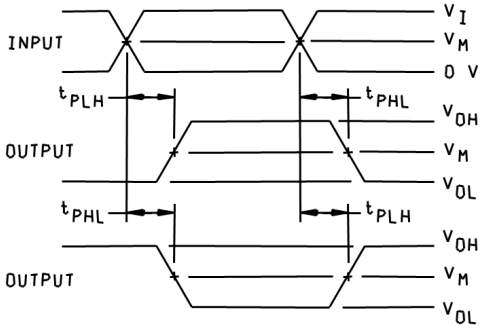
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	500Ω	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2\times V_{CC}$	50 pF	500Ω	0.3 V



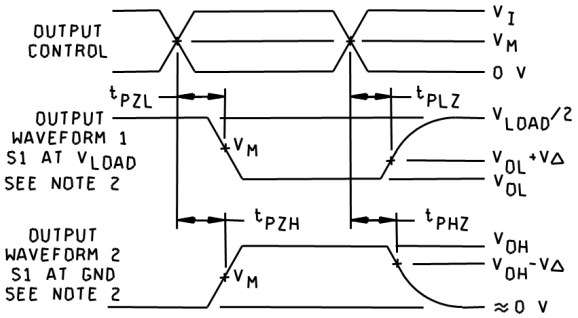
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PHL} and t_{PLH} are the same as t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 6. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/06633-01XE	01295	CLVC1G175MDCKREP	BUD
V62/06633-01YE	2/	CLVC1G175MDBVREP	

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243