REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-01-09	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-07-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO**
Original date of drawing YY MM DD 06-06-06	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, 3.3 V CAN TRANSCEIVERS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/06629
	REV B	**PAGE** 1 **OF** 14

AMSC N/A

5962-V072-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.* .

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3 V can transceivers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06629	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65HVD230M-EP	3.3 V can transceiver

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator Finish designator	Material Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.3 V to 6.0 V
Voltage range at any bus terminal (CANH or CANL) ..... -7.0 V to 16 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω (See figure 12) ..... -25.0 V to 25.0 V
Input voltage range (V_I) (D or R) ..... -0.5 V to V_{CC} + 0.5 V
Electrostatic discharge: Human body model 3/
  CANH, CANL and GND ..... 15 kV
  All pins ..... 2.5 kV
  Charged device model , All pins 4/ ..... 4.0 kV
Continuous total power dissipation ..... see dissipation rating table
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Lead temperature 1.6 mm from case for 10 seconds ..... 260°C
Dissipation rating table:

Case outline	$T_A \leq 25°C$ Power rating	Derating factor 5/ Above $T_A = 25°C$	$T_A = 70°C$ Power rating	$T_A = 85°C$ Power rating	$T_A = 125°C$ Power rating
X	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}): ..... 3.0 V to 3.6 V
Voltage at any bus terminal (common mode) (V_{IC}) ..... -2.0 to 7.0 V 5/
Voltage at any bus terminal (separately) (V_{II}) ..... -2.5 to 7.5 V
Minimum high level input voltage, (V_{IH}) D, R ..... 2.0 V
Maximum low level input voltage, (V_{IL}) D, R ..... 0.8 V
Differential input voltage, (V_{ID}) See figure ? ..... -6.0 V to 6.0 V
$V_{(RS)}$ ..... 0.0 V to V_{CC}
$V_{(RS)}$ for standby or sleep ..... 0.75 V_{CC} to V_{CC}
Rs wave shaping resistance ..... 0 Ω to 100 kΩ
Minimum high level output current, (I_{OH}):
  Driver ..... -40 mA
  Receiver ..... -8 mA
Maximum low level output current, (I_{OL}):
  Driver ..... 48 mA
  Receiver ..... 8 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC Standard 22, test method A114-A.
4/ Tested in accordance with JEDEC Standard 22, test method C101
5/ This is the inverse of the junction to ambient thermal resistance when board mounted and with no air flow.
6/ The algebraic convention, in which the least positive (most negative) limit is designated as minimum in used in this data.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
JESD22-A114	–	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Equivalent input and output schematic diagrams. Equivalent input and output schematics diagrams shall be as shown in figures 5.

3.5.6 Voltage waveforms. The voltage waveforms shall be as shown in figures 6-13.

TABLE I. Electrical performance characteristics. 1/

Test			Symbol	Conditions		Limits		Unit
						Min	Max	
Driver electrical characteristics over recommended operating conditions (unless otherwise noted)								
Bus output voltage	Dominant		V_{OH}	V_I = 0 V, See figure 6 and 8	CANH	2.45	V_{CC}	V
					CANL	0.5	1.25	
	Recessive		V_{OL}	V_I = 3 V, See figure 6 and 8	CANH	2.3 Typ 2/		
					CANL	2.3 Typ 2/		
Differential output voltage	Dominant		$V_{OD(D)}$	V_I = 0 V, See figure 6		1.5	3	V
				V_I = 0 V, See figure 7		1.2	3	
	Recessive		$V_{OD(R)}$	V_I = 3 V, See figure 6		-120	12	mV
				V_I = 3 V, No load		-0.5	0.05	V
High level input current			I_{IH}	V_I = 2 V		-30		µA
Low level input current			I_{IL}	V_I = 0.8 V		-30		µA
Short circuit output current			I_{OS}	V_{CANH} = -2 V		-250	250	mA
				V_{CANL} = 7 V		-250	250	
Output current			C_O	See receiver				
Supply current	Standby	Device type 01	I_{CC}	$V_{(RS)} = V_{CC}$			600	µA
	All devices	Dominant		V_I = 0 V, No load	Dominant		17	mA
		Recessive		$V_I = V_{CC}$, No load	Recessive		17	
Driver switching characteristics at T_A = 25°C (unless otherwise noted)								
Propagation delay time, low to high level output			t_{PLH}	$V_{(RS)}$ = 0 V	C_L = 50 pF, See figure 9		85	ns
				R_S with 10 kΩ to ground			190	
				R_S with 100 kΩ to ground			870	
Propagation delay time, high to low level output			t_{PHL}	$V_{(RS)}$ = 0 V			130	
				R_S with 10 kΩ to ground			205	
				R_S with 100 kΩ to ground			1200	
Pulse skew ($\lvert t_{P(HL)} - t_{P(LH)} \rvert$)			$t_{sk(p)}$	$V_{(RS)}$ = 0 V		35 Typ		
				R_S with 10 kΩ to ground		60 Typ		
				R_S with 100 kΩ to ground		370 Typ		
Differential output signal rise time			t_r	$V_{(RS)}$ = 0 V		25	100	
Differential output signal fall time			t_f			40	80	
Differential output signal rise time			t_r	R_S with 10 kΩ to ground		75	160	
Differential output signal fall time			t_f			80	150	
Differential output signal rise time			t_r	R_S with 100 kΩ to ground		350	1200	
Differential output signal fall time			t_f			600	1200	
Receiver electrical characteristics over recommended operating conditions (unless otherwise noted)								
Positive going input threshold voltage			V_{IT+}	3/			900	mV
Negative going input threshold voltage			V_{IT-}			500		
Hysteresis voltage (V_{IT+} - V_{IT-})			V_{hys}			100 Typ 2/		
High level output voltage			V_{OH}	-6 V ≤ V_{ID} ≤ 500 mV, I_O = - 8 mA, See figure 10		2.4		
Low level output voltage			V_{OL}	900 mV ≤ V_{ID} ≤ 6 V, I_O = 8 mA, See figure 10			0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Condition		Limits		Unit
				Min	Max	
Receiver electrical characteristics over recommended operating conditions (unless otherwise noted) – Continued.						
Bus input current	I_I	V_{IH} = 7 V	Other input at 0 V, D = 3 V	100	250	µA
		V_{IH} = 7 V, V_{CC} = 0 V		100	350	
		V_{IH} = -2 V		-200	-30	
		V_{IH} = -2 V, V_{CC} = 0 V		-100	-20	
CANH, CANL input capacitance	C_i	Pin to ground, $V_{(D)}$ = 3 V, V_I = 0.4 sin(4E6πt) + 0.5 V		32 Typ 2/		pF
Differential input capacitance	C_{diff}	Pin to pin, $V_{(D)}$ = 3 V, V_I = 0.4 sin(4E6πt) + 0.5 V		16 Typ 2/		
Differential input resistance	R_{diff}	Pin to pin, $V_{(D)}$ = 3 V		40	100	kΩ
CANH, CANL input resistance	R_T			20	50	
Supply current	I_{CC}	See Driver				
Receiver switching characteristics at T_A = 25°C (unless otherwise noted)						
Propagation delay time, low to high level output	t_{PLH}	See figure 11			55	ns
Propagation delay time, high to low level output	t_{PHL}				55	
Pulse skew ($\lvert t_{P(HL)} - t_{P(LH)} \rvert$)	$t_{sk(p)}$				10	
Output signal rise time	t_r			1.5 Typ		
Output signal fall time	t_f			1.5 Typ		
Total loop delay, driver input to receiver output	$t_{(loop)}$	$V_{(RS)}$ = 0 V			135	
		R_S with 10 kΩ to ground			175	
		R_S with 100 kΩ to ground			920	
Device control pin characteristics over recommended operating conditions (unless otherwise noted)						
Wake up time from standby mode with R_S	$t_{(WAKE)}$	See figure 13			1.5	µS
Reference output voltage	V_{ref}	-5 µA < $I_{(Vref)}$ < 5 µA		0.45 V_{CC}	0.55 V_{CC}	V
		-50 µA < $I_{(Vref)}$ < 50 µA		0.4 V_{CC}	0.6 V_{CC}	
Input current for high speed	$I_{(RS)}$	$V_{(RS)}$ < 1 V		-450	0	µA

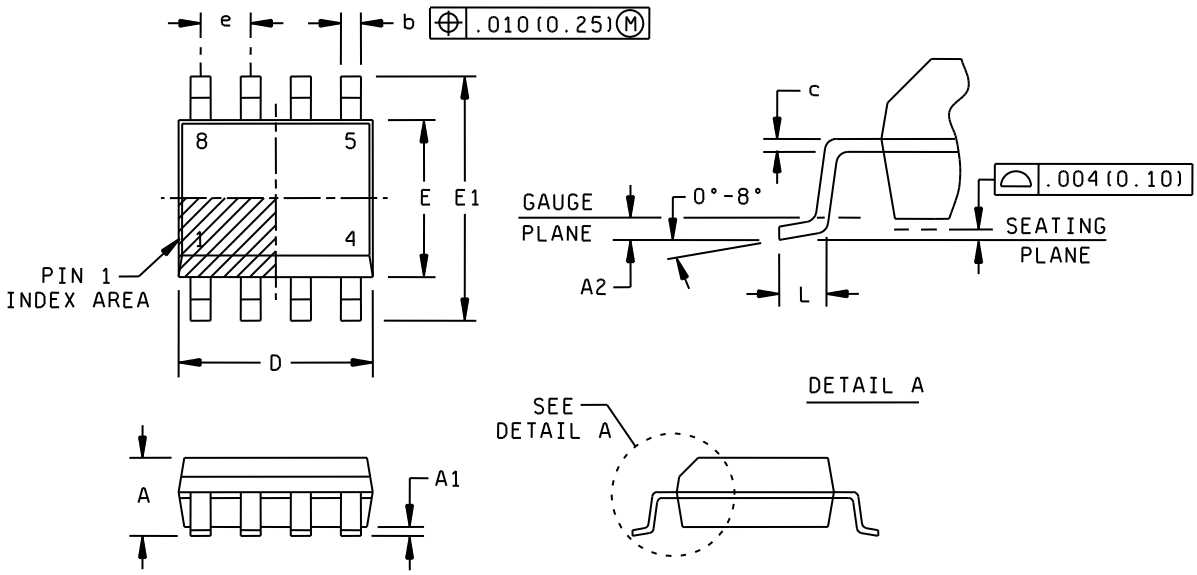
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical values are at 25°C and with a 3.3 V supply.

3/ Receiver characteristics table Over Common Mode with $V_{(RS)}$ at 1.2 V

V_{IC}	V_{ID}	V_{CANH}	V_{CANL}	R Output	
-2 V	900 mV	-1.55 V	-2.45 V	L	V_{OH}
7 V	900 mV	8.45 V	6.5 5 V	L	
1 V	6 V	4 V	-2 V	L	
4 V	6 V	7 V	1 V	L	
-2 V	500 mV	-1.75 V	-2.25 V	H	V_{OL}
7 V	500 mV	7.25 V	6.75 V	H	
1 V	-6V	-2 V	4 V	H	
4 V	-6 V	1 V	7 V	H	
X	X	Open	Open	H	

Case X



Dimension									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.75	D	.189	.197	4.80	5.00
A1	.004	.010	0.10	0.25	E	.150	.157	3.80	4.00
A2	.010 Typ		0.25 Typ		E1	.228	.244	5.80	6.20
b	.012	.020	0.31	0.51	e	.050 NOM		1.27 NOM	
c	.007	.010	0.17	0.25	L	.016	.050	0.40	1.27

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
3. Falls within JEDEC MS-012 variation AA.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Description
1	D	Driver input
2	GND	Ground
3	V_{CC}	Supply voltage
4	R	Receiver output
5	V_{REF}	Reference output
6	CANL	Low bus output
7	CANH	High bus output
8	R_S	Stanby/slope control

FIGURE 2. Terminal connections.

Driver				
Input D	R_S	Output		Bus state
		CANH	CANL	
L	$V_{(RS)}$ < 1.2 V	H	L	Dominant
H		Z	Z	Recessive
Open	X	Z	Z	Recessive
X	$V_{(RS)}$ > 0.75 V_{CC}	Z	Z	Recessive

Receiver		
Differential input	R_S	Output R
V_{ID} ≥ 0.9 V	X	L
0.5 V < V_{ID} < 0.9 V	X	?
V_{ID} ≤ 0.5 V	X	H
Open	X	H

Transceiver modes	
$V_{(RS)}$	**Operating mode**
$V_{(RS)}$ > 0.75 V_{CC}	Standby
10 kΩ to 100 kΩ to ground	Slope control
$V_{(RS)}$ < 1 V	High speed (no slope control)

H = High level
L = Low level
X = Irrelevant
? = Indeterminate

FIGURE 3. Function table.

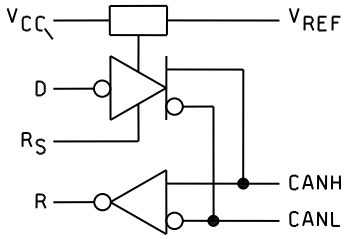


FIGURE 4. Logic diagram.

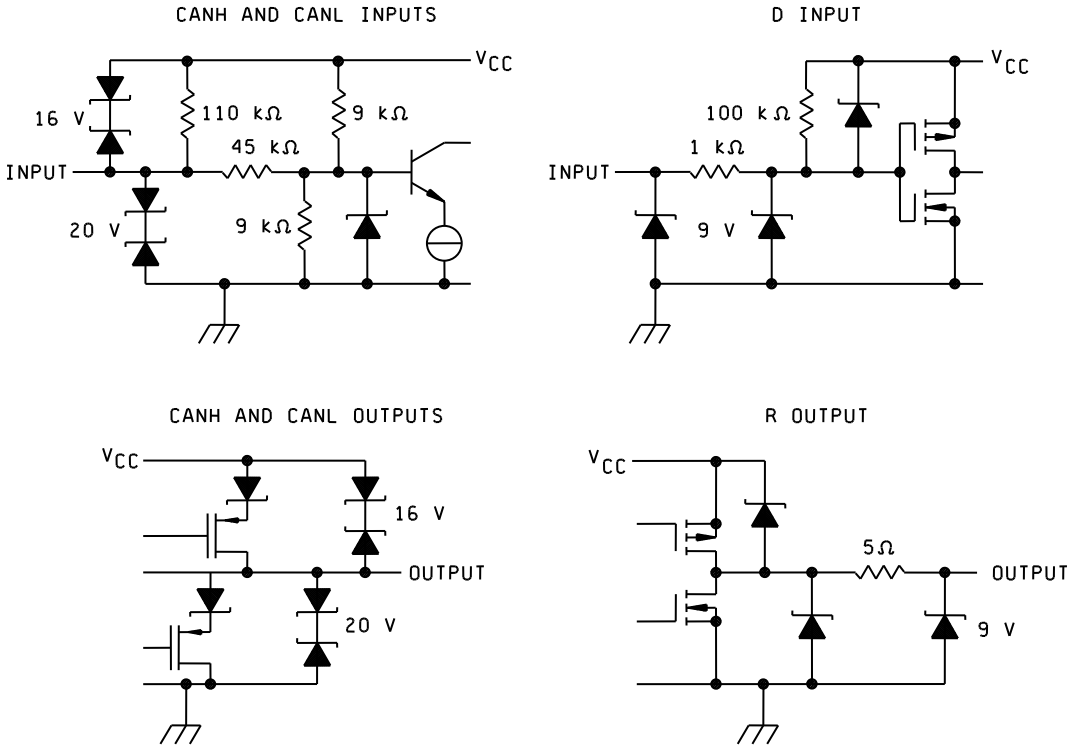
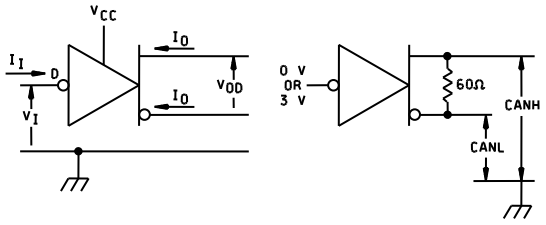
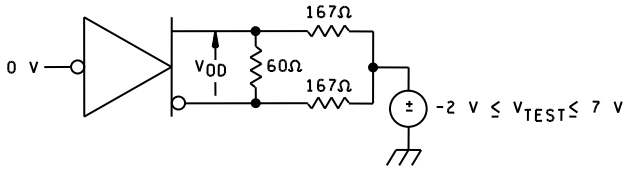


FIGURE 5. Equivalent input and output schematic diagrams.



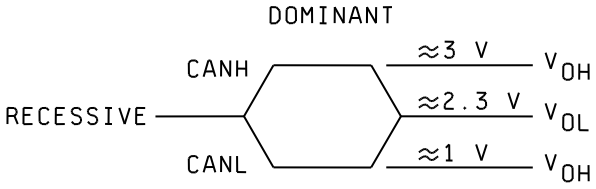
Driver voltage and current definitions

FIGURE 6. Voltage waveforms.



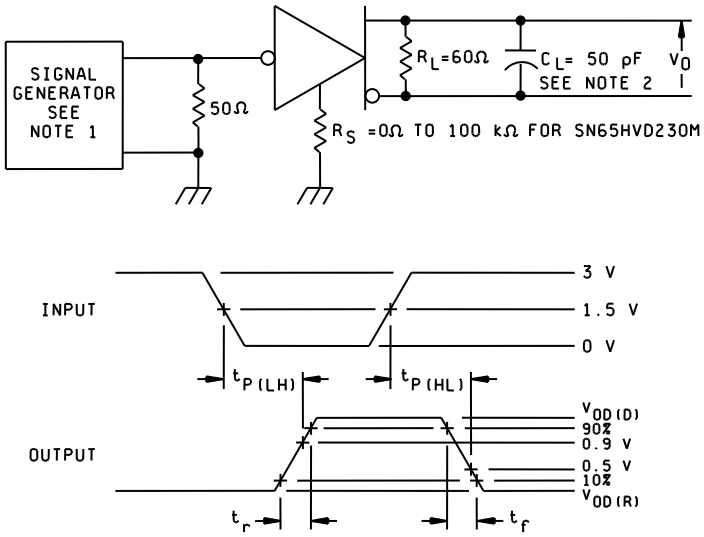
Driver V_{OD}

FIGURE 7. Voltage waveforms.



Driver output voltage definitions

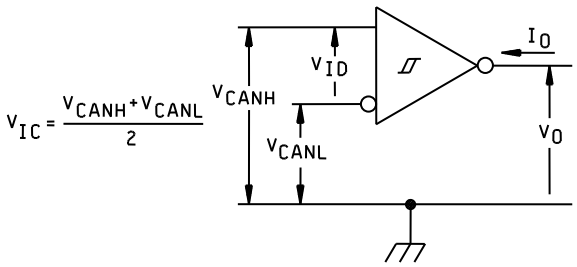
FIGURE 8. Voltage waveforms.



Driver test circuit and voltage waveforms

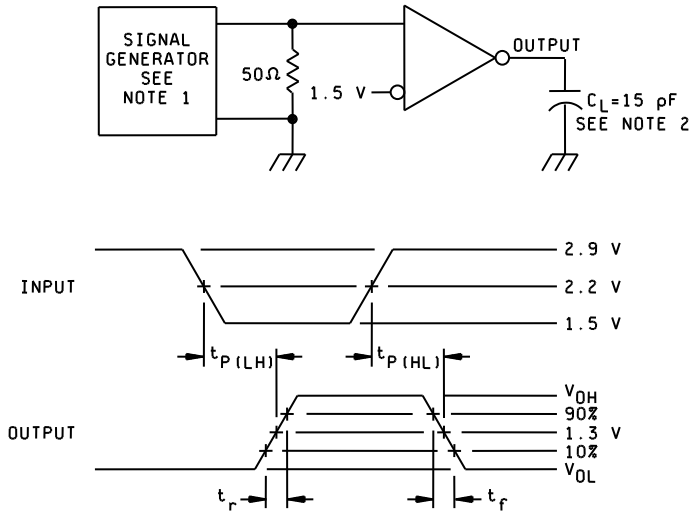
Notes:
1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 9. Voltage waveforms.



Receiver voltage and current definitions

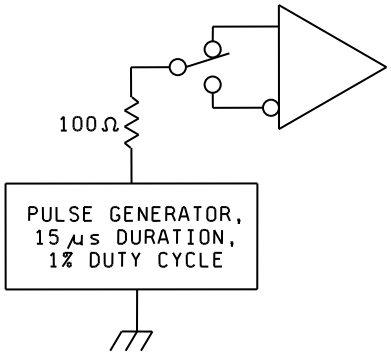
FIGURE 10. Voltage waveforms.



Receiver test circuit and voltage waveforms

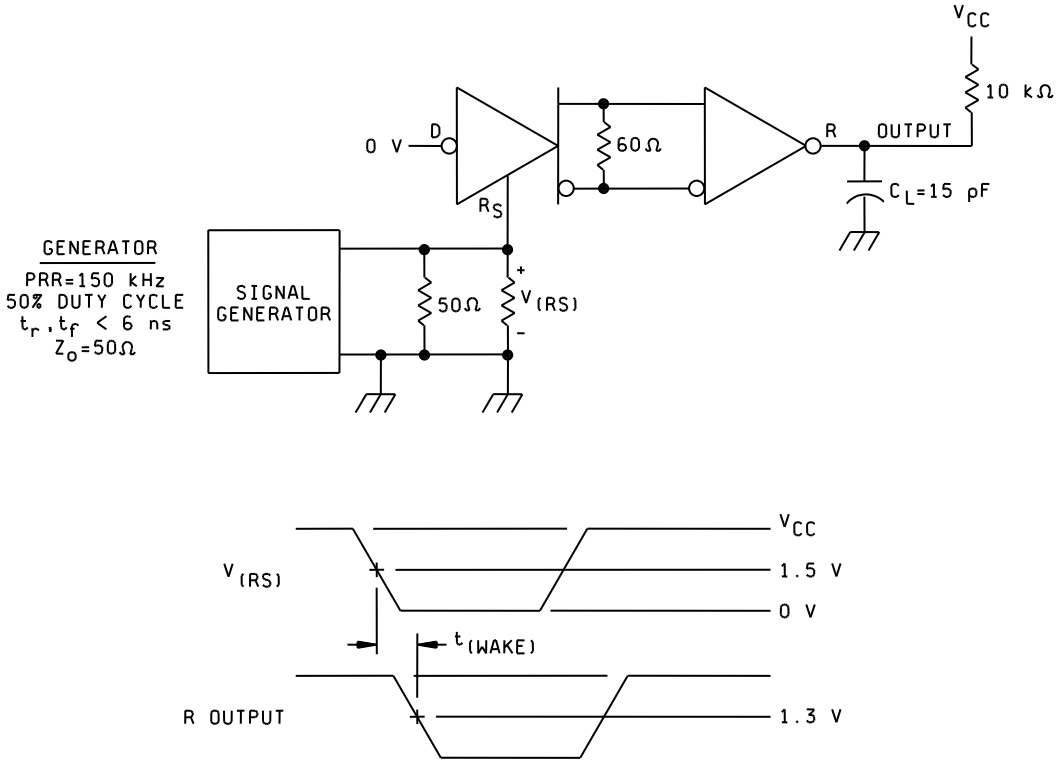
Notes:
1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 11. Voltage waveforms.



Over voltage protection

FIGURE 12. Voltage waveforms.



$t_{(WAKE)}$ test circuit and voltage waveforms

FIGURE 13. Voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06629-01XE	01295	SN65HVD230MDREP	HV230M

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243