REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-01-09	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-07-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B								
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PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-05-30	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/06628
	REV B	**PAGE** 1 **OF** 12

AMSC N/A

5962-V071-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit transparent D-type latch with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06628	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ABT16373A-EP	16-bit transparent D-type latch with 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MO-118	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high or power-off state (V_O)	-0.5 V to 5.5 V
Maximum current into any output in the low state (I_O)	96 mA
Maximum input clamp current (I_{IK}), ($V_I < 0$)	-18 mA
Maximum output clamp current (I_{OK}), ($V_O < 0$)	-50 mA
Maximum package thermal impedance (θ_{JA})	94°C/W 3/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high-level input voltage (V_{IH})	2 V
Maximum low-level input voltage (V_{IL})	0.8 V
Input voltage range (V_I)	0 V to V_{CC}
Maximum high-level output current (I_{OH})	-24 mA
Maximum low-level output current (I_{OL})	48 mA
Maximum input transition rise and fall rate ($\Delta t/\Delta V$) (Outputs enabled)	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$)	200 μs/V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ The package and thermal impedance is calculated in accordance with EIA/JEDEC Std JESD 51.
4/ Unused inputs must be held high or low to prevent them from floating.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical Characteristics							
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_I = -18 mA	+25°C	01		-1.2	V
			-55°C to +125°C			-1.2	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -3 mA	+25°C		2.5		V
			-55°C to +125°C		2.5		
		V_{CC} = 5 V, I_{OH} = -3 mA	+25°C		3		
			-55°C to +125°C		3		
		V_{CC} = 4.5 V, I_{OH} = -24 mA	+25°C		2		
			-55°C to +125°C		2		
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA	+25°C			0.55	V
			-55°C to +125°C			0.55	
Hysteresis voltage	Vhys	V_{CC} = 5 V	+25°C		100 TYP		mV
Input current	I_I	V_{CC} = 0 V to 5.5 V, V_I = V_{CC} or GND	+25°C			±1	µA
			-55°C to +125°C			±1	
3-state output current power-up	I_{OZPU} 2/	V_{CC} = 0 V to 2.1 V, $\overline{\quad}$ V_O = 0.5 V to 2.7 V, OE = X	+25°C			±50	µA
			-55°C to +125°C			±50	
3-state output current power-down	I_{OZPD} 2/	V_{CC} = 2.1 V to 0 V, $\overline{\quad}$ V_O = 0.5 V to 2.7 V, OE = X	+25°C			±50	µA
			-55°C to +125°C			±50	
3-state output leakage current high	I_{OZH}	V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, OE ≥ 2 V	+25°C			10	µA
			-55°C to +125°C			10	
3-state output leakage current low	I_{OZL}	V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, OE ≥ 2 V	+25°C			-10	µA
			-55°C to +125°C			-10	
Input/output power-off leakage current	I_{off}	V_{CC} = 0 V, V_I or V_O ≤ 4.5 V	+25°C			±100	µA
Output high leakage current	I_{CEX}	Outputs high V_{CC} = 5.5 V, V_O = 5.5 V	+25°C			50	µA
			-55°C to +125°C			50	
Output current	I_O 3/	V_{CC} = 5.5 V, V_O = 2.5 V	+25°C		-50	-180	mA
			-55°C to +125°C		-50	-180	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical Characteristics - Continued.							
Quiescent supply current	I_{CC}	Outputs high V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	+25°C			2	mA
			-55°C to +125°C			2	
		Outputs low V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	+25°C			85	
			-55°C to +125°C			85	
		Outputs disabled V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	+25°C			2	
			-55°C to +125°C			2	
Quiescent supply current delta	ΔI_{CC} 4/	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND.	+25°C			1.5	mA
			-55°C to +125°C			1.5	
Input capacitance	C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V	+25°C		3.5 TYP		pF
Output capacitance	C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V	+25°C		9.5 TYP		pF
Timing Requirements							
Pulse duration, LE high	t_w	V_{CC} = 5 V, See figure 5.	+25°C	01	3.3		ns
		V_{CC} = 4.5 V and 5.5 V, See figure 5.	-55°C to +125°C		3.3		
Setup time, data before LE ↓	t_w	V_{CC} = 5 V, See figure 5.	+25°C		1.5		ns
		V_{CC} = 4.5 V and 5.5 V, See figure 5.	-55°C to +125°C		2.4		
Hold time, data after LE ↓	t_w	V_{CC} = 5 V, See figure 5.	+25°C		1		ns
		V_{CC} = 4.5 V and 5.5 V, See figure 5.	-55°C to +125°C		2.2		
Switching Characteristics							
Propagation delay time, D to Q	t_{PLH}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		1.4	5.3	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		1.4	6.5	
	t_{PHL}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		2	5.4	
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		2	6.5	

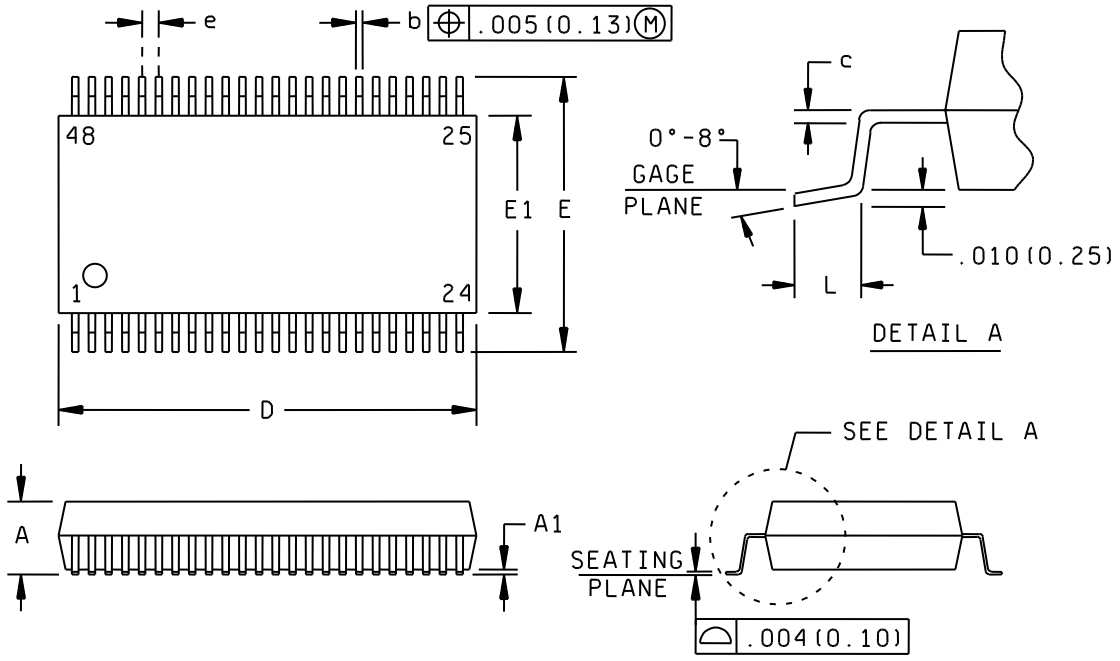
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching Characteristics							
Propagation delay time, LE to Q	t_{PLH}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		1.7	5.7	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		1.7	7	
	t_{PHL}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		2.3	5.6	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		2.3	6.3	
Propagation delay time, output enable, OE to Q	t_{PZH}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		1.1	5	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		1.1	6.4	
	t_{PZL}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		1.5	4.9	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		1.5	5.8	
Propagation delay time, output disable, OE to Q	t_{PHZ}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		2.4	7.1	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		2.4	8.3	
	t_{PLZ}	V_{CC} = 5 V, C_L = 50 pF, See figure 5.	+25°C		1.6	6.3	ns
		V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, See figure 5.	-55°C to +125°C		1.6	8	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ This parameter is characterized, but not production tested.
3/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
4/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.110	---	2.79	e	0.025 Nominal		0.635 Nominal	
A1	0.008	---	0.20	---	E	0.395	0.420	10.03	10.67
b	0.008	0.0135	0.203	0.343	E1	0.291	0.299	7.39	7.59
c	0.005	0.010	0.13	0.25	L	0.020	0.040	0.51	1.02
D	0.620	0.630	15.75	16.00					

NOTES:
1. All linear dimensions are inches (millimeters are shown for reference).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not exceed 0.006 inch (0.15 mm).
4. Falls within JEDEC MO-118.

FIGURE 1. Case outlines.

Device Type:		01			
Case Outline:		X			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	$1\overline{OE}$	17	2Q4	33	2D3
2	1Q1	18	V_{CC}	34	GND
3	1Q2	19	2Q5	35	2D2
4	GND	20	2Q6	36	2D1
5	1Q3	21	GND	37	1D8
6	1Q4	22	2Q7	38	1D7
7	V_{CC}	23	2Q8	39	GND
8	1Q5	24	$2\overline{OE}$	40	1D6
9	1Q6	25	2LE	41	1D5
10	GND	26	2D8	42	V_{CC}
11	1Q7	27	2D7	43	1D4
12	1Q8	28	GND	44	1D3
13	2Q1	29	2D6	45	GND
14	2Q2	30	2D5	46	1D2
15	GND	31	V_{CC}	47	1D1
16	2Q3	32	2D4	48	1LE

FIGURE 2. Terminal connections.

(Each 8-bit section)

Inputs			Output
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level
L = low level
X = Irrelevant
Z = High-impedance state
Q_0 = Level of Q before the indicated steady-state input conditions were established.

FIGURE 3. Function table.

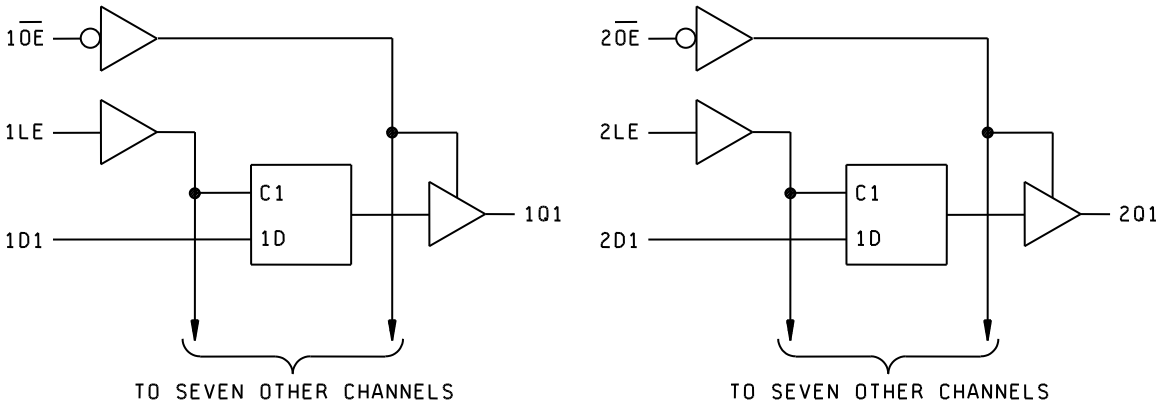
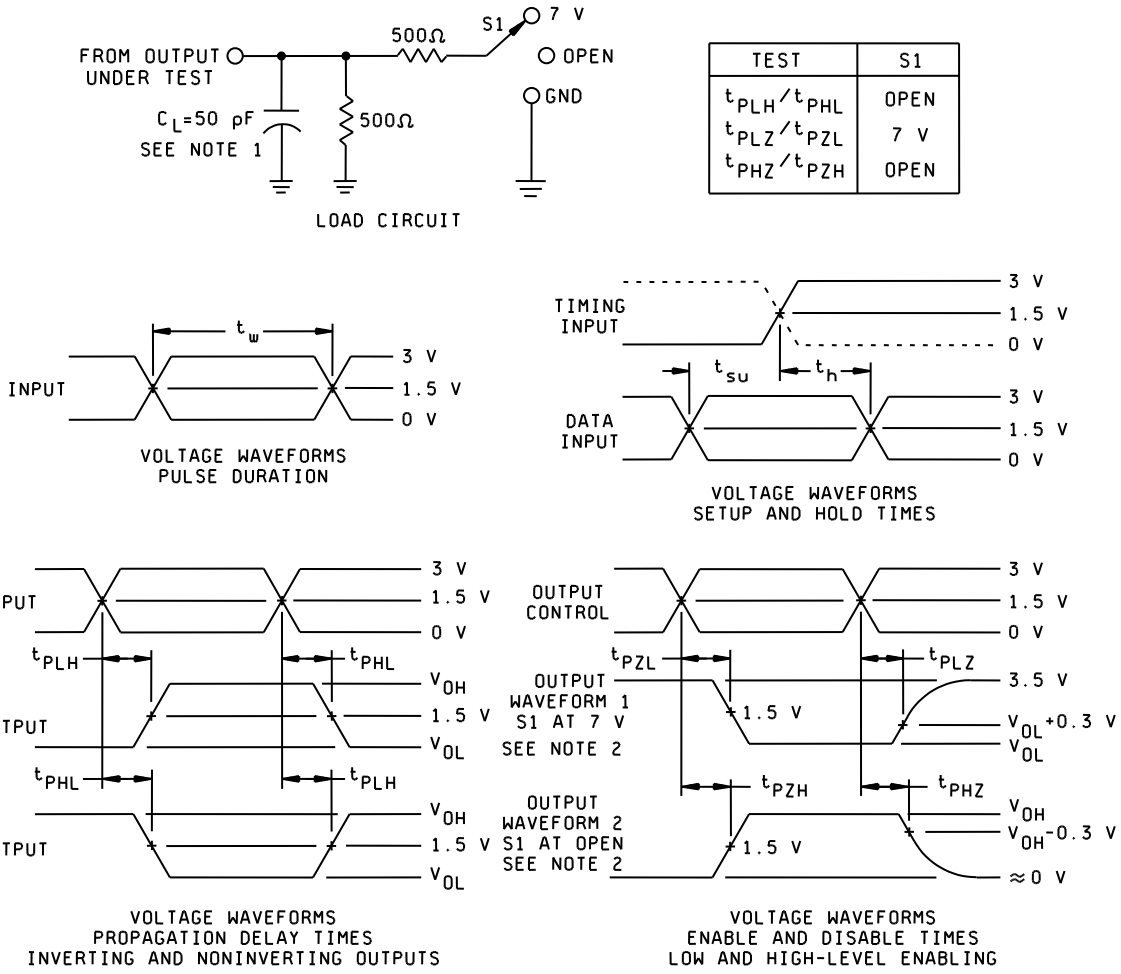


FIGURE 4. Logic diagram.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time, with one transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package		Vendor part number	Top-side marking
V62/06628-01XE	01295	Small outline	Tape and reel	CABT16373AMDLREP	ABT16373AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243