REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Change the topside marking from MA3232C to MB3232M as specified under paragraph 6.3. Make change to note 2 and add note to case outline Y as specified under figure 1. Update document paragraphs to current requirements. - ro	14-05-28	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-04-27	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 3 V TO 5.5 V MULTICHANNEL RS-232 LINE DRIVER / RECEIVER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06623**
	REV A	**PAGE** 1 **OF** 15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3 V to 5.5 V multichannel RS-232 line driver / receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06623	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MAX3232-EP	3 V to 5.5 V multichannel RS-232 line driver / receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-150	Plastic small outline
Y	16	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.3 V to 6 V 2/
Positive output supply voltage range (V+) ..... -0.3 V to 7 V 2/
Negative output supply voltage range (V-) ..... 0.3 V to -7 V 2/
Supply voltage difference (V+ - V-) ..... 13 V 2/
Input voltage range (V_I):
  Drivers ..... -0.3 V to 6 V
  Receivers ..... -25 V to 25 V
Output voltage range (V_O):
  Drivers ..... -13.2 V to 13.2 V
  Receivers ..... -0.3 V to V_{CC} + 0.3 V
Package thermal impedance (θ_{JA}): 3/
  Case X ..... 82°C/W
  Case Y ..... 108°C/W
Operating virtual junction temperature (T_J) ..... 150°C
Storage temperature range (T_{stg}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC}):
  V_{CC} = 3.3 V ..... 3 V to 3.6 V
  V_{CC} = 5 V ..... 4.5 V to 5.5 V
Driver high level input voltage (V_{IH}) at DIN pins:
  V_{CC} = 3.3 V ..... 2 V minimum
  V_{CC} = 5 V ..... 2.4 V minimum
Driver low level input voltage (V_{IL}) at DIN pins ..... 0.8 V maximum
Driver input voltage (V_I) at DIN pins ..... 0 V to 5.5 V
Receiver input voltage (V_I) ..... -25 V to 25 V
Operating free air temperature (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. See figure 6.

2/ All voltages are with respect to network GND.

3/ Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits. See figure 6.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figure 5.

3.5.6 Typical operating circuit. The typical operating circuit shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ see figure 6	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	No load, V_{CC} = 3.3 V to 5 V	-55°C to +125°C	01		2	mA
Driver section							
High level output voltage	V_{OH}	DOUT at R_L = 3 kΩ to GND, DIN = GND	-55°C to +125°C	01	5		V
Low level output voltage	V_{OL}	DOUT at R_L = 3 kΩ to GND, DIN = V_{CC}	-55°C to +125°C	01	5		V
High level input current	I_{IH}	$V_I = V_{CC}$	-55°C to +125°C	01		±1	μA
Low level input current	I_{IL}	V_I at GND	-55°C to +125°C	01		±1	μA
Short circuit output 3/ current	I_{OS}	V_{CC} = 3.6 V, V_O = 0 V	-55°C to +125°C	01		±60	mA
		V_{CC} = 5.5 V, V_O = 0 V				±60	
Output resistance	r_o	V_{CC}, V+, and V- = 0 V, V_O = ±2 V	-55°C to +125°C	01	300		Ω
Switching characteristics section							
Maximum data rate		C_L = 1000 pF, R_L = 3 kΩ, one DOUT switching, see figure 5	-55°C to +125°C	01	150		kbit/s
Pulse skew 4/	$t_{sk(p)}$	C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, see figure 5	+25°C	01	300 typical 5/		ns
Slew rate, transition region	SR(tr)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V, C_L = 150 pF to 1000 pF, see figure 5	-55°C to +125°C	01	6	30	V/μs
		R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V, C_L = 150 pF to 2500 pF, see figure 5			4	30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ see figure 6	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	No load, V_{CC} = 3.3 V to 5 V	-55°C to +125°C	01		2	mA
Receiver section							
High level output voltage	V_{OH}	I_{OH} = -1 mA	-55°C to +125°C	01	V_{CC} – 0.6		V
Low level output voltage	V_{OL}	I_{OL} = 1.6 mA	-55°C to +125°C	01		0.4	V
Positive going input threshold voltage	V_{IT+}	V_{CC} = 3.3 V	-55°C to +125°C	01		2.4	V
		V_{CC} = 5 V				2.4	
Negative going input threshold voltage	V_{IT+}	V_{CC} = 3.3 V	-55°C to +125°C	01	0.6		V
		V_{CC} = 5 V			0.8		
Input hysteresis (V_{IT+} - V_{IT-})	V_{hys}		+25°C	01	0.3 typical 5/		V
Input resistance	r_i	V_I = ±3 V to ±25 V	-55°C to +125°C	01	3	8	kΩ
Switching characteristics section							
Propagation delay time, low to high level output	t_{PLH}	C_L = 150 pF	+25°C	01	300 typical 5/		ns
Propagation delay time, high to low level output	t_{PHL}	C_L = 150 pF	+25°C	01	300 typical 5/		ns
Pulse skew 4/	$t_{sk(p)}$		+25°C	01	300 typical 5/		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Test conditions are C1-C4 = 0.1 μF at V_{CC} = 3.3 V ±0.3 V; C1 = 0.047 μF, C2 –C4 = 0.33 μF at V_{CC} = 5 V ±0.5 V.

3/ Short circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

4/ Pulse skew is defined as | $t_{PLH} – t_{PHL}$ | of each channel of the same device.

5/ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = +25°C.

Case X

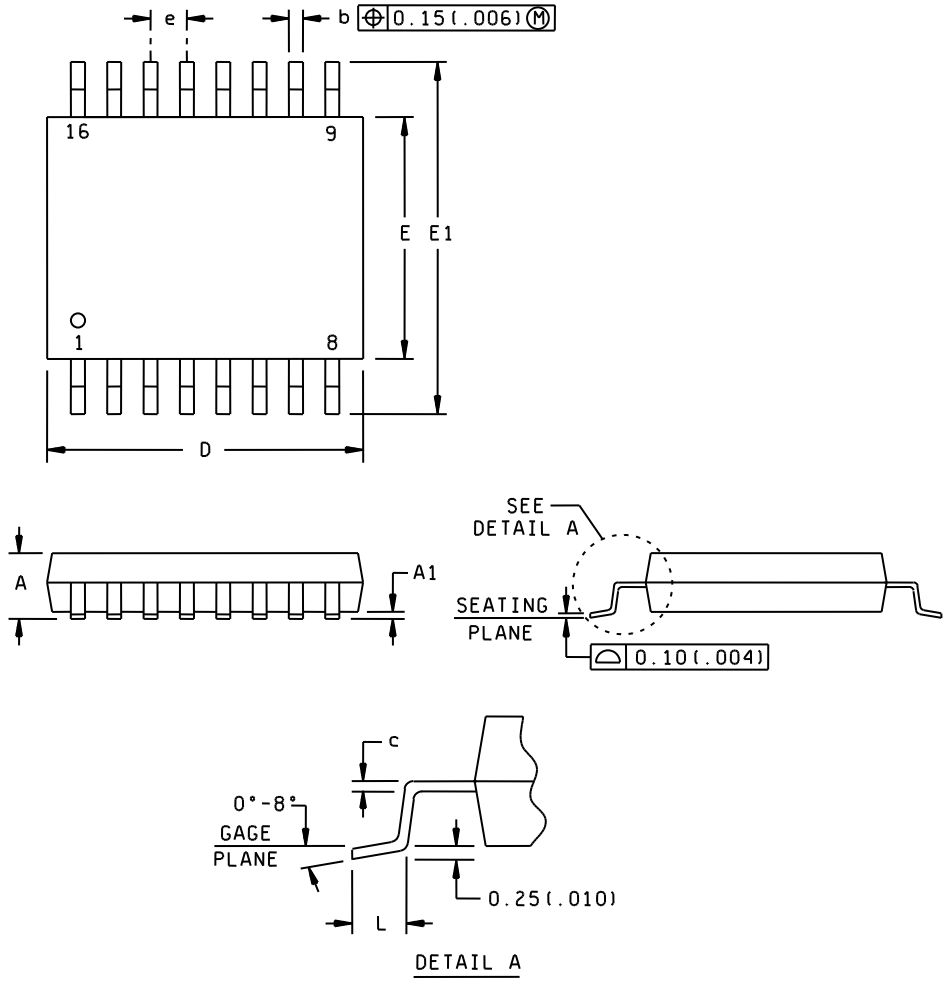

FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/06623
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.078	---	2.00
A1	.001	---	0.05	---
b	.008	.014	0.22	0.38
c	.003	.009	0.09	0.25
D	.232	.255	5.90	6.50
E	.196	.220	5.00	5.60
E1	.291	.322	7.40	8.20
e	.025 nominal		0.65 nominal	
L	.021	.037	0.55	0.95

NOTES:
1. All linear dimensions are in millimeters, inch equivalents are given for general information only.
2. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeter (.006 inch)
3. Fall within JEDEC MO-150.

FIGURE 1. Case outlines – Continued.

Case Y

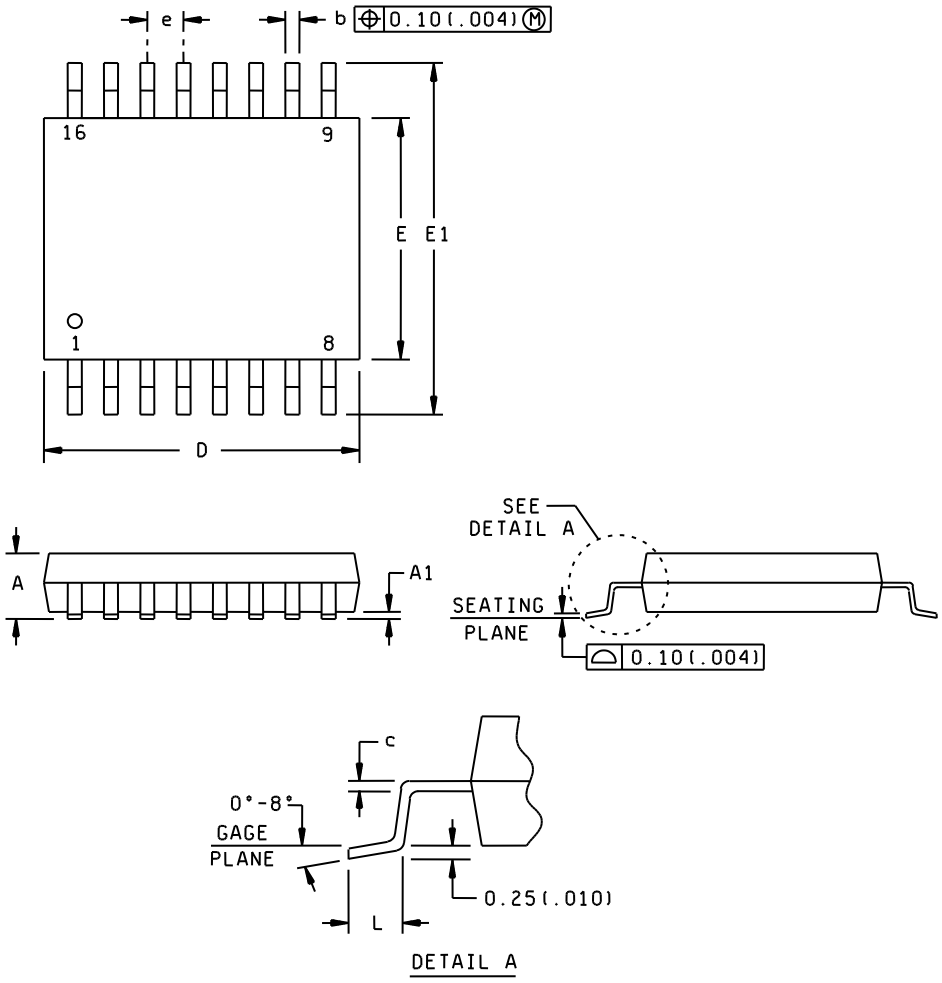


FIGURE 1. Case outlines – Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.005 nominal		.015 nominal	
D	.192	.200	4.90	5.10
E	.169	.177	4.30	4.50
E1	.244	.259	6.20	6.60
e	.025 nominal		0.65 nominal	
L	.019	.029	0.50	0.75

NOTES:
1. All linear dimensions are shown in millimeters, inch equivalents are given for general information only.
2. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.009 inch) each side.
3. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) each side.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

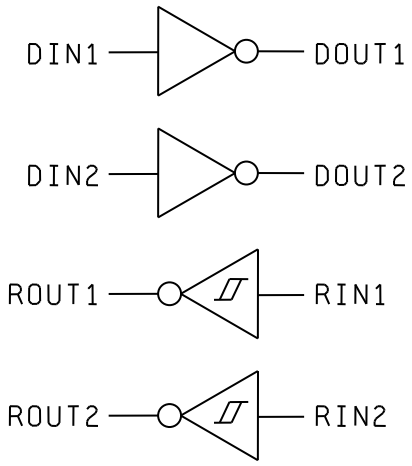
Device type	01
Case outlines	X and Y
Terminal number	Terminal symbol
1	C1+
2	V+
3	C1-
4	C2+
5	C2-
6	V-
7	DOUT2
8	RIN2
9	ROUT2
10	DIN2
11	DIN1
12	ROUT1
13	RIN1
14	DOUT1
15	GND
16	V_{CC}

FIGURE 2. Terminal connections.

Each driver		Each receiver	
Input DIN	Output DOUT	Input RIN	Output ROUT
L	H	L	H
H	L	H	L
---	---	Open	H

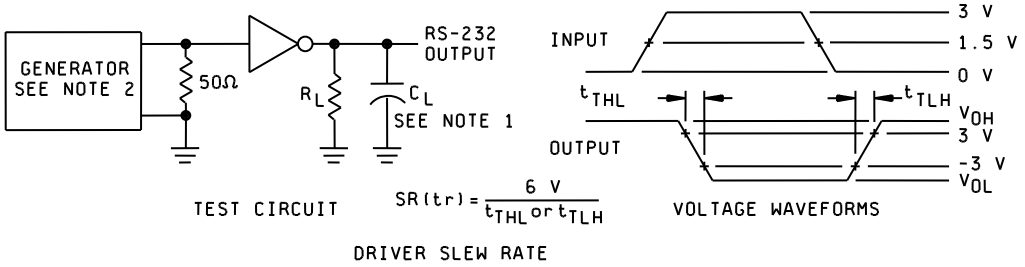
H = High level
L = Low level
Open = Input disconnected or connected driver off

FIGURE 3. Truth table.

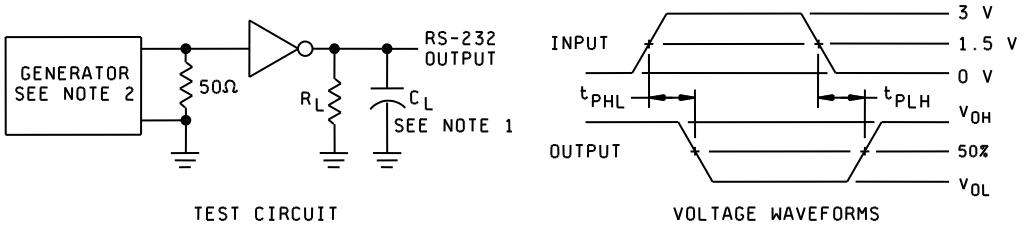


(Positive logic)

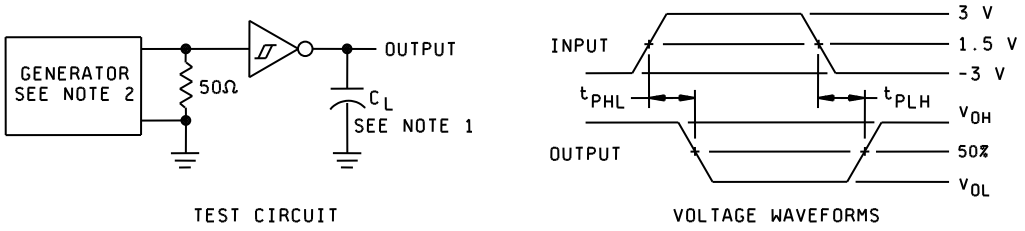
FIGURE 4. Logic diagram.



DRIVER SLEW RATE



DRIVER PULSE SKEW

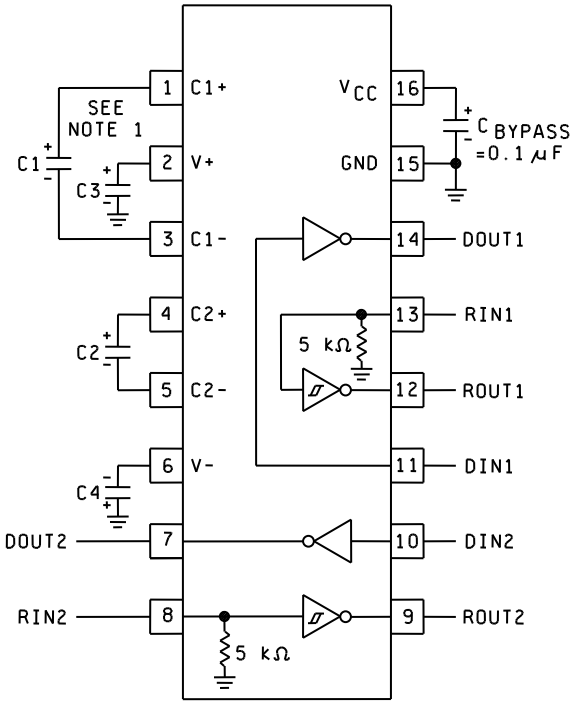


RECEIVER PROPAGATION DELAY TIMES

NOTES:

1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 5. Timing waveforms and test circuits.



V_{CC} versus capacitor values		
V_{CC}	C1	C2, C3, C4
3.3 V ±0.3 V	0.1 µF	0.1 µF
5 V ±0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

NOTES:

1. C3 can be connected to V_{CC} or GND.
2. Resistor values shown are nominal.
3. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

FIGURE 6. Typical operating circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Top side marking	Vendor part number
V62/06623-01XE	01295	Reel of 2000	MB3232M	MAX3232MDBREP
V62/06623-01YE	01295	Reel of 2000	MB3232M	MAX3232MPWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493