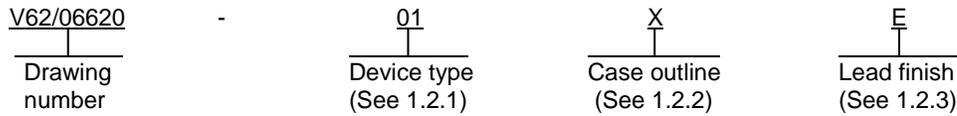


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quadruple 2-input EXCLUSIVE-OR gate microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	CD74ACT86-EP	Quadruple 2-input EXCLUSIVE-OR gate

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	14	MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6 V
Maximum input clamp current (I_{IK}) ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA 2/
Maximum output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA 2/
Maximum continuous output current (I_O) ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance (θ_{JA})	86°C/W 3/
Storage temperature range (T_{STG})	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Input voltage (V_I)	0 V to V_{CC}
Output voltage (V_O)	0 V to V_{CC}
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	24 mA
Maximum input transition rise or fall rate ($\Delta t / \Delta v$)	10 ns/V

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and voltage waveforms shall be as shown in figure 5.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions-	V _{CC}	Limits				Unit	
				T _A = 25°C		-55°C ≤ T _A ≤ 125°C			
				Min	Max	Min	Max		
High level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5 V	4.4		4.4		V
			I _{OH} = -24 mA		3.94		3.7		
			I _{OH} = -50 mA 1/	5.5 V	3.85		3.85		
Low level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5 V		0.1		0.1	V
			I _{OL} = 24 mA			0.36		0.5	
			I _{OL} = 50 mA 1/	5.5 V		1.65		1.65	
Input current	I _I	V _I = V _{CC} or GND	5.5 V		±0.1			±1	μA
Supply current	I _{CC}	V _I = V _{CC} or GND, I _O = 0,	5.5V		4			80	μA
Supply current change 2/	ΔI _{CC}	V _I or V _O = 0 to 5.5 V	4.5 V to 5.5 V		2.4			3	mA
Input capacitance	C _i	V _I = V _{CC} or GND			10			10	pF
Power dissipation capacitance	C _{pd}		5.0 V	57 Typ					
Propagation delay time, from input A or B to output Y	t _{PLH}		4.5 V to 5.5 V			3.7		14.6	ns
	t _{PHL}					3.7		14.6	

1/ Test one output at a time, not exceeding 1-s duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50 Ω transmission line drive capability at 85°C and 75 Ω transmission line drive capability at 125°C

2/ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

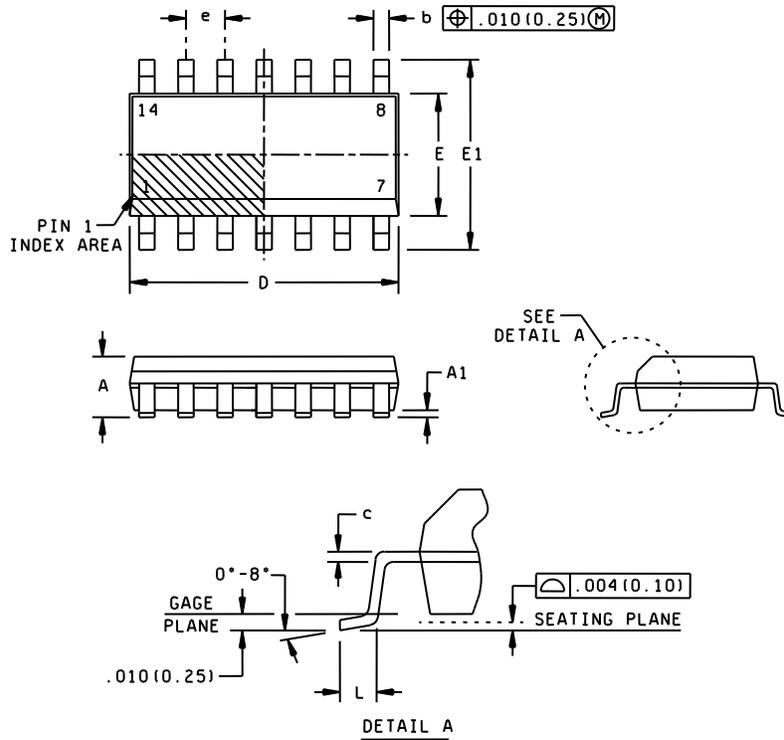
ACT input load table

Input	Unit Load
All	0.48

Unit load is ΔI_{CC} limit specified in electrical characteristic table (e.g., 2.4 mA at 25°C)

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Case X



Dimension									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.75		0.069	E	3.80	4.00	0.150	0.157
A1	0.10	0.25	0.004	0.010	E1	5.80	6.20	0.228	0.244
b	0.31	0.51	0.012	0.020	e	1.27 NOM		0.050 NOM	
c	0.17	0.25	0.007	0.010	L	0.40	1.27	0.016	0.050
D	8.55	8.75	0.337	0.344					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches).
3. Falls within JEDEC MS-012 variation AB.

FIGURE 1. Case outline.

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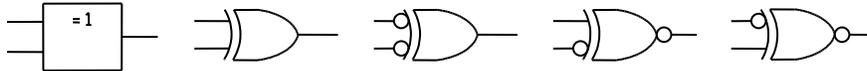
Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V _{CC}

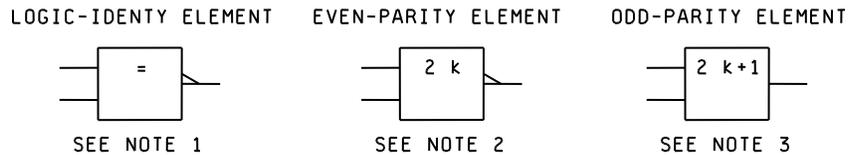
FIGURE 2. Terminal connections.

Input		Output Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

FIGURE 3. Function table.



Five equivalent exclusive-OR symbols

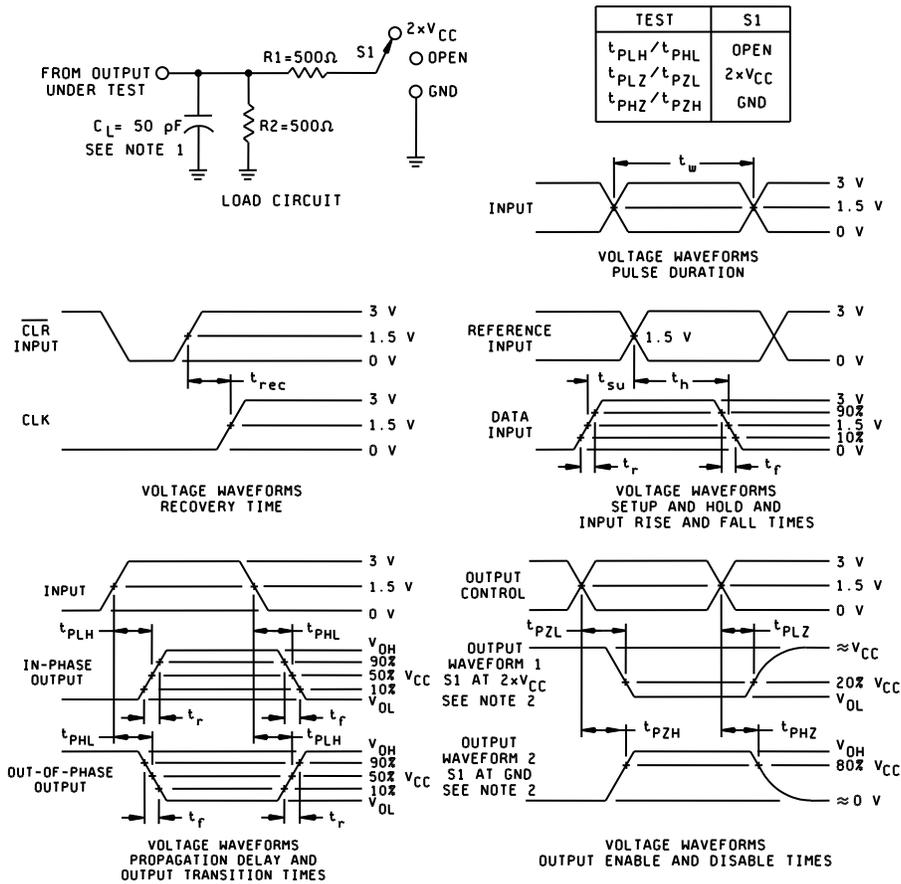


Notes:

1. The output is active (low) if all inputs stand at the same logic level (i.e., A = B).
2. The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.
3. The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

FIGURE 4. Logic diagram.

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NOTES:

- C_L includes probe and test fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, and $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
- For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PHL} and t_{PLH} are the same as t_{pd} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms – Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06620-01XE	01295	CD74ACT86MDREP	ACT86MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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