REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Activate device type 03. - CFS	07-02-21	Thomas M. Hess
B	Correct package style in 1.2.2. - CFS	07-04-17	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	13-12-11	Thomas M. Hess
D	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-07-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	
REV STATUS OF PAGES	**REV**			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 06-05-09	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL SIGNAL PROCESSORS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06619**
	REV **D**	**PAGE** 1 **OF** 38

AMSC N/A

5962-V067-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance floating-point digital signal processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Circuit function
01	SM320F2808-EP	Digital Signal Processors
02	SM320F2806-EP	Digital Signal Processors
03	SM320F2801-EP	Digital Signal Processors

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	100	JEDEC MS-026	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage ranges, (V_{DDIO}, V_{DD3VFL}) (with respect to V_{SS}) ..... -0.3 V to +4.6 V
Supply voltage ranges, (V_{DDA2}, V_{DDAIO}) (with respect to V_{SSA}) ..... -0.3 V to +4.6 V
Supply voltage ranges, (V_{DD}) (with respect to V_{SS}) ..... -0.3 V to +2.5 V
Supply voltage ranges, (V_{DD1A18}, V_{DD2A18}) (with respect to V_{SSA}) ..... -0.3 V to +2.5 V
Supply voltage ranges, (V_{SSA2}, V_{SSAIO}, $V_{SS1AGND}$, $V_{SS2AGND}$) (with respect to V_{SS}) ..... -0.3 V to +0.3 V
Input voltage range, (V_{IN}) ..... -0.3 V to +4.6 V
Output voltage range, (V_O) ..... -0.3 V to +4.6 V
Input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{DDIO}$) ..... ±20 mA 4/
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$) ..... ±20 mA
Operating ambient temperature ranges, (T_A) ..... -55°C to +125°C 5/
Junction temperature range T_J ..... -55°C to +150°C 5/
Storage temperature range, (T_{STG})..... -65°C to +150°C 5/

1.4 Recommended operating conditions.

Device supply voltage, I/O, (V_{DDIO}) ..... +3.14 V to +3.47 V
Device supply voltage, CPU (V_{DD}) ..... +1.71 V to 1.89 V
Supply ground, (V_{SS}, V_{SSIO}) ..... 0 V
ADC supply voltage, 3.3 V (V_{DDA2}, V_{DDAIO}) ..... +3.14 V to +3.47 V
ADC supply voltage, 1.8 V (V_{DD1A18}, V_{DD2A18}) ..... +1.71 V to +1.89 V
Flash programming supply voltage, (V_{DD3VFL}) ..... +3.14 V to +3.47 V
Device clock frequency (system clock), ($f_{SYSCLKOUT}$) ..... 2 MHz to 100 MHz
High level input voltage, (V_{IH}) ..... +2.0 V to V_{DDIO}
Maximum low level input voltage, (V_{IL}) ..... 0.8 V
Maximum high level output source current, V_{OH} = 2.4 V (I_{OH}) :
All I/Os except group 2 ..... -4 mA
Group 2 6/ ..... -8 mA
Maximum low level output sink current, V_{OL} = V_{OL} max (I_{OL}) :
All I/Os except group 2 ..... 4 mA
Group 2 6/ ..... 8 mA
Ambient temperature, (T_A) ..... -55°C to +125°C
Thermal resistance characteristics for case outline X:

Parameter	Air Flow			
	0 lfm	150 lfm	250 lfm	500lfm
θ_{JA}[°C/W] High k PCB	48.16	40.06	37.96	35.17
Ψ_{JT}[°C/W]	0.3425	0.85	1.0575	1.410
θ_{JC}	12.89			
θ_{JB}	29.58			

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ All voltage values are with respect to V_{SS}, unless otherwise noted.
4/ Continuous clamp current per pin is ±2 mA. This includes the analog inputs which have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA2} or below V_{SSA2}
5/ Long term high temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life.
6/ Group 2 pins are as follows: GPIO28, GPIO29, GPIO30, GPIO31, TDO, XCLOUT, EMU0, and EMU1.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.astm.org.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.5 Package life time versus operating junction temperature. The package life time versus operating junction temperature shall be as specified in figure 4.

3.5.6 Typical operational power versus frequency (for device type 01). The typical operational power versus frequency (for device type 01) shall be as specified in figure 5.

3.5.7 Test load circuits. The test load circuits shall be as specified in figure 6.

3.5.7 Timing waveforms. The timing waveforms shall be as shown in figures 7- 27

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/		Limits		Unit
					Min	Max	
High level output voltage		V_{OH}	$I_{OH} = I_{OH\ max}$		2.4		V
			I_{OH} = 50 µA		V_{DDIO} – 0.2		
Low level output voltage		V_{OL}	$I_{OL} = I_{OL\ max}$			0.4	V
Low level input current	With pull up	I_{IL}	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)	-80	-190	µA
	Pull up disabled		V_{DDIO} = 3.3 V, V_{IN} = 0 V			±2	
High level input current	With pull up	I_{IH}	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$			±2	µA
	Pull up disabled				38	80	
Off state output current, high impedance state (off state)		I_{OZ}	$V_O = V_{DDIO}$ or 0 V			±2	µA
Input capacitance		C_i			2 Typ		pF

Current consumption by power supply pins at 100 MHz SYSCLOUT - Device type 01

Mode	Test condition	I_{DD}		I_{DDIO} 3/		I_{DD3VFL}		I_{DDA18} 4/		I_{DDA33} 5/	
		Typ 6/	Max	Typ 6/	Max	Typ	Max	Typ 6/	Max	Typ 6/	Max
Operational (Flash)	7/	195 mA	230 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	8/	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
SWTANDBY	9/	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	10/	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

Current consumption by power supply pins at 100 MHz SYSCLOUT - Device type 02

Operational (Flash)	7/	195 mA	230 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	8/	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
SWTANDBY	9/	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	10/	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

Current consumption by power supply pins at 100 MHz SYSCLOUT - Device type 03

Operational (Flash)	11/	180 mA	210 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	8/	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
SWTANDBY	9/	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	10/	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/		Limits		Unit
					Min	Max	
Clock table and Nonmenclature							
On-chip oscillator clock			$t_{c(OSC)}$, Cycle time		28.6	50	ns
			Frequency		20	35	MHz
XCLKIN 12/			$t_{c(CI)}$, Cycle time		10	250	ns
			Frequency		4	100	MHz
SYSCLKOUT			$t_{c(SCO)}$, Cycle time		10	500	ns
			Frequency		2	100	MHz
XCLKOUT			$t_{c(XCO)}$, Cycle time		10	2000	ns
			Frequency		0.5	100	MHz
HSPCLK 13/			$t_{c(HCO)}$, Cycle time		10		ns
			Frequency			100	MHz
LSPCLK 13/			$t_{c(LCO)}$, Cycle time		10		ns
			Frequency			100	MHz
ADC clock			$t_{c(ADCCLK)}$, Cycle time		80		ns
			Frequency			12.5	MHz
Input clock frequency							
	Input clock frequency	f_x	Resonator		20	35	MHz
			Crystal		20	35	
			External oscillator/clock Source (XCLKIN or X1 pin)	Without PLL	4	100	
				With PLL	5	30	
	Limp mode clock frequency	f_l			1-5 Typ		
XCLKIN 14/ timing requirements – PLL Enabled							
C8	Cycle time, XCLKIN	$t_{c(CI)}$	See figure 7		33.3	200	ns
C9	Fall time, XCLKIN	$t_{f(CI)}$				6	
C10	Rise time, XCLKIN	$t_{r(CI)}$				6	
C11	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	$t_{w(CIL)}$			45	55	%
C12	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	$t_{w(CIH)}$			45	55	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/		Limits		Unit
					Min	Max	
XCLKIN 14/ timing requirements – PLL disabled							
C8	Cycle time, XCLKIN	$t_{c(CI)}$	See figure 7		10	250	ns
C9	Fall time, XCLKIN	$t_{f(CI)}$		Up to 20 MHz		6	
				20 MHz to 100 MHz		2	
C10	Rise time, XCLKIN	$t_{r(CI)}$		Up to 20 MHz		6	
				20 MHz to 100 MHz		2	
C11	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	$t_{w(CIL)}$		XCLKIN ≤ 120 MHz	45	55	%
C12	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	$t_{w(CIH)}$		XCLKIN ≤ 120 MHz	45	55	
XCLKOUT Switching characteristics (PLL Bypassed or Enabled) 15/ 16/							
C1	Cycle time, XCLKOUT	$t_{c(XCO)}$	See figure 7		10		ns
C3	Fall time, XCLKOUT	$t_{f(XCO)}$			2 Typ		
C4	Rise time, XCLKOUT	$t_{r(XCO)}$			2 Typ		
C5	Pulse duration, XCLKOUT low	$t_{w(XCOL)}$			H-2	H+2	
C6	Pulse duration, XCLKOUT high	$t_{w(XCOH)}$			H-2	H+2	
	PLL lock time	t_p				$131072t_{c(OSCCLK)}$ 17/	cycles
Reset ($\overline{XRS}$) timing requirements							
	Pulse duration, stable XCLKIN to $\overline{XRS}$ high	$t_{w(RSL1)}$ 18/	See figure 8-10		$8t_{c(OSCCLK)}$		cycles
	Pulse duration, $\overline{XRS}$ low	$t_{w(RSL2)}$		Warm reset	$8t_{c(OSCCLK)}$		
	Pulse duration, reset pulse generated by watchdog	$t_{w(WDRS)}$			$512t_{c(OSCCLK)}$ Typ		
	Delay time, address/data valid after $\overline{XRS}$ high	$t_{d(EX)}$			$32t_{c(OSCCLK)}$ Typ		
	Oscillator start-up time	t_{OSCT} 19/			1	10	ms
	Hold time for boot mode pins	$t_{h(boot-mode)}$			$200t_{c(OSCCLK)}$		cycles

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
GENERAL PURPOSE INPUT/OUTPUT (GPIO)					
General purpose output switching characteristics (See figure 11)					
Rise time, GPIO switching low to high	$t_{r(GPO)}$	All GPIOs		8	ns
Fall time, GPIO switching high to low	$t_{f(GPO)}$	All GPIOs		8	
Toggling frequency, GPO pins	f_{GPO}			25	MHz
General purpose input timing requirements (See figure 12-13)					
Sampling period	$t_{w(SP)}$	QUALPDR = 0	$2*t_{c(SCO)}$		cycles
		QUALPDR ≠ 0	$2*t_{c(SCO)}*QUALPRD$		
Input qualifier sampling window	$t_{w(IQSW)}$		$t_{w(SP)}*(n^{20/}-1)$		
Pulse duration, GPIO low/high	$t_{r(GPI)}$ 21/	Synchronous mode	$2*t_{c(SCO)}$		
		With input qualifier	$t_{w(IQSW)}+ t_{w(SP)}+1t_{c(SCO)}$		
LOW POWER MODE WAKEUP TIMING					
IDLE mode timing requirements 22/ (See figure 14)					
Pulse duration, external wake up signal	$t_{w(WAKE-INT)}$	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW}$		
IDLE mode switching characteristics 22/					
Delay time, external wake signal to program execution resume 11/	$t_{d(WAKE-IDLE)}$				
- Wake up from Flash - Flash module in active state		Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)} + t_{w(IQSW)}$	
- Wake up from Flash - Flash module in sleep state		Without input qualifier		$1050t_{c(SCO)}$	cycles
		With input qualifier		$1050t_{c(SCO)}+ t_{w(IQSW)}$	
- Wake up from SARAM		Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)}+ t_{w(IQSW)}$	
STANDBY mode timing requirements (See figure 15)					
Pulse duration, external wake up signal	$t_{w(WAKE-INT)}$	Without input qualification	$3t_{c(OSCCLK)}$		cycles
		With input qualification 24/	(2+QUALSTDBY)* $t_{c(OSCCLK)}$		
STANDBY mode switching characteristics (See figure 15)					
Delay time, IDLE instruction executed to XCLKOUT low	$t_{d(IDLE-XCOL)}$		$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
Delay time, external wake signal to program execution resume 23/					
- Wake up from Flash - Flash module in active state	$t_{d(WAKE-STBY)}$	Without input qualifier		$100t_{c(SCO)}$	
		With input qualifier		$100t_{c(SCO)}+ t_{w(WAKE-INT)}$	
- Wake up from Flash - Flash module in sleep state		Without input qualifier		$1125t_{c(SCO)}$	
		With input qualifier		$1125t_{c(SCO)}+ t_{w(WAKE-INT)}$	
- Wake up from SARAM		Without input qualifier		$100t_{c(SCO)}$	
		With input qualifier		$100t_{c(SCO)}+ t_{w(WAKE-INT)}$	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
LOW POWER MODE WAKEUP TIMING - Continued					
HALT mode timing requirements					
Pulse duration, GPIO wake up signal	$t_{w(WAKE-GPIO)}$	See figure 16	$t_{OSCST}+2t_{c(OSCCLK)}$ 25/		cycles
Pulse duration, $\overline{XRS}$ wake up signal	$t_{w(WAKE-XRS)}$		$t_{OSCST}+8t_{c(OSCCLK)}$		
HALT mode switching characteristics					
Delay time, IDLE instruction executed to XCLKOUT low	$t_{d(IDLE-XCOL)}$	See figure 16	$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
PLL lock up time	t_p			$131072t_{c(OSCCLK)}$	
Delay time, PLL lock to program execution resume • Wake up from flash - Flash module in sleep state	$t_{d(WAKE-HALT)}$			$1125t_{c(SCO)}$	
• Wake up from SARM				$35t_{c(SCO)}$	
ENHANCED CONTROL PERIPHERALS					
ePWM timing requirements 22/					
Sync input pulse width	$t_{w(SYCIN)}$	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		
		With input qualifier	$1t_{c(SCO)}+ t_{w(IQSW)}$		
ePWM switching characteristics					
Pulse duration, PWMx output high/low	$t_{w(PWM)}$		20		ns
Sync output pulse width	$t_{w(SYCOUT)}$		$8t_{c(SCO)}$		cycles
Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced high	$t_{d(PWM)tza}$	No pin load		25	ns
Delay time, trip input active to PWM Hi-Z	$t_{d(TZ-PWM)HZ}$			20	
Trip zone input timing requirements 22/					
Pulse duration, $\overline{TZx}$ input low	$t_{w(TZ)}$	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		
		With input qualifier	$1t_{c(SCO)}+ t_{w(IQSW)}$		
High resolution PWM characteristics at SYSCLOUT = (60 – 100 MHz)					
Micro edge positioning (MEP) step size 26/				310	ps
Enhanced capture (eCAP) timing requirement 22/					
Capture input pulse width	$t_{w(CAP)}$	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		
		With input qualifier	$1t_{c(SCO)}+ t_{w(IQSW)}$		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
ENHANCED CONTROL PERIPHERALS – Continued					
eCAP switching characteristics					
Pulse duration, APWMx output high/ low	$t_{w(APWMX)}$		20		ns
Enhanced quadrature encoder pulse (eQEP) timing requirements 22/					
QEP input period	$t_{w(QEPP)}$	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2(1t_{c(SCO)}+ t_{w(IQSW)})$		
QEP index input high time	$t_{w(INDEXH)}$	Asynchronous/synchronous	$2t_{c(SCO)}$		
		With input qualifier	$2t_{c(SCO)}+ t_{w(IQSW)}$		
QED index input low time	$t_{w(INDEXL)}$	Asynchronous/synchronous	$2t_{c(SCO)}$		
		With input qualifier	$2t_{c(SCO)}+ t_{w(IQSW)}$		
QED strobe high time	$t_{w(STROBH)}$	Asynchronous/synchronous	$2t_{c(SCO)}$		
		With input qualifier	$2t_{c(SCO)}+ t_{w(IQSW)}$		
QED strobe input low time	$t_{w(STROBL)}$	Asynchronous/synchronous	$2t_{c(SCO)}$		
		With input qualifier	$2t_{c(SCO)}+ t_{w(IQSW)}$		
eQEP switching characteristics					
Delay time, external clock to counter increment	$t_{d(CNTR)xin}$			$4t_{c(SCO)}$	cycles
Delay time, QEP input edge to position compare sync output	$t_{d(PXCSOUT)QEP}$			$6t_{c(SCO)}$	
External ADC start of conversion switching characteristics					
Pulse duration, $\overline{\text{ADCSOCAO}}$ low	$t_{w(ADCSOCAL)}$	See figure 18	$32t_{c(HCO)}$		cycles
EXTERNAL INTERRUPT TIMING					
External interrupt timing requirements 22/					
Pulse duration, INT input high/ low	$t_{w(INT)}$	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)}+ t_{w(IQSW)}$		
External interrupt switching characteristics 22/					
Delay time, INT low/high to interrupt vector fetch	$t_{d(INT)}$	See figure 19		$12t_{c(SCO)}+ t_{w(IQSW)}$	cycles
I2C ELECTRICAL SPECIFICATION AND TIMING					
I2C timing					
SCL clock frequency	f_{SCL}	27/		400	kHz
Low level input voltage	V_{IL}			$0.3 V_{DDIO}$	V
High level input voltage	V_{IH}		$0.7 V_{DDIO}$		
Input hysteresis	V_{HYS}		$0.05 V_{DDIO}$		
Low level output voltage	V_{OL}	3 mA sink current	0	0.4	
Low period of SCL clock	t_{LOW}	27/	1.3		µs
High period of SCL clock	t_{HIGH}	27/	0.6		
Input current with an input voltage between $0.1 V_{DDIO}$ and $0.9 V_{DDIO}$ MAX	I_I		-10	10	µA

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Min	Max	Min	Max	
SPI MASTER MODE TIMING								
SPI master mode external timing (clock phase = 0) 35/ 36/ 37/ 38/ 39/				SPI when (SPIBRR+1) is even or SPIBRR = 0 or 2		SPI when (SPIBRR+1) is odd and SPIBRR > 3		
1	Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 20	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$		28/	29/	31/	32/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$		28/	29/	31/	32/	
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$		28/	29/	31/	32/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$		28/	29/	31/	32/	
4	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)	$t_{d(SPCH-SIMO)M}$			10		10	
	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)	$t_{d(SPCL-SIMO)M}$			10		10	
5	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)M}$		28/		33/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)M}$		28/		33/		
8	Setup time, SPIOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$		35		35		
	Setup time, SPIOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$		35		35		
9	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SOMI)M}$		30/		31/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SOMI)M}$		30/		31/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Min	Max	Min	Max	
SPI MASTER MODE TIMING - Continued								
SPI master mode external timing (clock phase = 1)) 35/ 36/ 37/ 38/ 39/				SPI when (SPIBRR+1) is even or SPIBRR = 0 or 2		SPI when (SPIBRR+1) is odd and SPIBRR > 3		
1	Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 21	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$		28/	29/	31/	32/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$		28/	29/	31/	32/	
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$		28/	29/	31/	32/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$		28/	29/	31/	32/	
6	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)M}$		28/		28/		
	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)M}$		28/		28/		
7	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SIMO)M}$		28/		28/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCL-SIMO)M}$		28/		28/		
10	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)M}$		35		35		
	Setup time, SPIOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)M}$		35		35		
11	Valid time, SPISOMI data valid after SPICLK high(clock polarity = 0)	$t_{v(SPCH-SOMI)M}$		30/		28/		
	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)M}$		30/		28/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/		Limits		Unit
					Min	Max	
	SPI SLAVE MODE TIMING						
SPI slave mode external timing (clock phase = 0) 36/ 37/ 38/ 39/ 46/							
12	Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 22		$4t_{c(LCO)}$		ns
13	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$			40/	41/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$			40/	41/	
14	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$			40/	41/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$			40/	41/	
15	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)	$t_{d(SPCH-SOMI)S}$				35	
	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)	$t_{d(SPCL-SOMI)S}$				35	
16	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$			42/		
	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$			42/		
19	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$			35		
	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$			35		
20	Valid time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)S}$			41/		
	Valid time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)S}$			41/		
SPI slave mode external timing (clock phase = 1) 20/ 21/							
12	Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 23		$8t_{c(LCO)}$		ns
13	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$			40/	41/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$			40/	41/	
14	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$			40/	41/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$			40/	41/	
17	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)S}$			43/		
	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)S}$			43/		
18	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$			42/		
	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$			42/		
21	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)S}$			35		
	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)S}$			35		
22	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SIMO)S}$			41/		
	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SIMO)S}$			41/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
ON CHIP ANALOG TO DIGITAL CONVERTER					
ADC electrical characteristics – DC specifications 47/ 48/					
Resolution			12		Bits
ADC clock			1		kHz
				12.5	MHz
Accuracy					
INL (integral nonlinearity)		1- 12.5 MHz ADC clock (6.25 MSPS)		±1.5	LSB
DNL (Differential nonlinearity) 49/		1- 12.5 MHz ADC clock (6.25 MSPS)		±1	
Offset error 50/			-60	+60	
Offset error with hardware trimming			±4 Typ		
Overall gain error with internal reference 51/			-60	+60	
Overall gain error with external reference		If ADCREFP-ADCREFM = 1 V ±0.1%	-60	+60	
Channel to channel offset variation			±4 Typ		
Channel to channel Gain variation			±4 Typ		
Analog input					
Analog input voltage (ADCINx to ADCLO) 52/			0	3	V
ADCLO			-5	5	mV
Input capacitance			10 Typ		pF
Input leakage current				±5	µA
Internal Voltage reference 51/					
$V_{ADCREFP}$ – ADCREFP output voltage at the pin based on internal reference			1.275 Typ		V
$V_{ADCREFP}$ – ADCREFM output voltage at the pin based on internal reference			0.525 Typ		
Voltage difference, ADCREFP-ADCREFM			0.75 Typ		
Temperature coefficient			50 Typ		PPM/°C
External Voltage reference 51/ 53/					
$V_{ADCREFIN}$ – External reference voltage input on ADCREFIN pin 0.2% or better accurate reference recommended		ADCREFSEL[15:14] = 11b	1.024 Typ		V
		ADCREFSEL[15:14] = 11b	1.500 Typ		
		ADCREFSEL[15:14] = 11b	2.048 Typ		
AC specifications					
Signal to noise ratio + distortion	SINAD (100 KHz)		67.5 Typ		dB
Signal to noise ratio	SNR (100KHz)		68 Typ		
Total harmonic distortion	THD (100 KHz)		-70 Typ		
Effective number of bits	ENOB 100 KHz)		10.9 Typ		Bits
Spurious free dynamic range	SFDR 100 KHz)		83 Typ		dB

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
ON CHIP ANALOG TO DIGITAL CONVERTER - Continued					
ADC power up Delays 54/					
Delay time for band gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled	$t_{d(BGR)}$	See figure 24-25	5 Typ		ms
Delay time for power down control to be stable. Bit delay time for band gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled. Bit 5 of the ADCTRL3 register (PWDNADC) is to be set to 1 before any ADC conversions are initiated	$t_{d(PWD)}$		20		µs
				1	ms
Sequential sampling mode timing See figure 26					
		Sample n	Sample n + 1	55/	
Delay time from even trigger to sampling	$t_{d(SH)}$	$2.5t_{c(ADCCLK)}$			ns
Sample/Hold width/Acquisition width	t_{SH}	(1+Acqps)* $t_{c(ADCCLK)}$		80 ns with Acqps = 0 Typ 56/	
Delay time for first result to appear in the Result register	$t_{d(schx\_n)}$	$4t_{c(ADCCLK)}$		320 Typ	
Delay time for successive results to appear in the Result register	$t_{d(schx\_n+1)}$		(2+Acqps)* $t_{c(ADCCLK)}$	160 Typ	
Simultaneous sampling mode timing See figure 27					
		Sample n	Sample n + 1	55/	
Delay time from even trigger to sampling	$t_{d(SH)}$	$2.5t_{c(ADCCLK)}$			ns
Sample/Hold width/Acquisition width	t_{SH}	(1+Acqps)* $t_{c(ADCCLK)}$		80 ns with Acqps = 0 Typ	
Delay time for first result to appear in the Result register	$t_{d(schA0\_n)}$	$4t_{c(ADCCLK)}$		320 Typ	
Delay time for first result to appear in the Result register	$t_{d(schB0\_n)}$	$5t_{c(ADCCLK)}$		400 Typ	
Delay time for successive result to appear in the Result register	$t_{d(schA0\_n+1)}$		(3+Acqps)* $t_{c(ADCCLK)}$	240 Typ	
Delay time for successive results to appear in the Result register	$t_{d(schB0\_n+1)}$		(3+Acqps)* $t_{c(ADCCLK)}$	240 Typ	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Test condition 2/	Limits		Unit
				Min	Max	
FLASH TIMING						
Flash endurance						
Flash endurance for the array (Write/erase cycles)		N_f	-55°C to 125°C	100		cycles
OTP endurance for the array (Write cycles)		N_{OTP}	-55°C to 125°C		1	write
Flash parameters at 150 MHz SYSCLKOUT 58/						
Program time	16 Bit Word			50 Typ		µs
	16K Sector			500 Typ		ms
	8K sector			250 Typ		ms
	4K Sector			120 Typ		ms
Erase time	16K Sector			10 Typ		S
	8K sector			10 Typ		S
	4K Sector			10 Typ		S
VDD3VFL current consumption during the Erase/Program cycle	Erase	$I_{DD3VFLP}$		75 Typ		mA
	Program			35 Typ		
V_{DD} current consumption during the Erase/Program cycle		I_{DDP}		140 Typ		
V_{DDIO} current consumption during the Erase/Program cycle		I_{DDIOP}		20 Typ		
Flash/OTP access timing 59/						
Paged Flash access time		$t_{a(fp)}$		36		ns
Random access time		$t_{a(fr)}$		36		
OTP access time		$t_{a(OTP)}$		60		

Minimum required Wait States at different frequencies

SYSCLKOUT (MHz)	**SYSCLKOUT** (ns)	**Page Wait state** 60/	**Random Wait state** 60/ 61/
100	10.00	3	3
75	13.33	2	2
50	20.00	1	1
30	33.33	1	1
25	40.00	0	1
15	66.67	0	1
4	250.00	0	1

See notes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Test conditions are over recommended ranges of supply voltage and operating case temperature unless otherwise specified. Device type: All.
3/ I_{DDIO} current is dependent on the electrical loading on the I/O pins.
4/ I_{DDA18} includes current into V_{DD1A18} and V_{DD2A18} pins.
5/ I_{DDA33} includes current into V_{DDA2} and V_{DDAIO} pins.
6/ The Typ numbers are applicable over room temperature and nominal voltage.
7/ The following peripheral clocks are enabled:
ePWM 1/2/3/4/5/6, eCAP 1/2/3/4, eQEP1/ 2, eCAN-A, SCI-A/B, SPI-A, ADC, I^2C
All PWM pins are toggled at 100 KHz. Data is continuous transmitted out of the SCI-A, SCI-B, and eCAN-A ports. The hardware multiplier is exercised. Code is running out of flash with 3 wait states. XCLKOUT is turned off.
8/ Flash is powered down. XCLKOUT is turned off. The following peripheral clocks are enabled:
eCAN-A, SCI-A, SPI-A, I^2C
9/ Flash is powered down. Peripheral clocks are off.
10/ Flash is powered down. Peripheral clocks are off. Input clock is disabled.
11/ The following peripheral clocks are enabled:
ePWM 1/2/3, eCAP 1/2, eQEP1, eCAN-A, SCI-A/B, SPI-A, ADC, I^2C
All PWM pins are toggled at 100 KHz. Data is continuous transmitted out of the SCI-A, SCI-B, and eCAN-A ports. The hardware multiplier is exercised. Code is running out of flash with 3 wait states. XCLKOUT is turned off.
12/ This also applied to the X1 pin if a 1.8 V oscillator is used.
13/ Lower LSPCLK and HSPCLK will reduce device power consumption.
14/ This applied to the X1 pin also.
15/ A load of 40 pF is assumed for these parameters.
16/ $H = 0.5t_{c(XCO)}$
17/ OSCCLK is either the output of the on-chip oscillator or the output from an external oscillator.
18/ In addition to the $t_{w(RSL1)}$ requirement, $\overline{XRS}$ has to be low at least for 1 ms after V_{DD} reaches 1.5 V.
19/ Dependent on crystal/resonator and board design.
20/ "n" represents the number of qualification samples as defined by GPxQSELn register.
21/ For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.
22/ For an explanation of the input qualifier parameters, see General purpose input timing requirements table.
23/ This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction, execution of an ISR (triggered by the wake up) signal involves addition latency.
24/ QUALSTDBY is a 6-bit field in the LPMCR0 register.
25/ See Rest ($\overline{XRS}$) timing requirements table for an explanation of t_{OSCST}.
26/ Maximum MEP step size is based on worst case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature. Applications that use the HRPWM feature should use MEP scale Factor Optimize (SFO) estimation software functions. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation. See manufacturer data for more information.
27/ I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately.
28/ $0.5t_{c(SPC)M} – 10$
29/ $0.5t_{c(SPC)M}$
30/ $0.25t_{c(SPC)M} – 10$
31/ $0.5t_{c(SPC)M} – 0.5t_{c(LCO)} – 10$
32/ $0.5t_{c(SPC)M} – 0.5t_{c(LCO)}$
33/ $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} – 10$
34/ $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$

35/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.

36/ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{LSPCLK}{4}$ or $\frac{LSPCLK}{(SPIBRR+1)}$

37/ $t_{c(LCO)}$ = LSPCLK cycle time.

38/ Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX
Slave mode transmit 12.5 MAX, slave mode receive 12.5 MHz MAX.

39/ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

40/ $0.5t_{c(SPC)S} - 10$

41/ $0.5t_{c(SPC)S}$

42/ $0.75t_{c(SPC)S}$

43/ $0.125t_{c(SPC)S}$

46/ The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.

47/ Tested at 12.5 MHz ADCCLK.

48/ All voltages listed in this table are with respect to V_{SSA2}.

49/ Manufacturer specifies that the ADC will have no missing codes.

50/ 1 LSB has the weight value of 3.0/4097 = 0.732 mV.

51/ A single internal/external band gap reference sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference. The total gain error listed for the internal reference depend on the temperature profile of the source used.

52/ Voltages above V_{DDA} + 0.3 or below V_{SS} – 0.3 applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.

53/ Manufacturer recommends using high precision external reference for 2.048 V reference.

54/ Timings maintain compatibility to the 281x ADC module. The 280x ADC also support driving all 3 bits at the same time and waiting $t_{d(BGR)}$ ms before first conversion.

55/ At 12.5 MHz ADC clock, $t_{c(ADCCLK)}$ = 80 ns.

56/ Acqps value = 0 – 15 ADCTRL1[8:11]

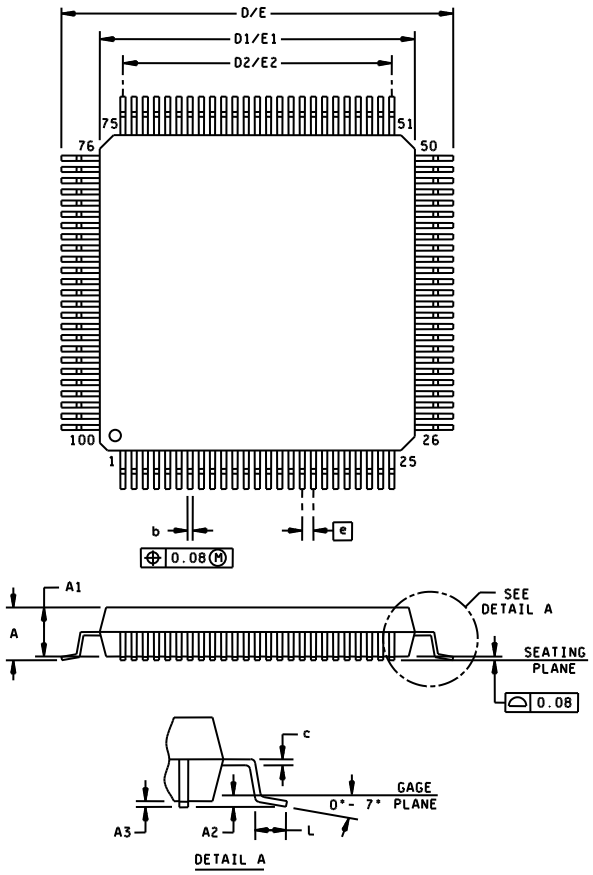
57/ Typical parameters as seen at room temperature using flash API version 3.00 including function call overhead.

58/ For 100 MHz, PAGE WS = 3 and RANDOM WS = 3
For 75 MHz, PAGE WS = 2 and RANDOM WS = 2
Formulas to compute page wait state and random wait state:

Page Wait State = $\left[\left(\frac{t_{a(fp)}}{t_{c(SCO)}}\right) - 1\right]$ (round up to the highest integer), or 0 whichever is larger

Random Wait State = $\left(\left[\frac{t_{a(fr)}}{t_{c(SCO)}}\right] - 1\right)$ round up to the highest integer), or 1 whichever is larger

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	15.80	16.20
A1	1.35	1.45	D1/E1	13.80	14.20
A2	0.25 Typ		D2/E2	12.00 Typ	
A3	0.05		e	0.50 Typ	
b	0.17	0.27	L	0.45	0.75
c	0.13 Nom				

Notes:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026

FIGURE 1. Case outlines.

Case X –Device type 01

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
1	GPIO12/ $\overline{\text{TZ1}}$ /CANTXB/SPISIMOB	35	ADCREFIN	68	V_{DD}
2	V_{SS}	36	ADCREFM	69	V_{SS}
3	V_{DDIO}	37	ADCREFP	70	GPIO11/EPWM6B/SCIRXDB/ ECAP4
4	GPIO29/SCITXDA/ $\overline{\text{TZ6}}$	38	ADCRESEXT	71	GPIO22/EQEP1S/SPICLKC/SCITXDB
5	GPIO33/SCLA/EPWMSYNCO/ $\overline{\text{ADCSOCBO}}$	39	$V_{SS2AGND}$	72	GPIO23/EQEP1I/SPISTEC/ SCIRXDB
6	GPIO30/CANRXA	40	V_{DD2A18}	73	TDI
7	GPIO31/CANTXA	41	V_{SS}	74	TMS
8	GPIO14/ $\overline{\text{TZ3}}$ /SCITXDB/SPICLKB	42	V_{DD}	75	TCK
9	GPIO15/ $\overline{\text{TZ4}}$ /SCITXDB/SPISTEB	43	GPIO34	76	TDO
10	V_{DD}	44	GPIO1/EPWM1B/SPISIMOD	77	V_{SS}
11	V_{SS}	45	GPIO2/EPWM2A	78	$\overline{\text{XRS}}$
12	V_{DD1A18}	46	V_{DDIO}	79	GPIO27/ECAP4/EQEP2S/SPIISTEB
13	$V_{SS1AGND}$	47	GPIO0/EPWM1A	80	EMU0
14	V_{SSA2}	48	GPIO2/EPWM2B/SPISOMID	81	EMU1
15	V_{DDA2}	49	V_{SS}	82	V_{DDIO}
16	ADCINA7	50	GPIO16/SPISIMOA/CANTXB/ $\overline{\text{TZ5}}$	83	GPIO24/ECAP1/EQEP2A/SPISIMOB
17	ADCINA6	51	GPIO4/EPWM3A	84	$\overline{\text{TRST}}$
18	ADCINA5	52	GPIO17/SPISOMIA/CANRXB/ $\overline{\text{TZ6}}$	85	V_{DD}
19	ADCINA4	53	GPIO5/EPWM3B/SPICLKD/ECAP1	86	X2
20	ADCINA3	54	GPIO18/SPICLKA/SCITXDB	87	V_{SS}
21	ADCINA2	55	V_{SS}	88	X1
22	ADCINA1	56	GPIO6/EPWM4A/EPWMSYNCI/EPWMSYNCO	89	V_{SS}
23	ADCINA0	57	GPIO19/SPISTEA/SCIRXDB	90	XCLKIN
24	ADCLO	58	GPIO7/EPWM4B/SPISTED/ECAP2	91	GPIO25/ECAP2/EQEP2B/SPISOMIB
25	V_{SSAIO}	59	V_{DD}	92	GPIO28/SCIRXDA/ $\overline{\text{TZ5}}$
26	V_{DDAIO}	60	GPIO8/EPWM5A/CANTXB/ $\overline{\text{ADCS0CAO}}$	93	V_{DD}
27	ADCINB0	61	GPIO9/EPWM5B/SCITXDB/ECAP3	94	V_{SS}
28	ADCINB1	62	V_{SS}	95	GPIO13/ $\overline{\text{TZ2}}$ /CANRXB/SPISOMIB
29	ADCINB2	63	GPIO20/EQEP1A/SPISIMOC/CANTXB	96	V_{DD3VFL}
30	ADCINB3	64	GPIO10/EPWM6A/CANRXB/ $\overline{\text{ADCSOCBO}}$	97	TEST1
31	ADCINB4	65	V_{DDIO}	98	TEST2
32	ADCINB5	66	XCLKOUT	99	GPIO26/ECAP3/EQEP2I/SPICLKB
33	ADCINB6	67	GPIO21/EQEP1B/SPISPMIC/CANRXB	100	GPIO32/SDAA/EPWMSYNCI/ $\overline{\text{ADCS0CAO}}$
34	ADCINB7				

FIGURE 2. Terminal connections.

Case X –Device type 02

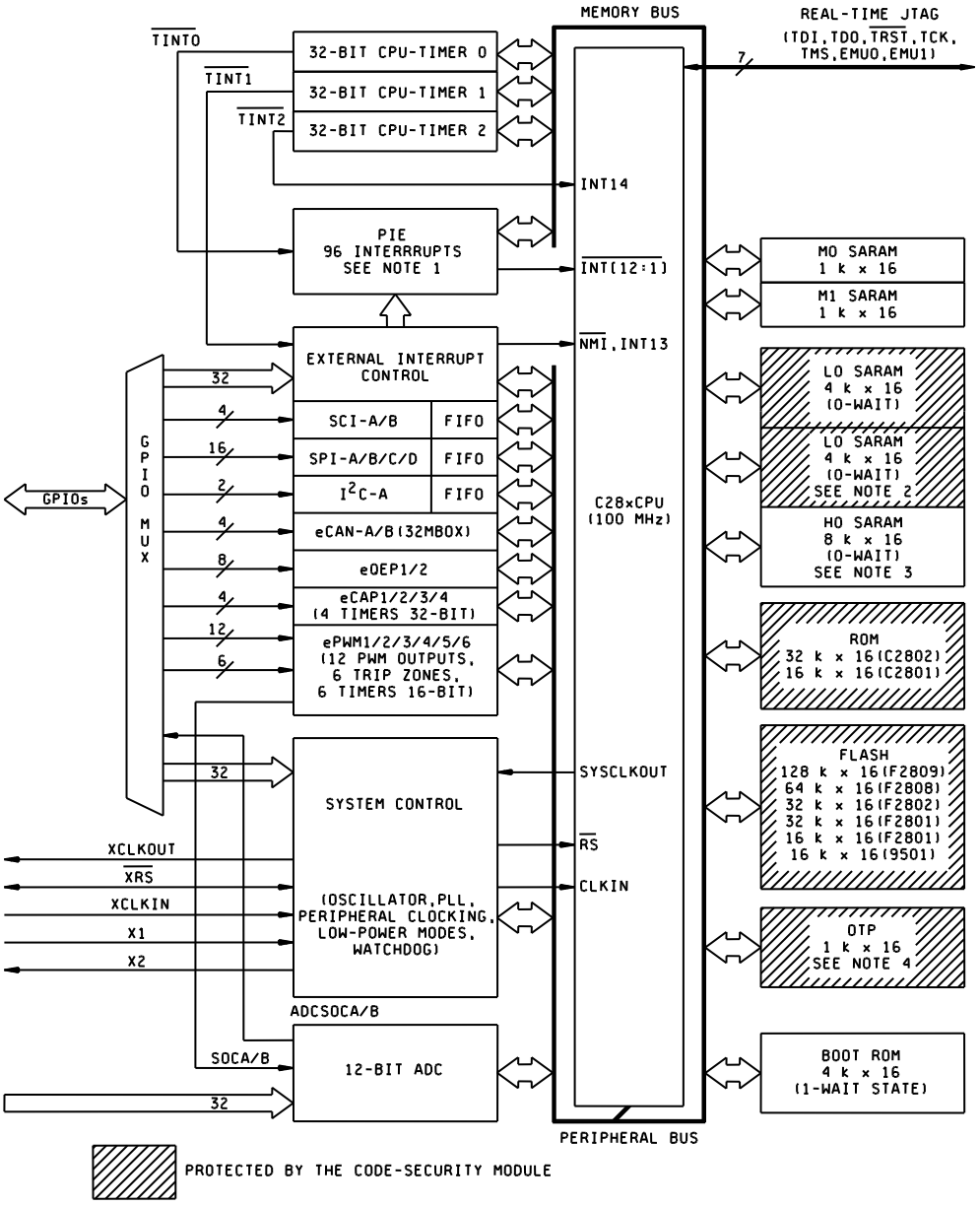
Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
1	GPIO12/ $\overline{\text{TZ1}}$ /SPISIMOB	35	ADCREFIN	68	V_{DD}
2	V_{SS}	36	ADCREFM	69	V_{SS}
3	V_{DDIO}	37	ADCREFP	70	GPIO11/EPWM6B/SCIRXDB/ ECAP4
4	GPIO29/SCITXDA/ $\overline{\text{TZ6}}$	38	ADCRESEXT	71	GPIO22/EQEP1S/SPICLKC/SCITXDB
5	GPIO33/SCLA/EPWMSYNCO/ $\overline{\text{ADCSOCBO}}$	39	$V_{SS2AGND}$	72	GPIO23/EQEP1I/SPISTEC/ SCIRXDB
6	GPIO30/CANRXA	40	V_{DD2A18}	73	TDI
7	GPIO31/CANTXA	41	V_{SS}	74	TMS
8	GPIO14/ $\overline{\text{TZ3}}$ /SCITXDB/SPICLKB	42	V_{DD}	75	TCK
9	GPIO15/ $\overline{\text{TZ4}}$ /SCITXDB/SPISTEB	43	GPIO34	76	TDO
10	V_{DD}	44	GPIO1/EPWM1B/SPISIMOD	77	V_{SS}
11	V_{SS}	45	GPIO2/EPWM2A	78	$\overline{\text{XRS}}$
12	V_{DD1A18}	46	V_{DDIO}	79	GPIO27/ECAP4/EQEP2S/SPIISTEB
13	$V_{SS1AGND}$	47	GPIO0/EPWM1A	80	EMU0
14	V_{SSA2}	48	GPIO2/EPWM2B/SPISOMID	81	EMU1
15	V_{DDA2}	49	V_{SS}	82	V_{DDIO}
16	ADCINA7	50	GPIO16/SPISIMOA/ $\overline{\text{TZ5}}$	83	GPIO24/ECAP1/EQEP2A/SPISIMOB
17	ADCINA6	51	GPIO4/EPWM3A	84	$\overline{\text{TRST}}$
18	ADCINA5	52	GPIO17/SPISOMIA/ $\overline{\text{TZ6}}$	85	V_{DD}
19	ADCINA4	53	GPIO5/EPWM3B/SPICLKD/ECAP1	86	X2
20	ADCINA3	54	GPIO18/SPICLKA/SCITXDB	87	V_{SS}
21	ADCINA2	55	V_{SS}	88	X1
22	ADCINA1	56	GPIO6/EPWM4A/EPWMSYNCI/EPWMSYNCO	89	V_{SS}
23	ADCINA0	57	GPIO19/SPISTEA/SCIRXDB	90	XCLKIN
24	ADCLO	58	GPIO7/EPWM4B/SPISTED/ECAP2	91	GPIO25/ECAP2/EQEP2B/SPISOMIB
25	V_{SSAIO}	59	V_{DD}	92	GPIO28/SCIRXDA/ $\overline{\text{TZ5}}$
26	V_{DDAIO}	60	GPIO8/EPWM5A/ $\overline{\text{ADCS0CAO}}$	93	V_{DD}
27	ADCINB0	61	GPIO9/EPWM5B/SCITXDB/ECAP3	94	V_{SS}
28	ADCINB1	62	V_{SS}	95	GPIO13/ $\overline{\text{TZ2}}$ /SPISOMIB
29	ADCINB2	63	GPIO20/EQEP1A/SPISIMOC	96	V_{DD3VFL}
30	ADCINB3	64	GPIO10/EPWM6A/ $\overline{\text{ADCSOCBO}}$	97	TEST1
31	ADCINB4	65	V_{DDIO}	98	TEST2
32	ADCINB5	66	XCLKOUT	99	GPIO26/ECAP3/EQEP2I/SPICLKB
33	ADCINB6	67	GPIO21/EQEP1B/SPISPMIC	100	GPIO32/SDAA/EPWMSYNCI/ $\overline{\text{ADCS0CAO}}$
34	ADCINB7				

FIGURE 2. Terminal connections - Continued.

Case X –Device type 03

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
1	GPIO12/ $\overline{\text{TZ1}}$ /SPISIMOB	35	ADCREFIN	68	V_{DD}
2	V_{SS}	36	ADCREFM	69	V_{SS}
3	V_{DDIO}	37	ADCREFP	70	GPIO11
4	GPIO29/SCITXDA/ $\overline{\text{TZ6}}$	38	ADCRESEXT	71	GPIO22/EQEP1S
5	GPIO33/SCLA/EPWMSYNCO/ $\overline{\text{ADCSOCBO}}$	39	$V_{SS2AGND}$	72	GPIO23/EQEP1I
6	GPIO30/CANRXA	40	V_{DD2A18}	73	TDI
7	GPIO31/CANTXA	41	V_{SS}	74	TMS
8	GPIO14/ $\overline{\text{TZ3}}$ /SPICLKB	42	V_{DD}	75	TCK
9	GPIO15/ $\overline{\text{TZ4}}$ /SPISTEB	43	GPIO34	76	TDO
10	V_{DD}	44	GPIO1/EPWM1B	77	V_{SS}
11	V_{SS}	45	GPIO2/EPWM2A	78	$\overline{\text{XRS}}$
12	V_{DD1A18}	46	V_{DDIO}	79	GPIO27/SPIISTEB
13	$V_{SS1AGND}$	47	GPIO0/EPWM1A	80	EMU0
14	V_{SSA2}	48	GPIO2/EPWM2B	81	EMU1
15	V_{DDA2}	49	V_{SS}	82	V_{DDIO}
16	ADCINA7	50	GPIO16/SPISIMOA/ $\overline{\text{TZ5}}$	83	GPIO24/ECAP1/SPISIMOB
17	ADCINA6	51	GPIO4/EPWM3A	84	$\overline{\text{TRST}}$
18	ADCINA5	52	GPIO17/SPISOMIA/ $\overline{\text{TZ6}}$	85	V_{DD}
19	ADCINA4	53	GPIO5/EPWM3B/ECAP1	86	X2
20	ADCINA3	54	GPIO18/SPICLKA	87	V_{SS}
21	ADCINA2	55	V_{SS}	88	X1
22	ADCINA1	56	GPIO6/EPWMSYNCI/EPWMSYNCO	89	V_{SS}
23	ADCINA0	57	GPIO19/SPISTEA	90	XCLKIN
24	ADCLO	58	GPIO7/ECAP2	91	GPIO25/ECAP2/SPISOMIB
25	V_{SSAIO}	59	V_{DD}	92	GPIO28/SCIRXDA/ $\overline{\text{TZ5}}$
26	V_{DDAIO}	60	GPIO8/ $\overline{\text{ADCS0CAO}}$	93	V_{DD}
27	ADCINB0	61	GPIO9	94	V_{SS}
28	ADCINB1	62	V_{SS}	95	GPIO13/ $\overline{\text{TZ2}}$ /SPISOMIB
29	ADCINB2	63	GPIO20/EQEP1A	96	V_{DD3VFL}
30	ADCINB3	64	GPIO10/ $\overline{\text{ADCSOCBO}}$	97	TEST1
31	ADCINB4	65	V_{DDIO}	98	TEST2
32	ADCINB5	66	XCLKOUT	99	GPIO26/SPICLKB
33	ADCINB6	67	GPIO21/EQEP1B	100	GPIO32/SDAA/EPWMSYNCI/ $\overline{\text{ADCS0CAO}}$
34	ADCINB7				

FIGURE 2. Terminal connections - Continued.



Notes:
1. 43 of the possible 96 interrupts are used on the devices.
2. Not available on the device type 03.
3. Not available on the device type 02 and 03.

FIGURE 3. Block diagram.

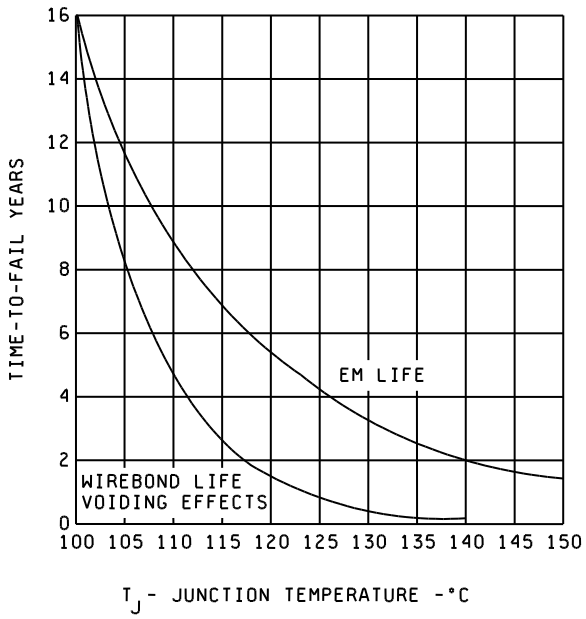
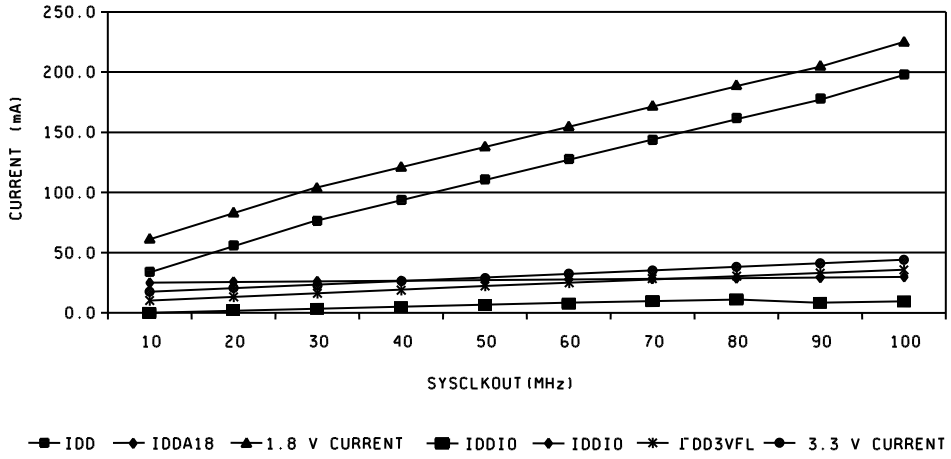


FIGURE 4. Package lifetime versus operating junction temperature.



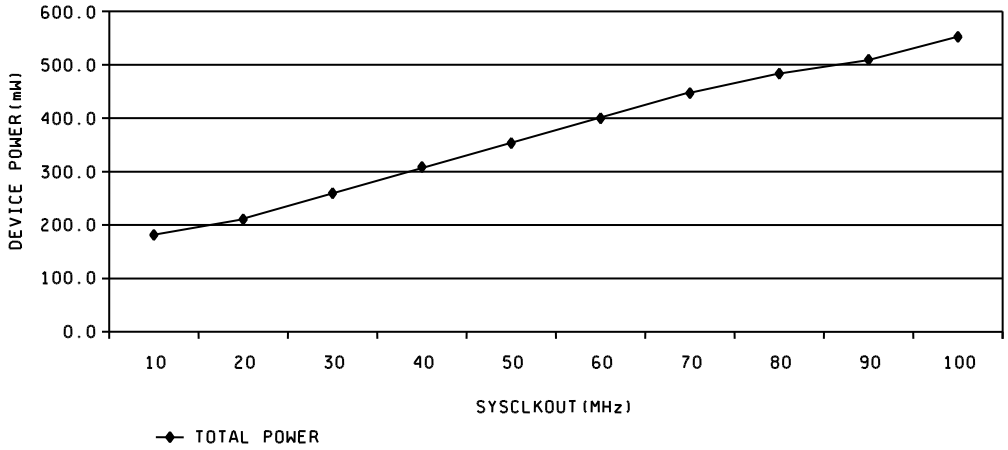
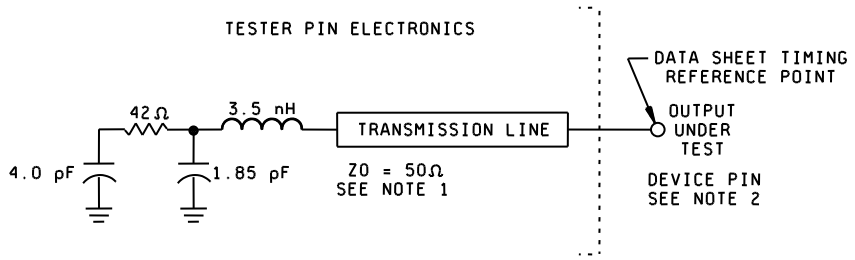


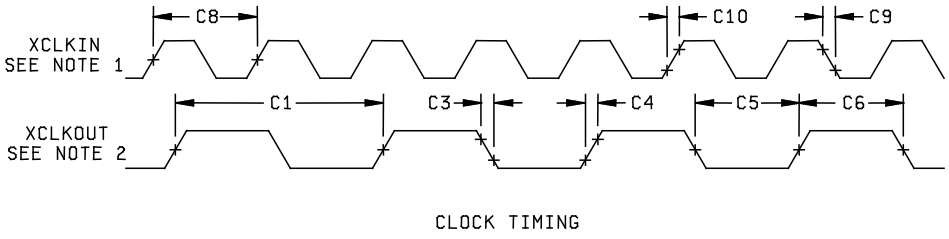
FIGURE 5. Typical operational power versus frequency (for device type 01).



Note:

1. Input requirements in the manufacturer are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.
2. The manufacturer data provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

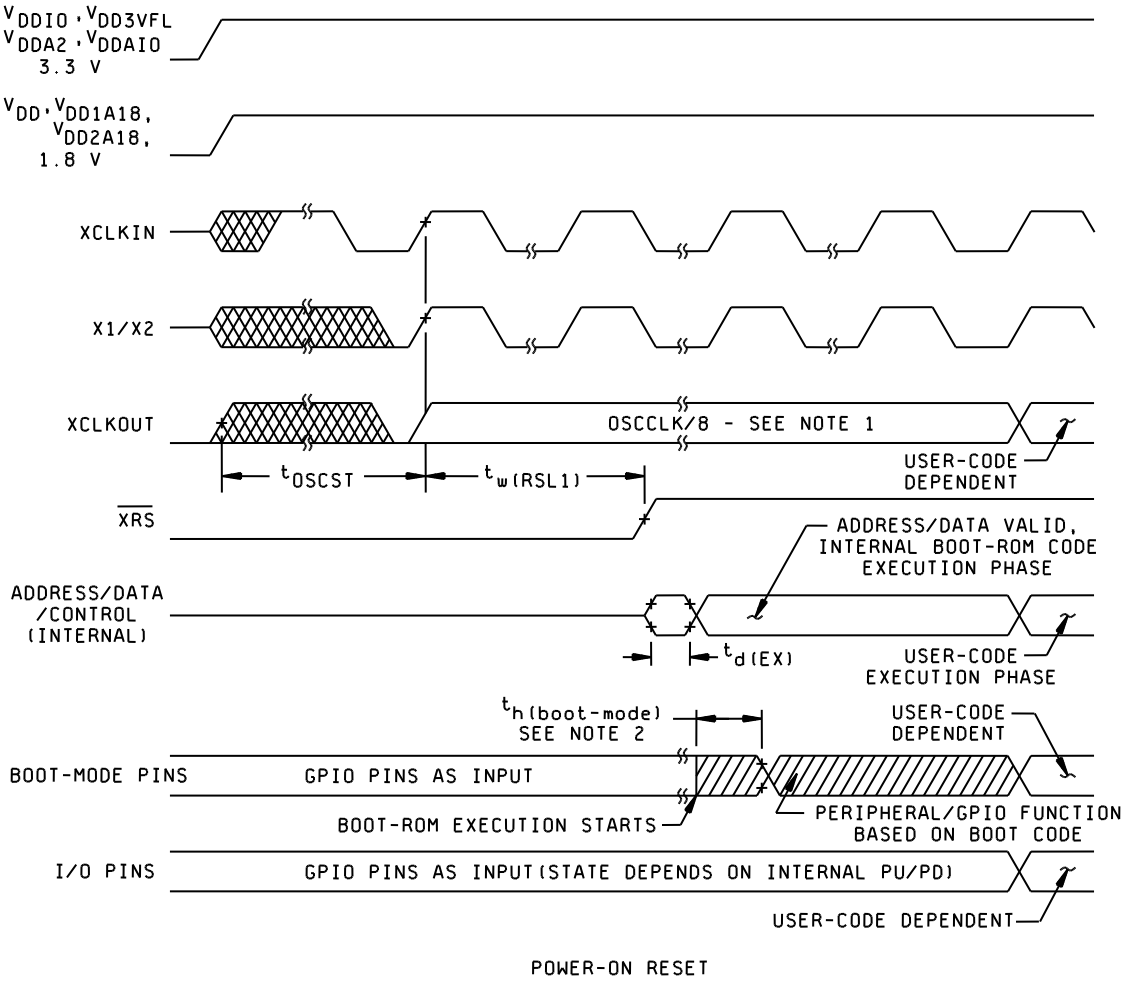
FIGURE 6. Test load circuit.



Note:

1. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship in this figure is intended to illustrate the timing parameters only and may differ based on configuration.
2. XCLKOUT configured to reflect SYSCLKOUT.

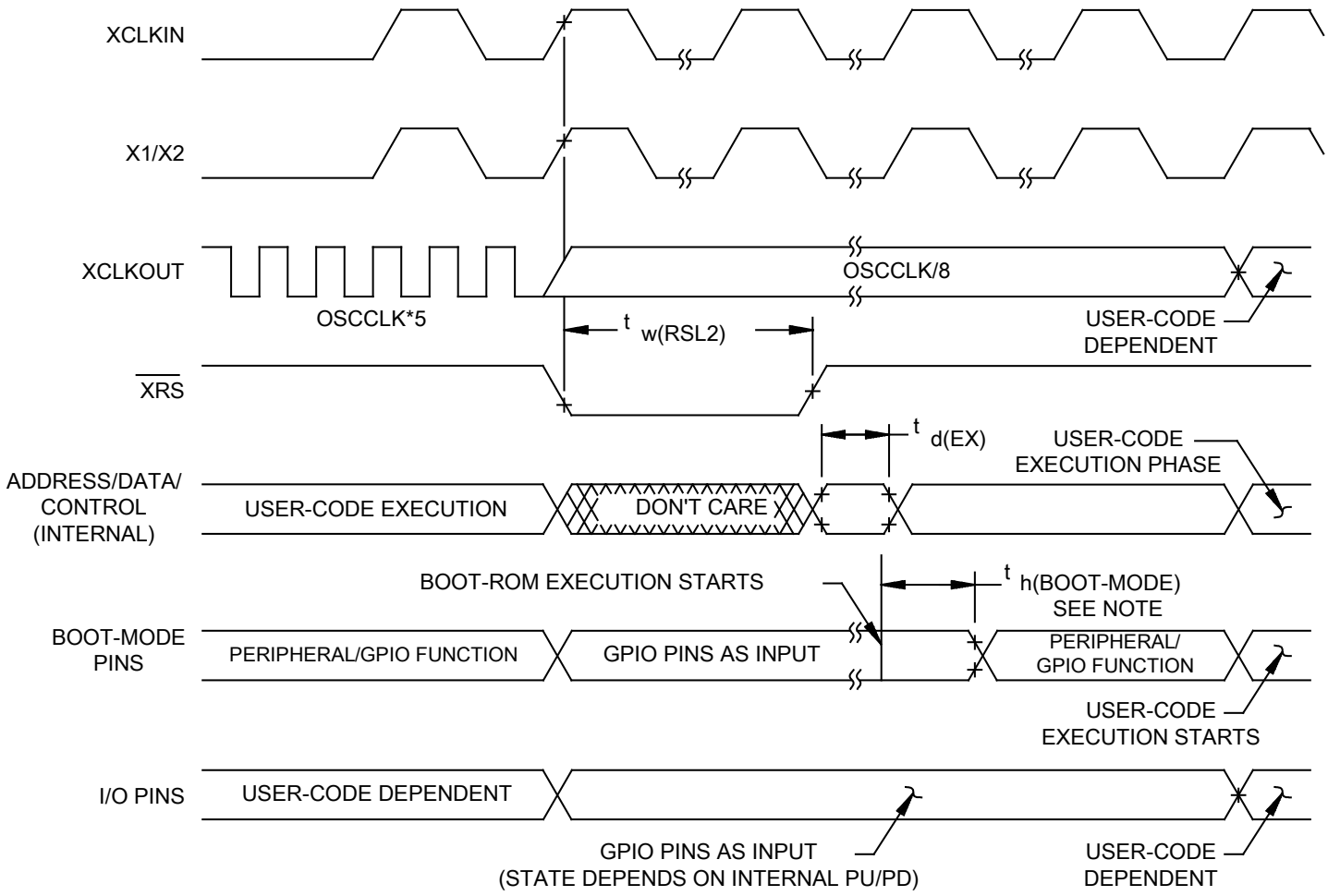
FIGURE 7 Timing waveforms.



Notes:

1. Upon power up, SYSCLKOUT is OSCCLK/2 Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = OSCCLK/8 during this phase.
2. After reset, the boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pins, the boot code branches to destination memory or boot code function. If boot ROM code executes after power on conditions (in debugger environment) the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

FIGURE 8 Timing waveforms.



WARM RESET

Notes:

1. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

FIGURE 9 Timing waveforms.

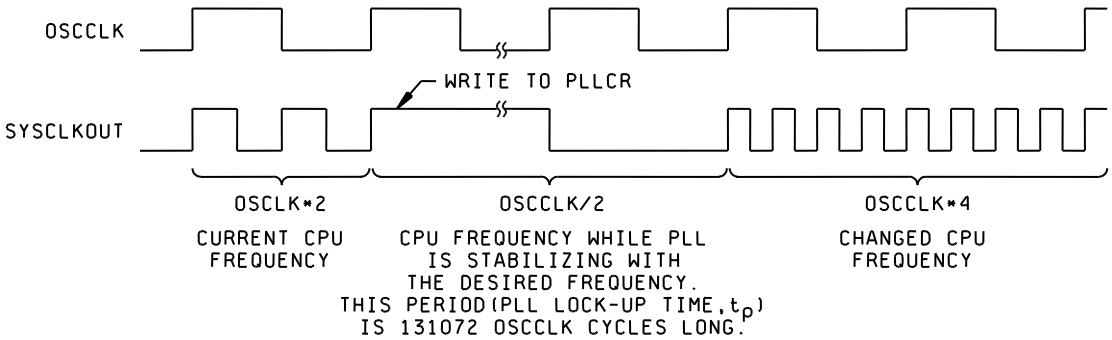


FIGURE 10 Timing waveforms.

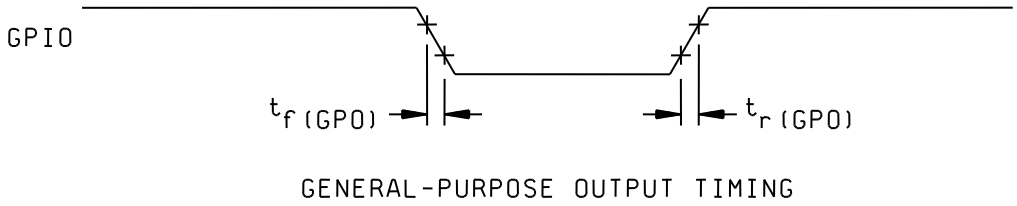
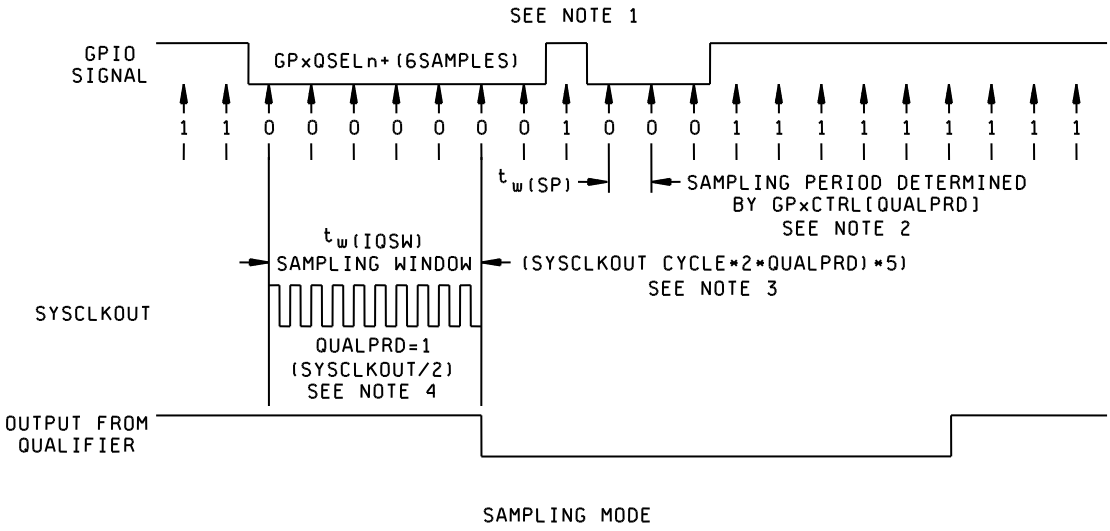


FIGURE 11 Timing waveforms.



Notes:

1. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value “n” the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2 n SYSCLKOUT cycles, the GPIO pin will be sampled).
2. The qualification period selected via GPxCTRL register applies to groups of 8 GPIO pins.
3. The qualification block can take either three or six samples. The GPxQSELn register selects which sample mode is used.
4. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2)SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT wide pulse ensures reliable recognition.

FIGURE 12 Timing waveforms.

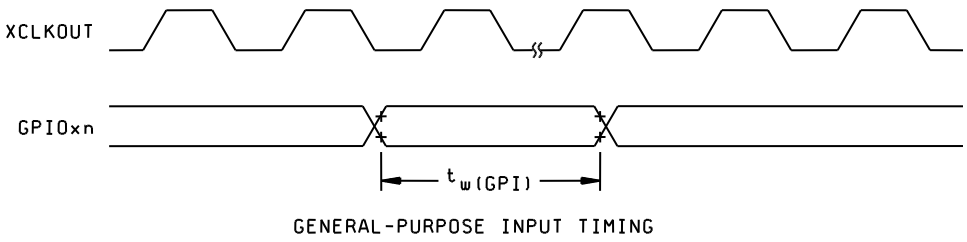
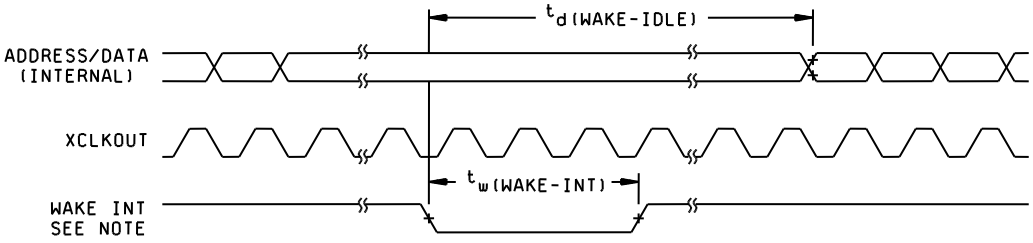


FIGURE 13 Timing waveforms.

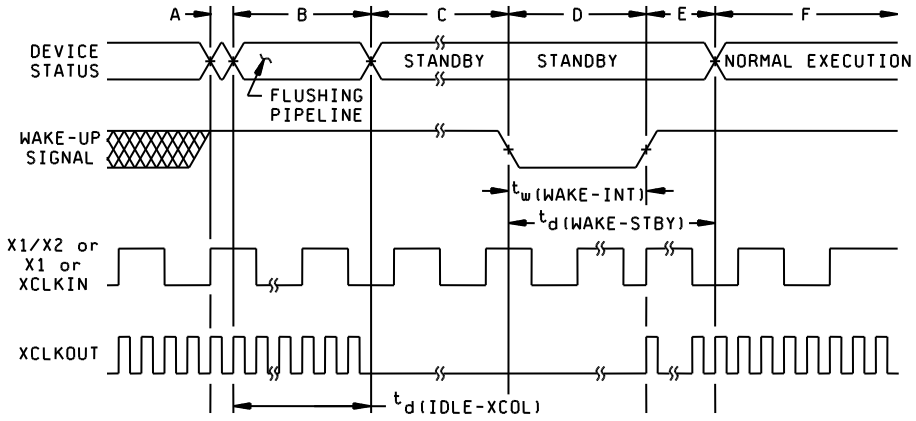


IDLE ENTRY AND EXIT TIMING

Note:

1. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$, XNMI, $\overline{\text{XRS}}$

FIGURE 14 Timing waveforms.

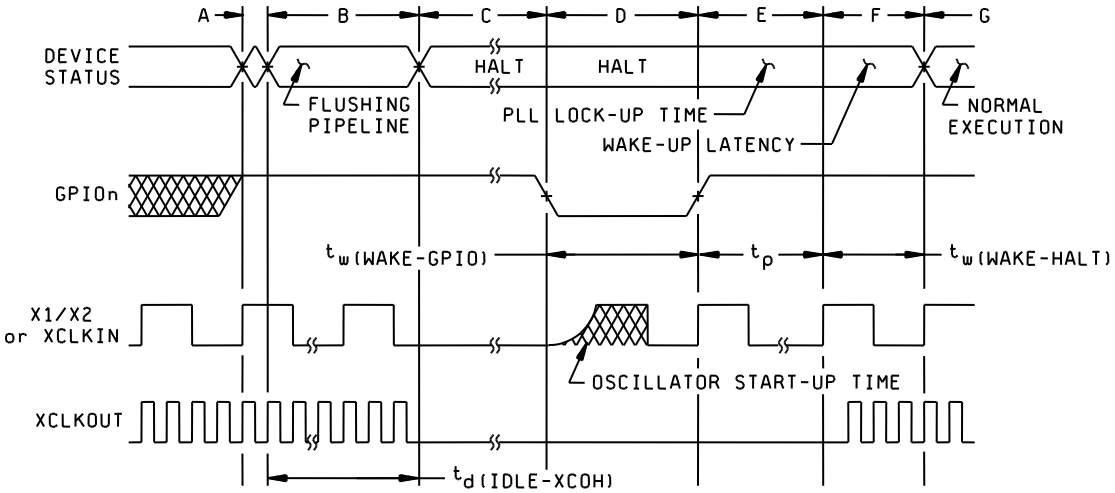


STANDBY ENTRY AND EXIT TIMING DIAGRAM

Notes:

1. IDLE instruction is executed to put the device into STANBY mode.
2. The PLL block respond to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles before being turned off. This 32 cycle delay enables the CPU pipe and any other pending operations to flush properly.
3. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.
4. The external wake up signal is driven active.
5. After a latency period, the STANDBY mode is excited.
6. Normal operation resumes. The device will respond to the interrupt (if enabled).

FIGURE 15 Timing waveforms.

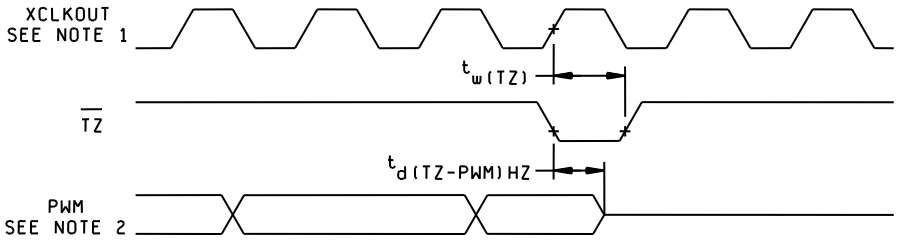


HALT WAKE UP USING GPIOn

Notes:

1. IDLE instruction is executed to put the device into HALT mode.
2. The PLL block responds to the HALT signal. SYSCLKOUT is held for another 32 cycles before the oscillator is tuned off and the CLKIN to the core is stopped. This 32 cycle delay enables the CPU pipe and any other pending operation to flush properly.
3. Clocks to the device are turned off and the internal oscillator and PLL are shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power.
4. When the GPIOn pin is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.
5. When XNMI is deactivated, it initiates the PLL lock sequence, which takes 131,072 OSCCLK(X1/X2 or X1 or XCLKIN) cycles.
6. When CLKIN to the core is enabled, the device will response to the interrupt (if enabled), after a latency. The HALT mode is now exited.
7. Normal operation resumes.

FIGURE 16 Timing waveforms.

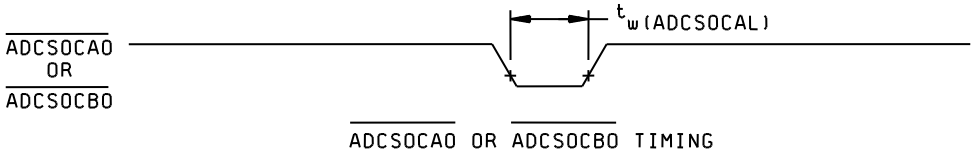


PWM HI-Z CHARACTERISTICS

Notes:

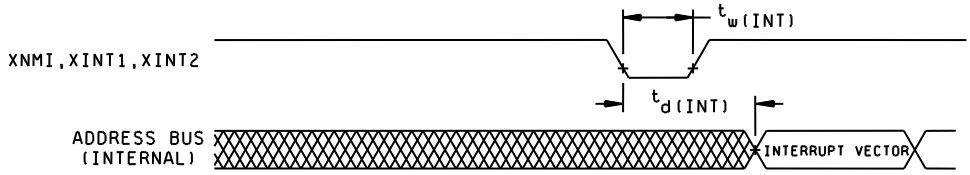
1. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$
2. PWM refers to all PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM

FIGURE 17 Timing waveforms.



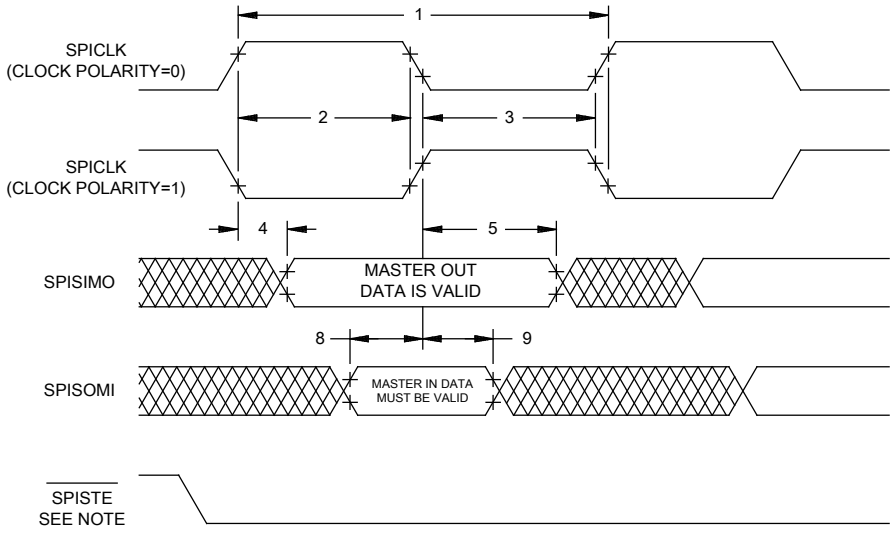
$\overline{ADCSOCAO}$ OR $\overline{ADCSOCBO}$ TIMING

FIGURE 18 Timing waveforms.



EXTERNAL INTERRUPT TIMING

FIGURE 19 Timing waveforms.

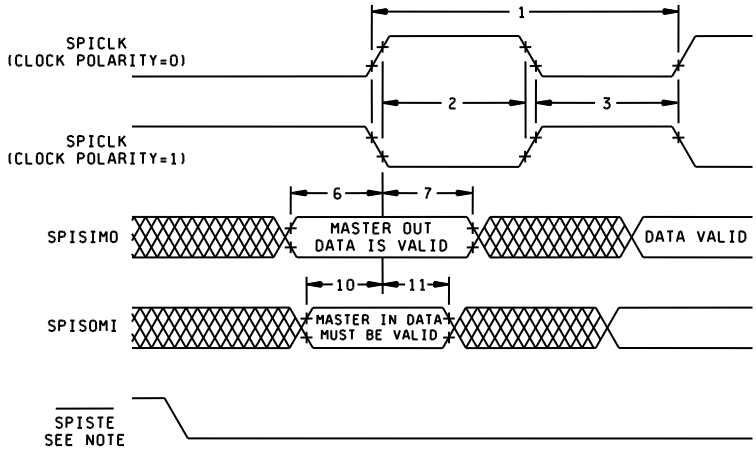


SPI MASTER MODE EXTERNAL TIMING(CLOCK PHASE=0)

Note:

1. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$(minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 20 Timing waveforms.

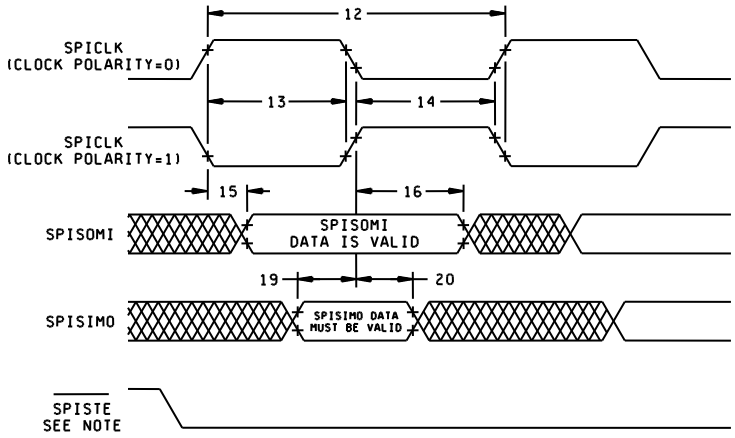


SPI MASTER EXTERNAL TIMING(CLOCK PHASE=1)

Note:

1. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$(minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 21 Timing waveforms.

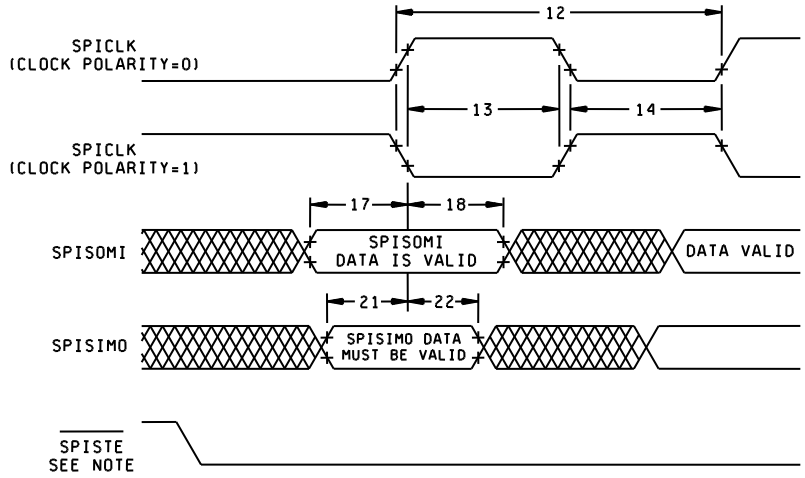


SPI SLAVE MODE EXTERNAL TIMING(CLOCK PHASE=0)

Note:

1. In the slave mode, $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$(minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 22. Timing waveforms.

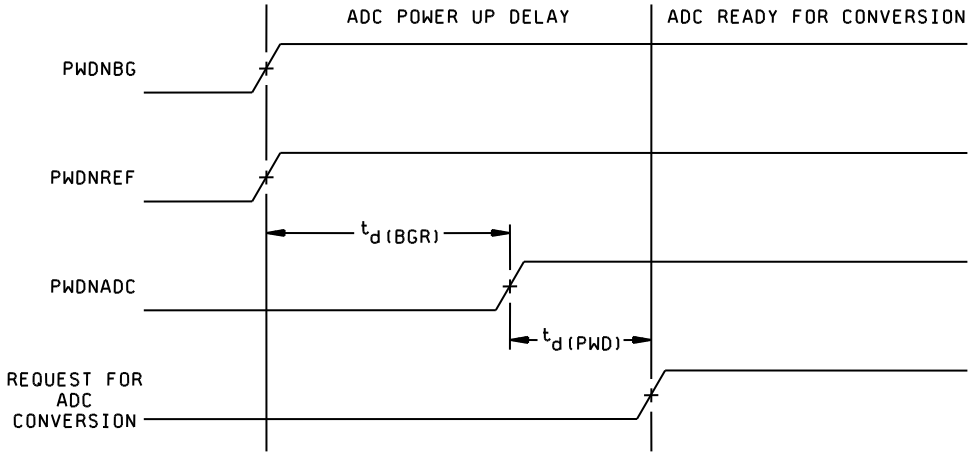


SPI SLAVE MODE EXTERNAL TIMING(CLOCK PHASE=1)

Note:

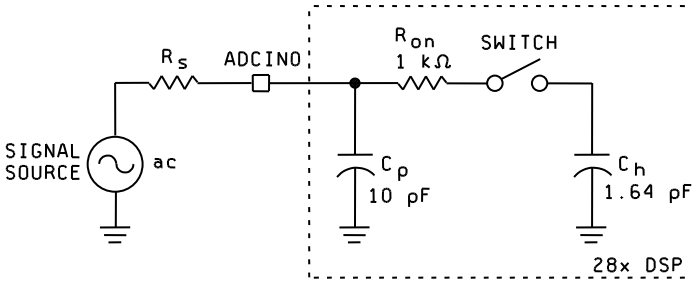
1. In the slave mode, $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$(minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 23. Timing waveforms.



ADC POWER-UP CONTROL BIT TIMING

FIGURE 24. Timing waveforms.

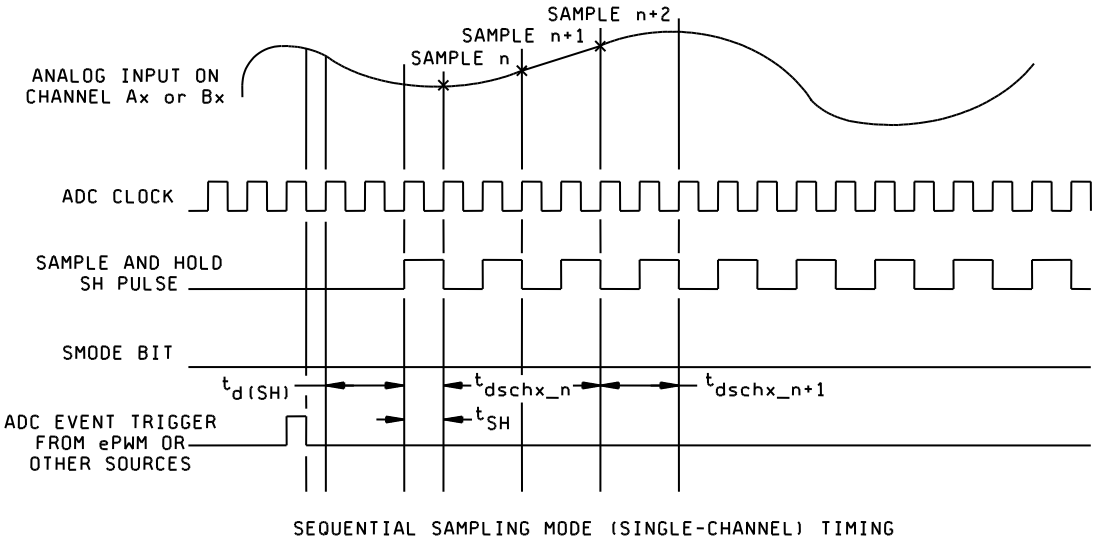


ADC ANALOG INPUT IMPEDANCE MODEL

Typical values of the circuit components:

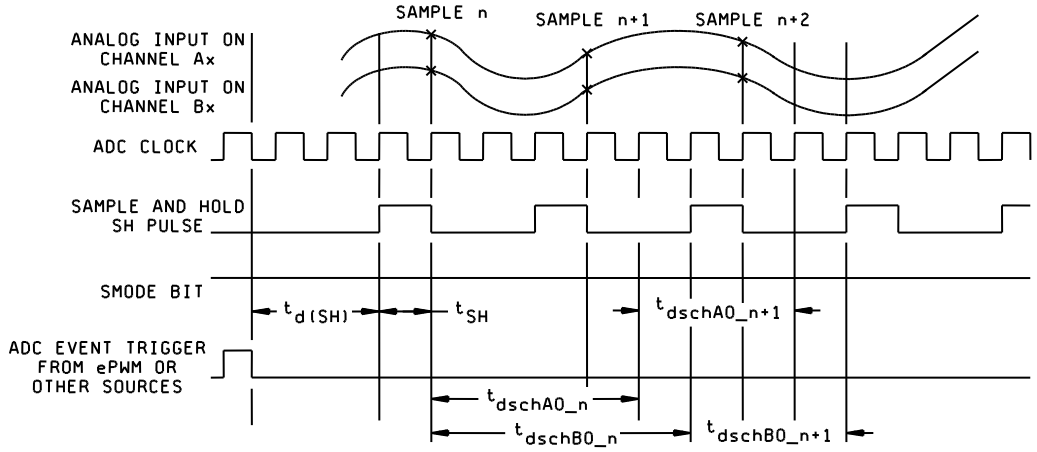
Switching resistance (R_{ON}) :	1 kΩ.
Sampling capacitor (C_h):	1.64 pF
Parasitic capacitance (C_p):	10 pF
Source resistance (R_s):	50 Ω

FIGURE 25. Timing waveforms.



SEQUENTIAL SAMPLING MODE (SINGLE-CHANNEL) TIMING

FIGURE 26. Timing waveforms.



SIMULTANEOUS SAMPLING MODE TIMING

FIGURE 27. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/06619-01XE	01295	SM320F2808PZMEP
V62/06619-02XE	2/	SM320F2806PZMEP
V62/06619-03XE	01295	SM320F2801PZMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243