REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. - ro	12-10-15	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A	A	A	A					
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-03-22	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, LINEAR, DUAL OUTPUT, LOW DROPOUT, VOLTAGE REGULATOR, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06617**
	REV **A**	**PAGE** 1 **OF** 13

AMSC N/A

5962-V008-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual output, low dropout, voltage regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS767D301-EP	Dual output, low dropout, voltage regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	28	MO-153	Plastic small outline with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range (V_I) ..... -0.3 V to 13.5 V 2/
Input voltage range (V_I) :
1IN, 2IN, $\overline{EN}$ pins ..... -0.3 V to V_I + 0.3 V
Output voltage (V_O) :
1OUT, 2OUT pins ..... 7 V
$\overline{RESET}$ pin ..... 16.5 V
Peak output current ..... Internally limited
Electrostatic discharge (ESD) rating:
Human body model (HBM) ..... 2 kV
Continuous total power dissipation (P_D) ..... See dissipation rating table
Operating virtual junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 3/

Input voltage range (V_I):
1IN, 2IN pins ..... 2.7 V to 10 V 4/
Output current for each LDO ..... 0 to 1 A 5/
Output voltage range (V_O) :
1OUT, 2OUT pins ..... 1.5 V to 5.5 V
Operating virtual junction temperature (T_J) ..... -55°C to +125°C

1.5 Dissipation rating table. 6/

Package	Air flow (CFM)	$T_A \leq 25°C$ power rating	Derating factor above $T_A = 25°C$	$T_A = 70°C$ power rating	$T_A = 85°C$ power rating
X	0	3.58 W	3.58°C/W	1.97 W	1.43 W
	250	5.07 W	5.07°C/W	2.79 W	2.03 W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to network ground terminal.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ To calculate the minimum input voltage for maximum output current, use the following equation:
$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
5/ Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this paragraph for extended periods of time.
6/ This parameter is measured with the recommended copper heat-sink pattern on a four layer printed circuit board (PCB), 1 ounce copper on 4 inch x 4 inch ground layer. For more information, refer to manufacturer technical brief literature number SLMA002.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Output voltage 3/ (adjustable)	V_O	1.5 V ≤ V_O ≤ 5.5 V, 10 μA < I_O < 1 A	-55°C to +125°C	01	0.97V_O	1.02V_O	V
Output voltage 3/ (3.3 V output)	V_O	4.3 V < V_I < 10 V, 10 μA < I_O < 1 A	-55°C to +125°C	01	3.201	3.366	V
Quiescent current 3/ (GND current) for each LDO		I_O = 1 A	-55°C to +125°C	01		125	μA
Output voltage 3/ 4/ line regulation for each LDO	ΔV_O / V_O	V_O + 1 V < V_I ≤ 10 V	+25°C	01	0.01 typical		%/V
Output noise voltage		BW = 200 Hz to 100 kHz, V_O = 1.8 V, I_C = 1 A, C_O = 10 μF	+25°C	01	55 typical		μV_{RMS}
Output current limit for each LDO		V_O = 0 V	-55°C to +125°C	01		2	A
Thermal shutdown junction temperature			+25°C	01	150 typical		°C
Standby current for each LDO		2.7 V < V_I < 10 V, $\overline{EN}$ = V_I	-55°C to +125°C	01		10	μA
FB input current (adjustable)		FB = 1.5	+25°C	01	2 typical		nA
High level enable input voltage			-55°C to +125°C	01	2		V
Low level enable input voltage			-55°C to +125°C	01		0.8	V
Power supply 3/ ripple rejection		f = 1 kHz, C_O = 10 μF	+25°C	01	60 typical		dB
Input current ($\overline{EN}$)		$\overline{EN}$ = 0 V	-55°C to +125°C	01	-1	1	μA
		$\overline{EN}$ = V_I			-1	1	
Load regulation			+25°C	01	3 typical		mV
Dropout voltage 5/		V_O = 3.3 V, I_O = 1 A	-55°C to +125°C	01		575	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Reset section							
Minimum input voltage for valid $\overline{\text{RESET}}$		$I_{O(RESET)}$ = 300 μA	+25°C	01	1.1 typical		V
Trip threshold voltage		V_O decreasing	-55°C to +125°C	01	92	98	%/V
Hysteresis voltage		Measured at V_O	+25°C	01	0.5 typical		%/V
Output low voltage		V_I = 2.7 V, $I_{O(RESET)}$ = 1 mA	-55°C to +125°C	01		0.4	V
Leakage current		$V_{(RESET)}$ = 7 V	-55°C to +125°C	01		1	μA
$\overline{\text{RESET}}$ time out delay			+25°C	01	200 typical		mV

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $V_I = V_{O(nominal)} + 1$ V, I_O = 1 mA, $\overline{EN}$ = 0, and C_O = 10 μF.

3/ The minimum IN operating voltage is 2.7 V or $V_{O(typical)} + 1$ V, whichever is greater. The maximum IN voltage is 10 V.

4/ If $V_O \leq 1.8$ V then $V_{I(min)}$ = 2.7 V, $V_{I(max)}$ = 10 V:

Line regulation (mV) = (% / V) x (V_O ($V_{I(max)}$ – 2.7 V) / 100) x 1000

If $V_O \geq 2.5$ V then $V_{I(min)}$ V_O + 1 V, and $V_{I(max)}$ = 10 V:

Line regulation (mV) = (% / V) x (V_O ($V_{I(max)}$ – (V_O + 1 V)) / 100) x 1000

5/ IN voltage equals $V_{O(typical)}$ – 100 mV: adjustable output voltage set to 3.3 V nominal with external resistor divider. Dropout voltage of 1.8 V and 2.5 V is limited by input voltage range limitations.

Case X

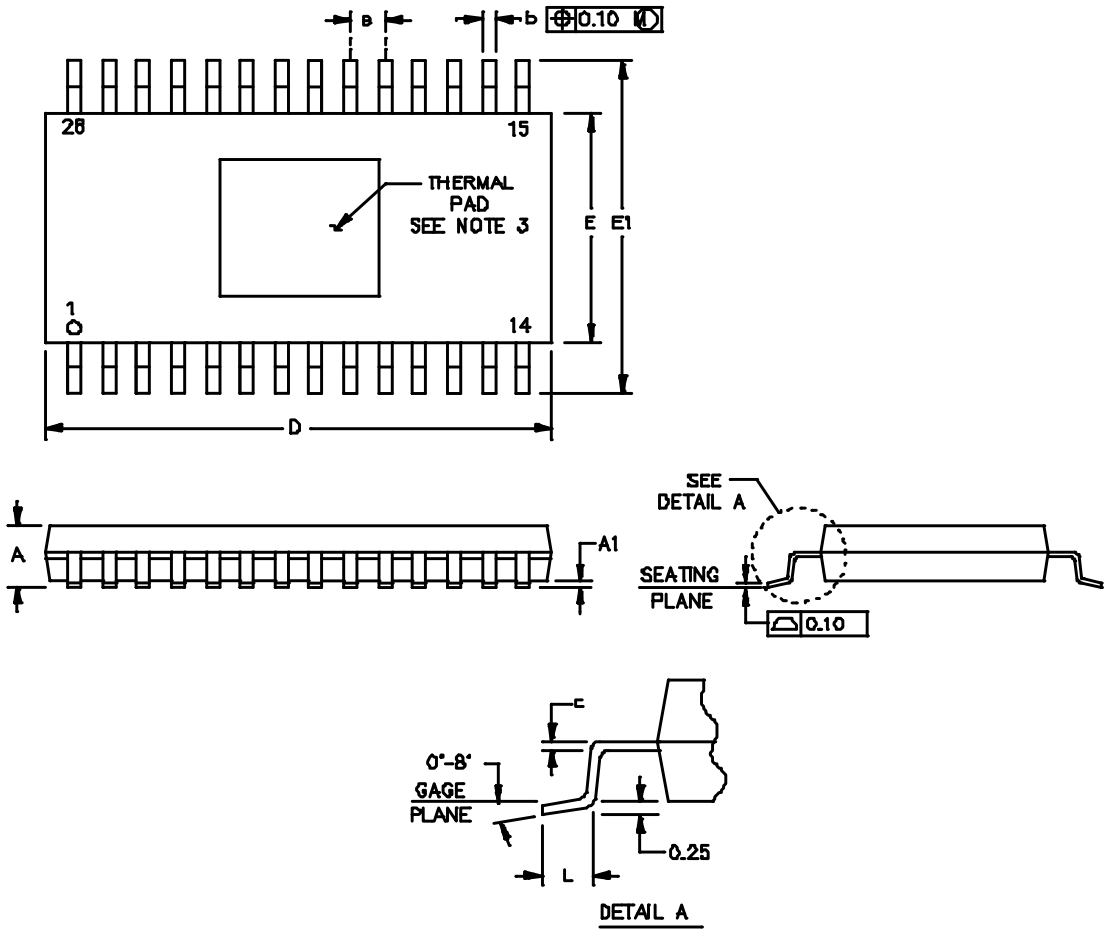


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.001	0.005	0.05	0.15
b	0.007	0.011	0.19	0.30
c	0.005 nominal		0.15 nominal	
D	0.377	0.385	9.60	9.80
e	0.025 BSC		0.65 BSC	
E	0.169	0.177	4.30	4.50
E1	0.244	0.259	6.20	6.60
L	0.019	0.029	0.50	0.75
n	28 leads		28 leads	

Notes:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per side.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer literature number SLMA002 for information regarding recommended board layout. This document is available from the manufacturer.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline – continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	NC
2	NC
3	1GND
4	$\overline{1EN}$
5	1IN
6	1IN
7	NC
8	NC
9	2GND
10	$\overline{2EN}$
11	2IN
12	2IN
13	NC
14	NC
15	NC
16	NC
17	2OUT
18	2OUT
19	NC
20	NC
21	NC
22	$\overline{2RESET}$
23	1OUT
24	1OUT
25	1FB/NC
26	NC
27	NC
28	$\overline{1RESET}$

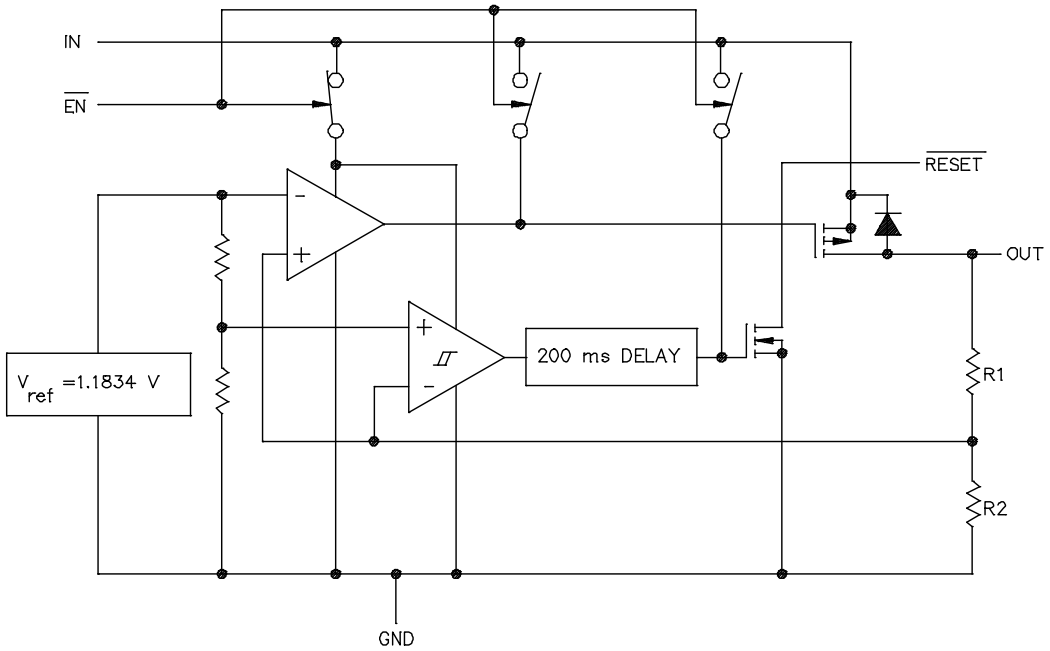
NC = No internal connection

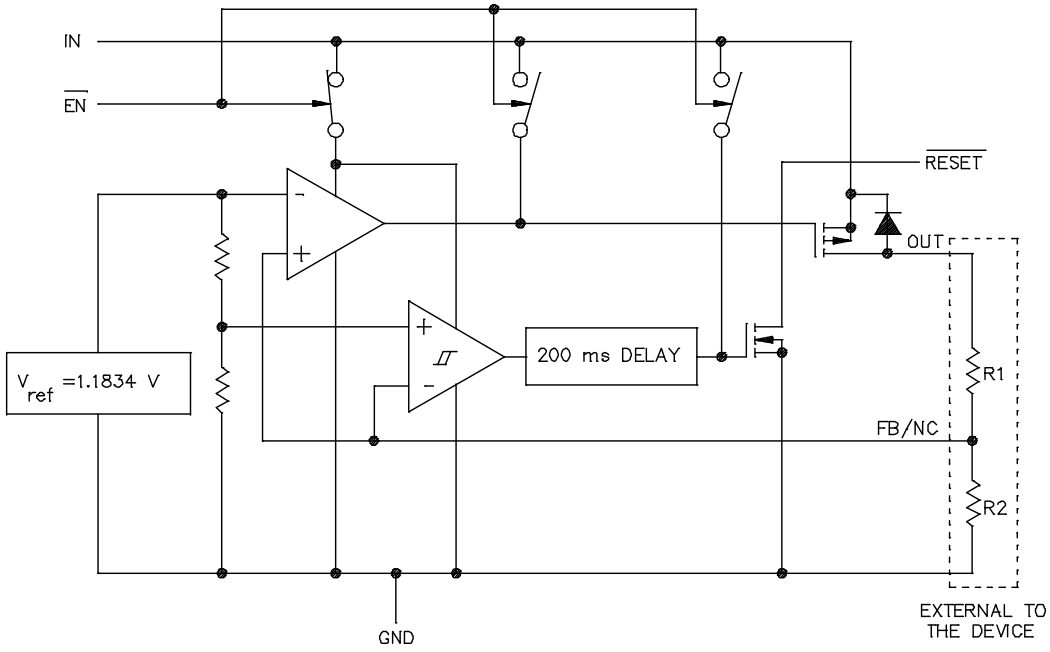
FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
1GND		Regulator 1 ground.
$\overline{1EN}$	I	Regulator 1 enable.
1IN	I	Regulator 1 input supply voltage.
2GND		Regulator 2 ground.
$\overline{2EN}$	I	Regulator 2 enable.
2IN	I	Regulator 2 input supply voltage.
2OUT	O	Regulator 2 output voltage.
$\overline{2RESET}$	O	Regulator 2 reset.
1OUT	O	Regulator 1 output voltage.
1FB/NC	I	Regulator 1 output voltage feedback for adjustable version and no connect for fixed output version.
$\overline{1RESET}$	O	Regulator 1 reset.
NC		No connection.

FIGURE 2. Terminal connections – Continued.

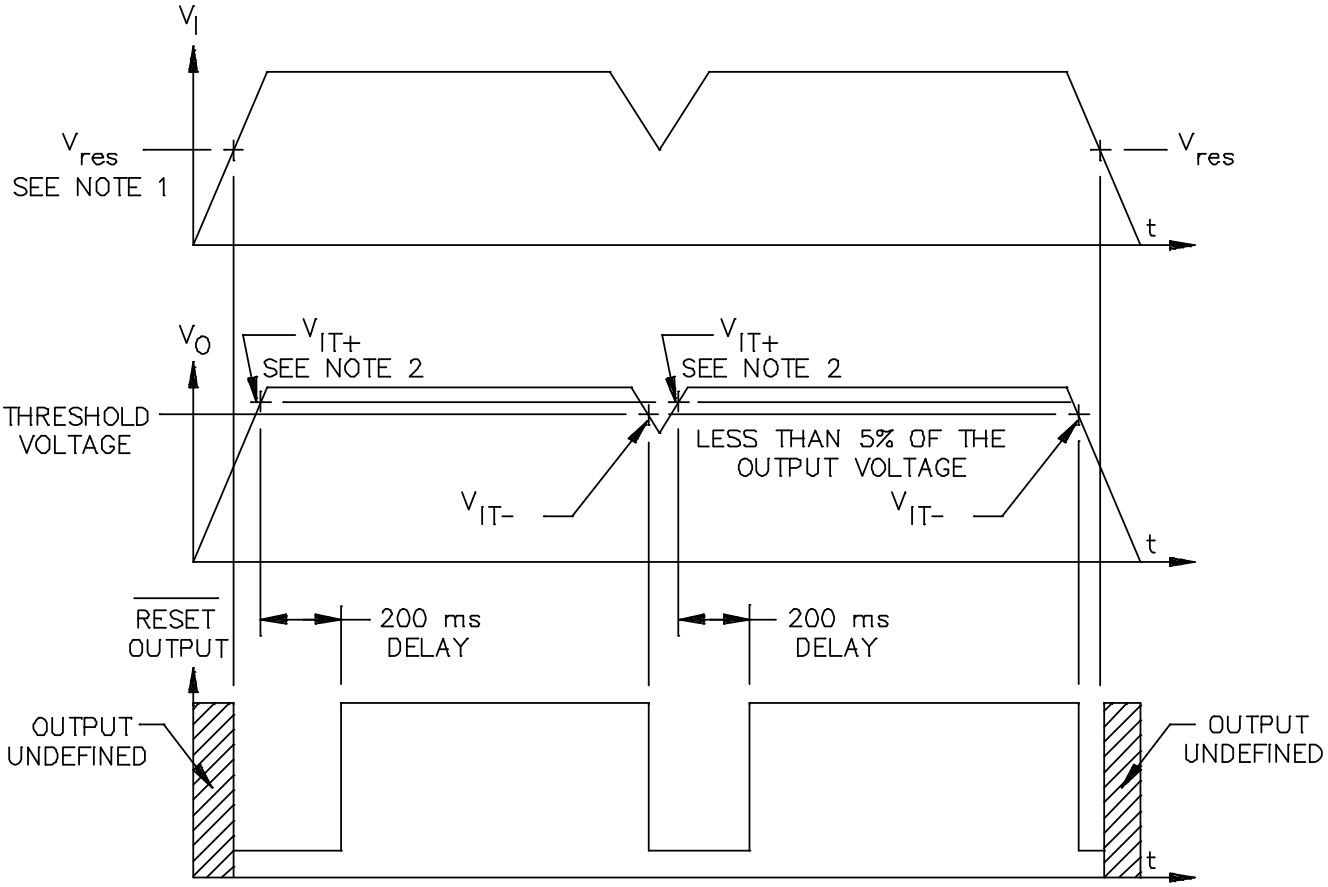
Adjustable version (for each LDO)





Fixed voltage version (for each LDO)

FIGURE 3. Block diagram.



NOTES:

1. V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.
2. V_{IT} - Trip voltage is typically 5% lower than the output voltage (95% V_O).

FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Regulator 1 V_O (V)	Regulator 2 V_O (V)	Vendor part number
V62/06617-01XE	01295	Adjustable (1.5 V to 5.5 V)	3.3 V	TPS767D301MPWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493