REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add footnotes 3/ and 4/ to output voltage (reference voltage) test under Table I. Update boilerplate paragraphs to current requirements. - ro	12-08-14	C. SAFFLE
B	Update boilerplate paragraphs to current requirements. - ro	18-04-04	C. SAFFLE
C	Add typical limits to tested parameters as specified under Table I. Update document paragraphs to current requirements. - ro	25-03-04	L. LEEPER BRANHAM

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C							
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							

PMIC N/A

Original date of drawing

06-03-15

PREPARED BY
RICK OFFICER

CHECKED BY
TOM HESS

APPROVED BY
RAYMOND MONNIN

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE

MICROCIRCUIT, LINEAR, DUAL OUTPUT, LOW DROPOUT VOLTAGE REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/06616
REV C		PAGE 1 OF 15

AMSC N/A

5962-V131-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual output, low dropout voltage regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	TPS70345-EP	Dual output, low dropout voltage regulator

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	MO-153	Plastic small outline with a thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range:
(V_{IN1}) ..... -0.3 V to +7 V 2/
(V_{IN2}) ..... -0.3 V to +7 V 2/
Voltage range at $\overline{EN}$ ..... -0.3 V to +7 V
Output voltage range (V_{OUT1}, V_{SENSE1}) ..... +5.5 V
Output voltage range (V_{OUT2}, V_{SENSE2}) ..... +5.5 V
Maximum $\overline{RESET}$, PG1 voltage ..... +7 V
Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage ..... V_{IN1}
Peak output current ..... Internally limited
Operating virtual junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (ESD) rating:
Human body model (HBM) ..... 2 kV

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are tied to network ground.

1.4 Recommended operating conditions. 3/

Input voltage range (V_{IN})	+2.7 V to +6.0 V 4/
Output current (I_O) (regulator 1)	0 to 1.0 A
Output current (I_O) (regulator 2)	0 to 2.0 A
Operating virtual junction temperature range (T_J)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Output voltage 3/ 4/ (reference voltage)	V_O	2.7 V < V_I < 6 V, FB connected to V_O	-55°C to +125°C	01	1.196	1.248	V
		2.7 V < V_I < 6 V, FB connected to V_O	25°C		1.224 typical		
Output voltage 1.2 V output (V_{OUT2})	V_O	2.7 V < V_I < 6 V	-55°C to +125°C	01	1.176	1.224	V
		2.7 V < V_I < 6 V	25°C		1.2 typical		
Quiescent current 3/ (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0 V		4/	-55°C to +125°C	01		250	µA
			25°C		185 typical		
Output voltage line regulation 5/ (ΔV_O / V_O) for regulator 1 and regulator 2		V_O + 1 V < V_I < 6 V 3/	-55°C to +125°C	01		0.1 %	V
		V_O + 1 V < V_I < 6 V 3/	25°C		0.01 % typical		
Load regulation for V_{OUT1} and V_{OUT2}		4/	25°C	01	1 typical		mV
Output current limit		Regulator 1, V_O = 0 V	-55°C to +125°C	01		2.35	A
			25°C		1.75 typical		
		Regulator 2, V_O = 0 V	-55°C to +125°C			4.8	
			25°C		3.8 typical		
Thermal shutdown junction temperature			25°C	01	150 typical		°C
Standby current	$I_{I(standby)}$	$\overline{EN}$ = V_I	25°C	01		2	µA
					1 typical		
		$\overline{EN}$ = V_I	-55°C to +125°C			10	
RESET TERMINAL							
Minimum input voltage for valid $\overline{RESET}$		$I_{(RESET)}$ = 300 µA, $V_{(RESET)}$ ≤ 0.8 V	-55°C to +125°C	01		1.3	V
			25°C		1 typical		
Trip threshold voltage		V_O decreasing	-55°C to +125°C	01	92%	98%	V_O
			25°C		95% typical		
Hysteresis voltage		Measured at V_O	+25°C	01	0.5% typical		V_O

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
RESET TERMINAL – CONTINUED.							
$t_{(RESET)}$		$\overline{RESET}$ pulse duration	-55°C to +125°C	01	80	160	ms
			25°C		120 typical		
$t_{r(RESET)}$		Rising edge deglitch	+25°C	01	30 typical		µs
Output low voltage		V_I = 3.5 V, $I_{(RESET)}$ = 1 mA	-55°C to +125°C	01		0.4	V
			25°C		0.15 typical		
Leakage current		$V_{(RESET)}$ = 6 V	-55°C to +125°C	01		1	µA
PG TERMINAL.							
Minimum input voltage for valid PG		$I_{(PG)}$ = 300 µA, $V_{(PG1)} \leq$ 0.8 V	-55°C to +125°C	01		1.3	V
			25°C		1.0 typical		
Trip threshold voltage		V_O decreasing	-55°C to +125°C	01	92%	98%	V_O
			25°C		95% typical		
Hysteresis voltage		Measured at V_O	+25°C	01	0.5% typical		V_O
$t_{r(PG1)}$		Rising edge deglitch	+25°C	01	30 typical		µs
Output low voltage		V_I = 2.7 V, $I_{(PG)}$ = 1 mA	-55°C to +125°C	01		0.4	V
			25°C		0.15 typical		
Leakage current		$V_{(PG1)}$ = 6 V	-55°C to +125°C	01		1	µA
EN TERMINAL.							
High level $\overline{EN}$ input voltage			-55°C to +125°C	01	2		V
Low level $\overline{EN}$ input voltage			-55°C to +125°C	01		0.7	V
Input current ($\overline{EN}$)			-55°C to +125°C	01	-1	1	µA
SEQ TERMINAL.							
High level SEQ input voltage			-55°C to +125°C	01	2		V
Low level SEQ input voltage			-55°C to +125°C	01		0.7	V
SEQ pullup current source			+25°C	01	6 typical		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
MR1 / MR2 TERMINALS.							
High level input voltage			-55°C to +125°C	01	2		V
Low level input voltage			-55°C to +125°C	01		0.7	V
Pullup current source			+25°C	01	9.5 typical		µA
V_{OUT2} TERMINAL.							
V_{OUT2} UV comparator positive going input threshold voltage of V_{OUT1} UV comparator			-55°C to +125°C	01	80% V_O	86% V_O	V
			25°C		83% V_O typical		
V_{OUT2} UV comparator hysteresis			+25°C	01	3% V_O typical		mV
V_{OUT2} UV comparator falling edge deglitch		V_{SENSE2} decreasing below threshold	+25°C	01	140 typical		µs
Peak output current		2 ms pulse width	+25°C	01	3 typical		A
Discharge transistor current		V_{OUT2} = 1.5 V	+25°C	01	7.5 typical		mA
V_{OUT1} TERMINAL.							
V_{OUT1} UV comparator positive going input threshold voltage of V_{OUT1} UV comparator			-55°C to +125°C	01	80% V_O	86% V_O	V
			25°C		83% V_O typical		
V_{OUT1} UV comparator hysteresis			+25°C	01	3% V_O typical		mV
V_{OUT1} UV comparator falling edge deglitch		V_{SENSE1} decreasing below threshold	+25°C	01	140 typical		µs
Dropout voltage 6/		I_O = 1 A, V_{IN1} = 3.2 V	-55°C to +125°C	01		255	mV
		I_O = 1 A, V_{IN1} = 3.2 V	+25°C		160 typical		
Peak output current		2 ms pulse width	+25°C	01	1.2 typical		A
Discharge transistor current		V_{OUT1} = 1.5 V	+25°C	01	7.5 typical		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
V_{IN1} / V_{IN2} TERMINAL.							
UVLO threshold			-55°C to +125°C	01	2.3	2.65	V
UVLO hysteresis			+25°C	01	110 typical		mV

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1 V, I_{OUTX} = 1 mA, $\overline{EN}$ = 0, C_{OUT1} = 22 μF, and C_{OUT2} = 47 μF.

3/ Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 6 V, minimum output current is 1 mA.

4/ I_O = 1 mA to 1 A for regulator 1 and 1 mA to 2 A regulator 2.

5/ If V_O < 1.8 V then V_{Imax} = 6 V, V_{Imin} = 2.7 V:

Line regulation (mV) = (% / V) x (V_O (V_{Imax} – 2.7 V) / 100) x 1000

If V_O > 2.5 V then V_{Imax} = 6 V, V_{Imin} = V_O + 1 V:

Line regulation (mV) = (% / V) x (V_O (V_{Imax} – (V_O + 1 V)) / 100) x 1000

6/ Input voltage (V_{IN1} or V_{IN2}) = $V_{O(typ)}$ – 100 mV. For the 1.5 V, 1.8 V, and 2.5 V regulators, the dropout voltage is limited by input voltage range. The 3.3 V regulator input voltage is set to 3.2 V to perform this test.

Case X

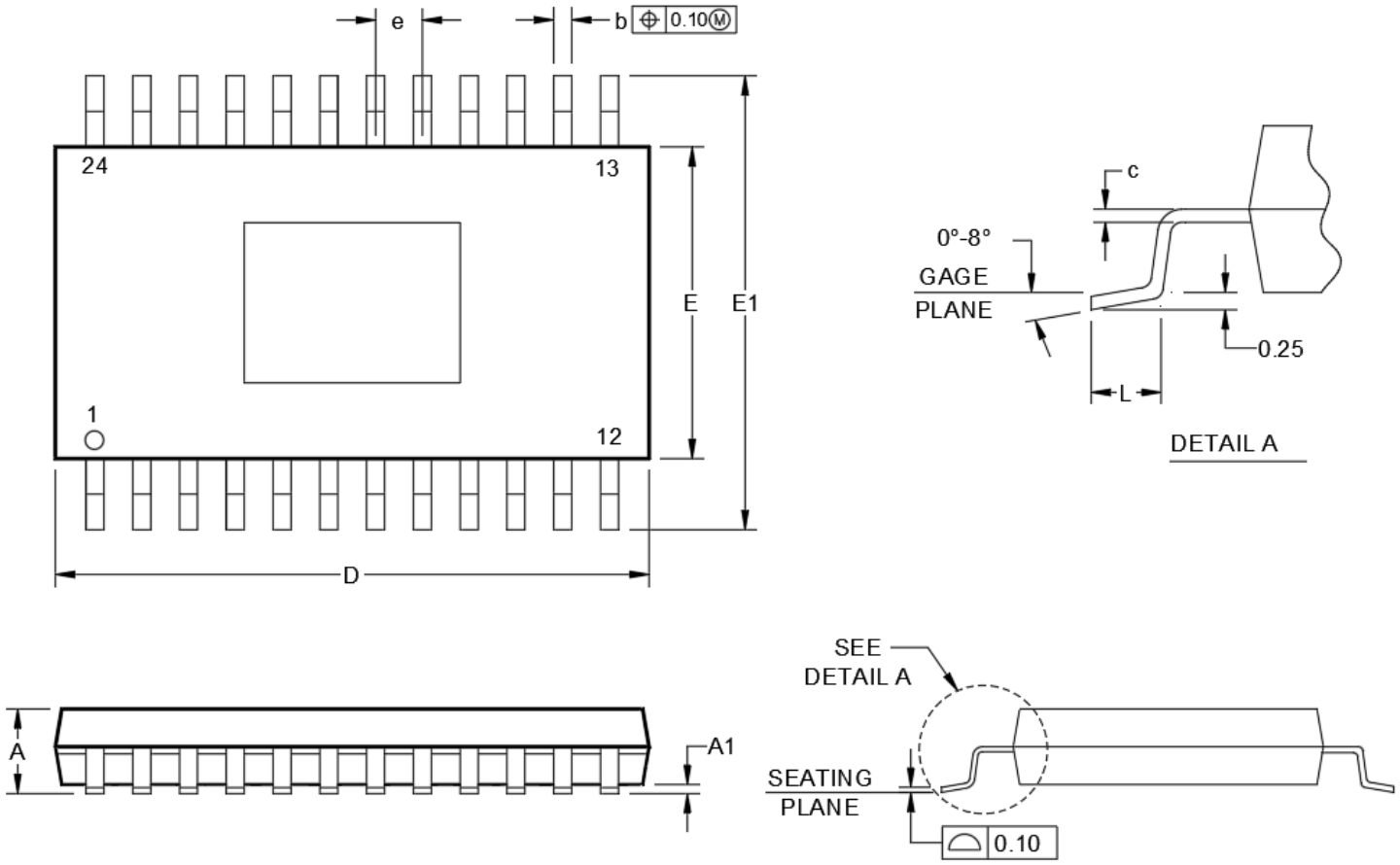


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/06616
		REV C	PAGE 8

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	---	1.20	---	.047
A1	0.05	0.15	.001	.005
b	0.19	0.30	.007	.011
c	0.15 nominal		.005 nominal	
D	7.70	7.90	.303	.311
E	4.30	4.50	.169	.177
E1	6.20	6.60	.244	.259
e	0.65 BSC		.025 BSC	
L	0.50	0.75	.019	.029
n	24		24	

Notes:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per side.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer literature number SLMA002 for information regarding recommended board layout. This document is available from the manufacturer.
4. Falls within JEDEC MO-153.

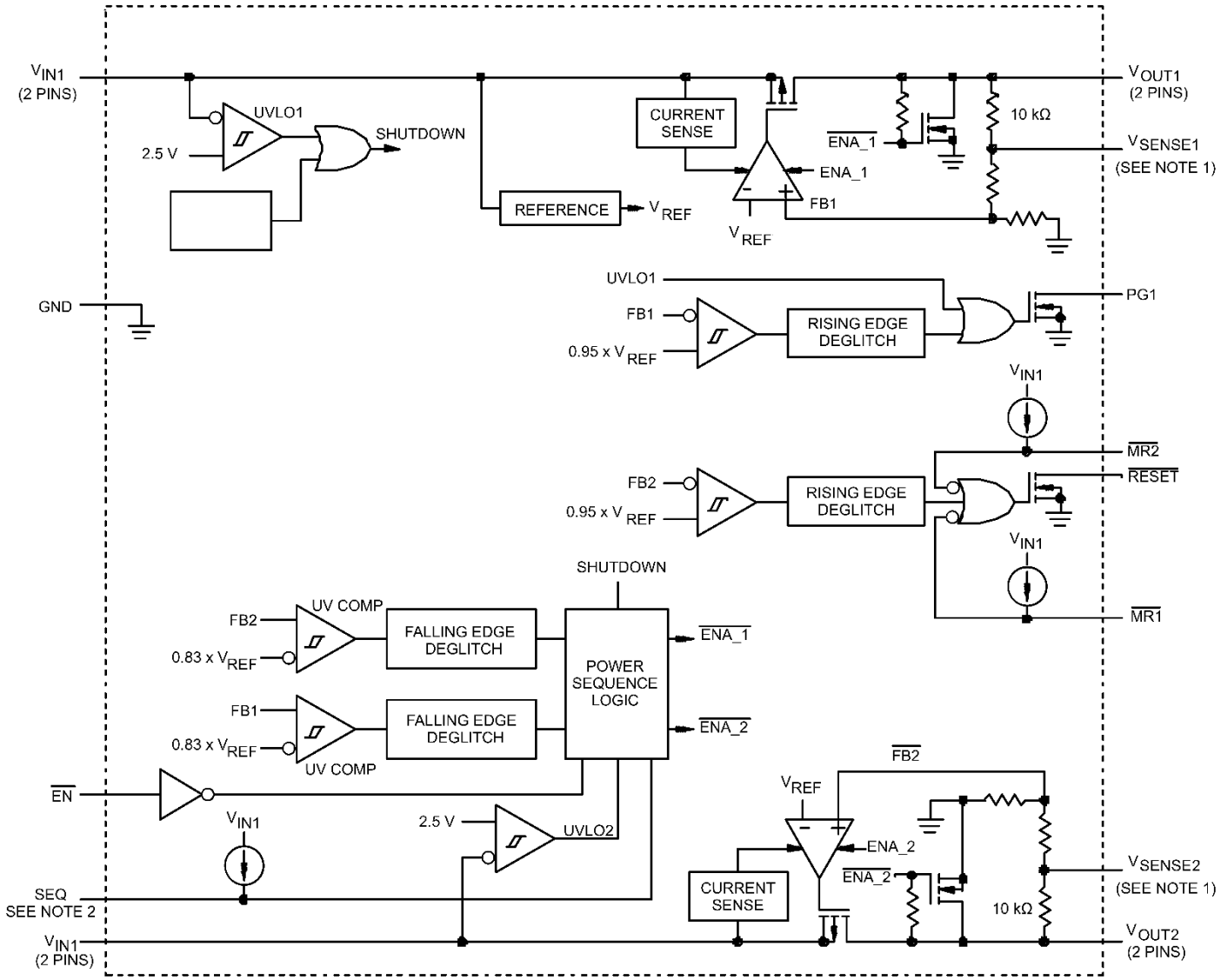
FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	GND / HEATSINK
2	V_{IN1}
3	V_{IN1}
4	NC
5	$\overline{MR2}$
6	$\overline{MR1}$
7	$\overline{EN}$
8	SEQ
9	GND
10	V_{IN2}
11	V_{IN2}
12	GND / HEATSINK
13	GND / HEATSINK
14	V_{OUT2}
15	V_{OUT2}
16	V_{SENSE2} / FB2
17	NC
18	$\overline{RESET}$
19	PG1
20	NC
21	V_{SENSE1} / FB1
22	V_{OUT1}
23	V_{OUT1}
24	GND / HEATSINK

FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
EN	I	Active low enable.
GND		Regulator ground.
GND / HEATSINK		Ground / heatsink.
MR1	I	Manual reset input 1, active low, pulled up internally.
MR2	I	Manual reset input 2, active low, pulled up internally.
NC		No connection.
PG1	O	Open drain output, low when V_{OUT1} voltage is less than 95 % of the nominal regulated voltage.
RESET	O	Open drain output, SVS (power on reset) signal, active low.
SEQ	I	Power up sequence control: SEQ = high, V_{OUT2} powers up first; SEQ = low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	I	Input voltage of regulator 1.
V_{IN2}	I	Input voltage of regulator 2.
V_{OUT1}	O	Output voltage of regulator 1.
V_{OUT2}	O	Output voltage of regulator 2.
V_{SENSE2}	I	Regulator 2 output voltage sense.
V_{SENSE1}	I	Regulator 1 output voltage sense.

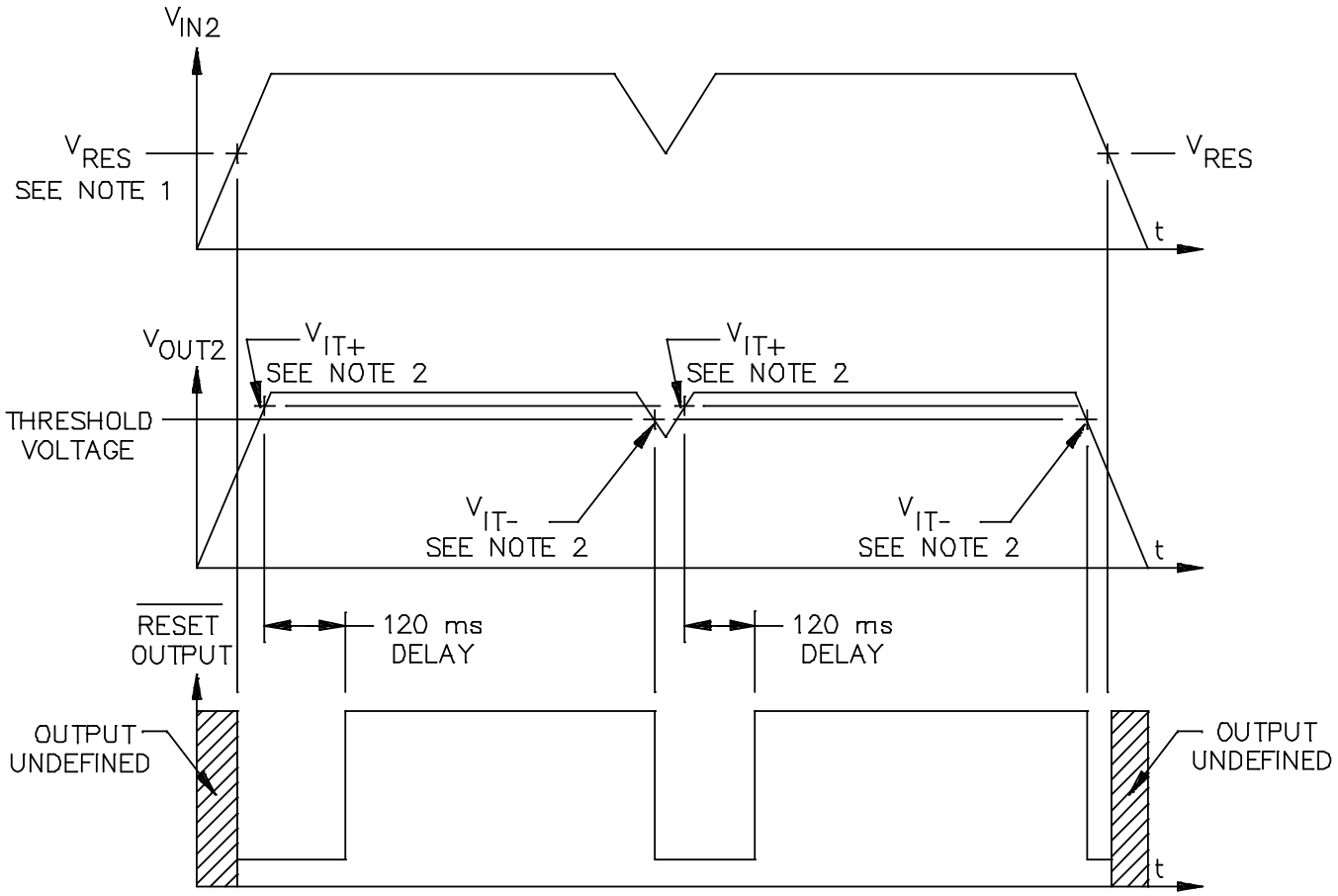
FIGURE 2. Terminal connections – Continued.



NOTES:

1. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the application information section.
2. If the SEQ terminal is floating at the input, V_{OUT2} powers up first.

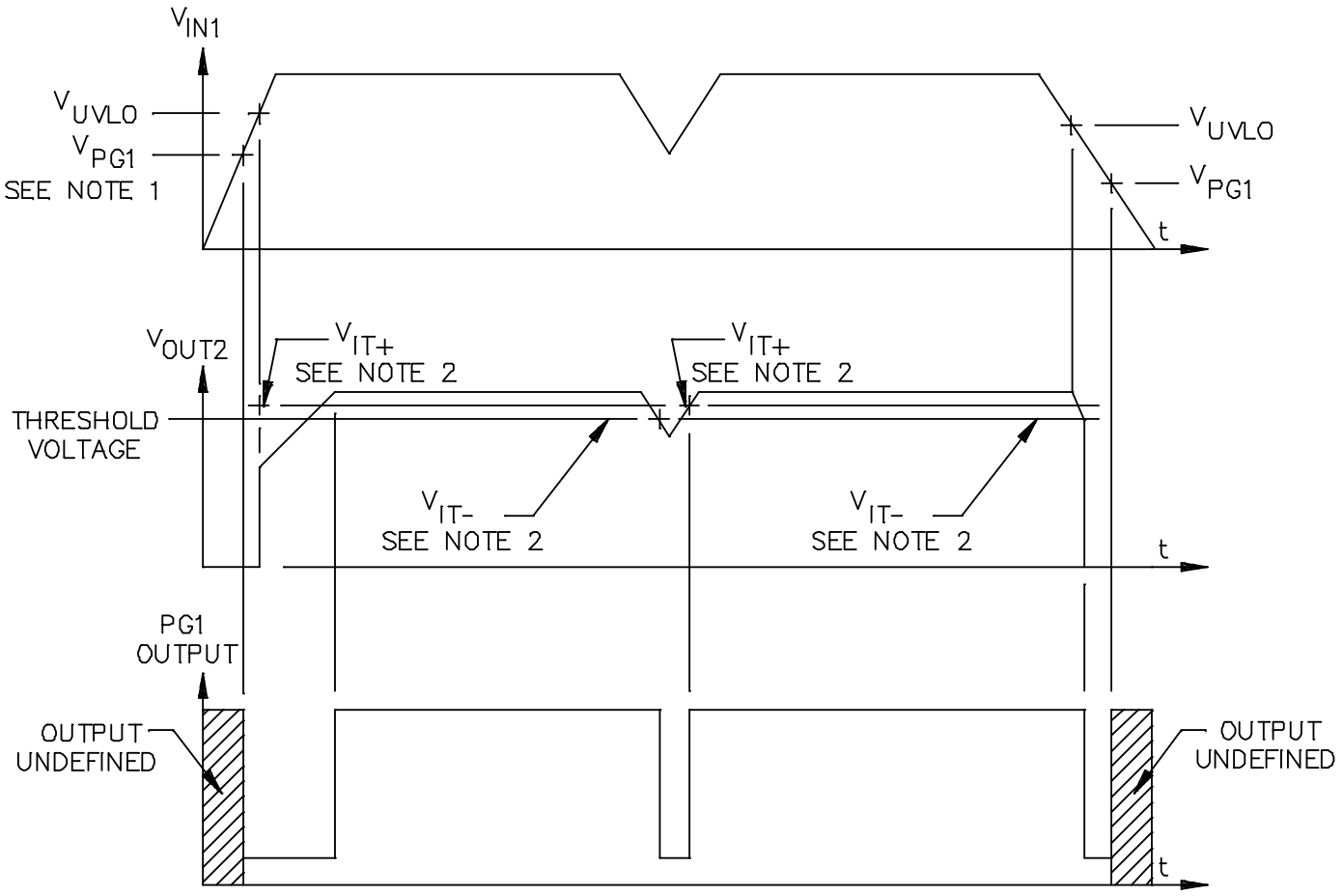
FIGURE 3. Logic diagram.



NOTES:

1. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.
2. V_{IT-} Trip voltage is typically 5% lower than the output voltage (95% V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

FIGURE 4. Timing waveforms.



Notes:

1. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.
2. V_{IT-} Trip voltage is typically 5% lower than the output voltage (95% V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

FIGURE 4. Timing waveforms – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Regulator 1 V_O (V)	Regulator 2 V_O (V)	Vendor part number
V62/06616-01XE	01295	3.3 V	1.2 V	TPS70345MPWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated 12500 TI Blvd. Dallas, TX 75243