REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add a note to figure 1. Add JEDEC references to paragraph 2. Update document paragraphs to current requirements. - ro	14-08-20	C. SAFFLE
B	Under figure 1, delete the last sentence of Note 3, make change to the dimension “c” minimum limit, and make correction to dimension “E” millimeter limits. Update document paragraphs to current requirements. - ro	20-04-02	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B																		
PAGE	18	19	20																		

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-02-21	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, EXTENDED COMMON MODE VOLTAGE, RS-485 TRANSCEIVER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06615**
	REV **B**	**PAGE** 1 **OF** 20

AMSC N/A

5962-V028-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance extended common mode voltage, RS-485 transceiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65HVD21-EP	Extended common mode voltage, RS-485 transceiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7 V 2/
Voltage at any bus I/O terminal ..... -27 V to 27 V
Voltage input, transient pulse, A and B, (through 100 Ω, see figure 20) ..... -60 V to 60 V
Voltage input at any D, DE or $\overline{RE}$ terminal ..... -0.5 V to V_{CC} + 0.5 V
Receiver output current, (I_O) ..... -10 mA to 10 mA
Electrostatic discharge:
  Human body model: 3/
    A, B, GND ..... 16 kV
    All pins ..... 5 kV
  Charged device model: (all pins) ..... 1.5 kV 4/
  Machine model: (all pins) ..... 200 V 5/
Continuous total power dissipation (P_D) ..... See power dissipation rating table
Junction temperature range (T_J) ..... +150°C

1.4 Recommended operating conditions. 6/

Supply voltage (V_{CC}) ..... 4.5 V to 5.5 V
Voltage at any bus I/O terminal (A, B) ..... -20 V to 25 V
High level input voltage, (V_{IH}) (D, DE, $\overline{RE}$) ..... 2 V to V_{CC}
Low level input voltage, (V_{IL}) (D, DE, $\overline{RE}$) ..... 0 V to 0.8 V
Differential input voltage, (V_{ID}) (A with respect to B) ..... -25 V to 25 V
Output current (Driver) ..... -110 mA to 110 mA
Output current (Receiver) ..... -8 mA to 8 mA
Junction temperature (T_J) ..... -55°C to +130°C
Operating free-air temperature range (T_A) ..... -55°C to +125°C 7/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC Standard 22, test method A114-A.
4/ Tested in accordance with JEDEC Standard 22, test method C101.
5/ Tested in accordance with JEDEC Standard 22, test method A115-A.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ Maximum free air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

1.5 Power dissipation ratings table.

Package	Circuit board model	$T_A \leq 25°C$ power rating	Derating 10/ factor above $T_A = 25°C$	$T_A = 70°C$ power rating	$T_A = 85°C$ power rating
X	Low – K 8/	577 mW	4.62 mW/°C	369 mW	300 mW
	High – K 9/	913 mW	7.3 mW/°C	584 mW	474 mW

1.6 Thermal characteristics.

Junction-to-board thermal resistance (θ_{JB}) ..... 86.2°C/W
Junction-to-case thermal resistance (θ_{JC}) ..... 47.1°C/W
Device power dissipation (P_D):
Typical operation:
Test conditions: V_{CC} = 5 V, T_J = 25°C, R_L = 54 Ω, C_L = 50 pF (driver),
C_L = 15 pF (receiver), 50 % duty cycle square wave signal,
driver and receiver enabled, 5 Mbps ..... 260 mW
Worst case operation:
Test conditions: V_{CC} = 5.5 V, T_J = 125°C, R_L = 54 Ω, C_L = 50 pF,
C_L = 15 pF (receiver), 50 % duty cycle square wave signal,
driver and receiver enabled, 5 Mbps ..... 342 mW
Thermal shut down junction temperature (T_{SD}) ..... +170°C

_____

8/ In accordance with the Low-K thermal metric definitions of EIA / JESD51-3.
High K specifies a high thermal conductivity printed circuit board used to measure theta parameters.
9/ In accordance with the High-K thermal metric definitions of EIA / JESD51-7.
Low K specifies a low thermal conductivity printed circuit board used to measure theta parameters.
10/ This is the inverse of the junction to ambient thermal resistance when board mounted and with no air flow.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JEDEC 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	–	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
JESD22-A115	–	Electrostatic Discharge Sensitivity Testing Machine Model (MM)

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth tables. The truth tables shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section.							
Input clamp voltage	V_{IK}	I_I = -18 mA	-55°C to +125°C	01	-1.5		V
Open circuit output voltage	V_O	A or B, no load	-55°C to +125°C	01	0	V_{CC}	V
Steady state differential output voltage magnitude	$\|V_{OD(SS)}\|$	No load (open circuit)	-55°C to +125°C	01	3.3	V_{CC}	V
		R_L = 54 Ω, see figure 5			1.8		
		With common mode loading, see figure 6			1.8		
Change in steady state differential output voltage between logic states	$\Delta\|V_{OD(SS)}\|$	See figure 5 and figure 7	-55°C to +125°C	01	-0.1	0.1	V
Steady state common mode output voltage	$V_{OC(SS)}$	See figure 5	-55°C to +125°C	01	2.1	2.9	V
Change in steady state common mode output voltage, $V_{OC(H)} - V_{OC(L)}$	$\Delta V_{OC(SS)}$	See figure 5 and figure 8	-55°C to +125°C	01	-0.1	0.1	V
Peak to peak common mode output voltage, $V_{OC(MAX)} - V_{OC(MIN)}$	$V_{OC(PP)}$	R_L = 54 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 5 and figure 8	+25°C	01	0.35 typical		V
Differential output voltage over and under shoot	$V_{OD(RING)}$	R_L = 54 Ω, C_L = 50 pF, see figure 9	-55°C to +125°C	01		10%	
Input current	I_I	D, DE	-55°C to +125°C	01	-100	100	µA
Output current with power off	$I_{O(OFF)}$	$V_{CC} \leq$ 2.5 V	-55°C to +125°C	01	-100	125	µA
High impedance state output current	I_{OZ}	DE at 0 V	-55°C to +125°C	01	-100	125	µA
Short circuit output current	I_{OS}	V_O = -7 V to 12 V, see figure 13	-55°C to +125°C	01	-270	250	mA
Differential output capacitance	C_{OD}		-55°C to +125°C	01	See receiver C_I		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section.							
Differential output propagation delay, high to low	t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see figure 7	-55°C to +125°C	01	15	60	ns
Differential output rise time	t_r	R_L = 54 Ω, C_L = 50 pF, see figure 7	-55°C to +125°C	01	15	60	ns
Differential output fall time	t_f	R_L = 54 Ω, C_L = 50 pF, see figure 7	-55°C to +125°C	01	15	60	ns
Propagation delay time, high impedance to high level output	t_{PZH}	$\overline{RE}$ at 0 V, see figure 10	-55°C to +125°C	01		140	ns
Propagation delay time, high level output to high impedance	t_{PHZ}	$\overline{RE}$ at 0 V, see figure 10	-55°C to +125°C	01		140	ns
Propagation delay time, high impedance to low level output	t_{PZL}	$\overline{RE}$ at 0 V, see figure 11	-55°C to +125°C	01		140	ns
Propagation delay time, low level output to high impedance	t_{PLZ}	$\overline{RE}$ at 0 V, see figure 11	-55°C to +125°C	01		140	ns
Time from an active differential output to standby	$t_{d(standby)}$	$\overline{RE}$ at 0 V_{CC}, see figure 12	-55°C to +125°C	01		4	µs
Wake up time from standby to an active differential output	$t_{d(wake)}$	$\overline{RE}$ at 0 V_{CC}, see figure 12	-55°C to +125°C	01		10	µs
Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$	$t_{sk(p)}$		-55°C to +125°C	01		10	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section.							
Positive going differential input voltage threshold	$V_{IT(+)}$	V_O = 2.4 V, I_O = -8 mA, see figure 14	-55°C to +125°C	01		200	mV
Negative going differential input voltage threshold	$V_{IT(-)}$	V_O = 0.4 V, I_O = 8 mA, see figure 14	-55°C to +125°C	01	-200		mV
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{HYS}		-55°C to +125°C	01	100		mV
Positive going differential input failsafe voltage threshold	$V_{IT(F+)}$	V_{CM} = -7 V to 12 V, see figure 19	-55°C to +125°C	01	40	200	mV
		V_{CM} = -20 V to 25 V, see figure 19				250	
Negative going differential input failsafe voltage threshold	$V_{IT(F-)}$	V_{CM} = -7 V to 12 V, see figure 19	-55°C to +125°C	01	-200	-40	mV
		V_{CM} = -20 V to 25 V, see figure 19			-250		
Input clamp voltage	V_{IK}	I_I = -18 mA	-55°C to +125°C	01	-1.5		V
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -8 mA, see figure 15	-55°C to +125°C	01	4		V
Low level output voltage	V_{OL}	V_{ID} = -200 mV, I_{OL} = 8 mA, see figure 15	-55°C to +125°C	01		0.4	V
Bus input current (power on or power off)	$I_{I(BUS)}$	V_I = -7 V to 12 V, other input = 0 V	-55°C to +125°C	01	-100	125	µA
Input current	I_I	$\overline{RE}$	-55°C to +125°C	01	-100	125	µA
Input resistance	R_I		-55°C to +125°C	01	96		kΩ
Differential input capacitance	C_{ID}	V_{ID} = 0.5 + 0.4 sine (2π x 1.5 x 10^6t)	-55°C to +125°C	01		20	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver switching characteristics section.							
Propagation delay time high to low level output	t_{PHL}	See figure 15	-55°C to +125°C	01		70	ns
Receiver output rise time	t_r	See figure 15	-55°C to +125°C	01		7	ns
Receiver output fall time	t_f	See figure 15	-55°C to +125°C	01		7	ns
Receiver output enable time to high level	t_{PZH}	See figure 16	-55°C to +125°C	01		145	ns
Receiver output disable time from high level	t_{PHZ}	See figure 16	-55°C to +125°C	01		45	ns
Receiver output enable time to low level	t_{PZL}	See figure 17	-55°C to +125°C	01		145	ns
Receiver output disable time from low level	t_{PLZ}	See figure 17	-55°C to +125°C	01		45	ns
Time from an active receiver output to standby	$t_{r(STANDBY)}$	See figure 18, DE at 0 V	-55°C to +125°C	01		4	µs
Wake up time from standby to an active receiver output	$t_{r(WAKE)}$	See figure 18, DE at 0 V	-55°C to +125°C	01		11	µs
Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$	$t_{sk(p)}$		-55°C to +125°C	01		7	ns
Delay time, bus fail to failsafe set	$t_{p(set)}$	See figure 19, pulse rate = 1 kHz	-55°C to +125°C	01		385	µs
Delay time, bus recovery to failsafe reset	$t_{p(reset)}$	See figure 19, pulse rate = 1 kHz	-55°C to +125°C	01		70	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current section.							
Supply current	I_{CC}	Driver enabled (DE at V_{CC}), receiver enabled (RE at 0 V), no load, V_I = 0 V or V_{CC}	-55°C to +125°C	01		15	mA
		Driver enabled (DE at V_{CC}), receiver disabled (RE at V_{CC}), no load, V_I = 0 V or V_{CC}				14	
		Driver disabled (DE at 0 V), receiver enabled (RE at 0 V), no load				9	
		Driver disabled (DE at 0 V), receiver disabled (RE at V_{CC}), D open				1.5	µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

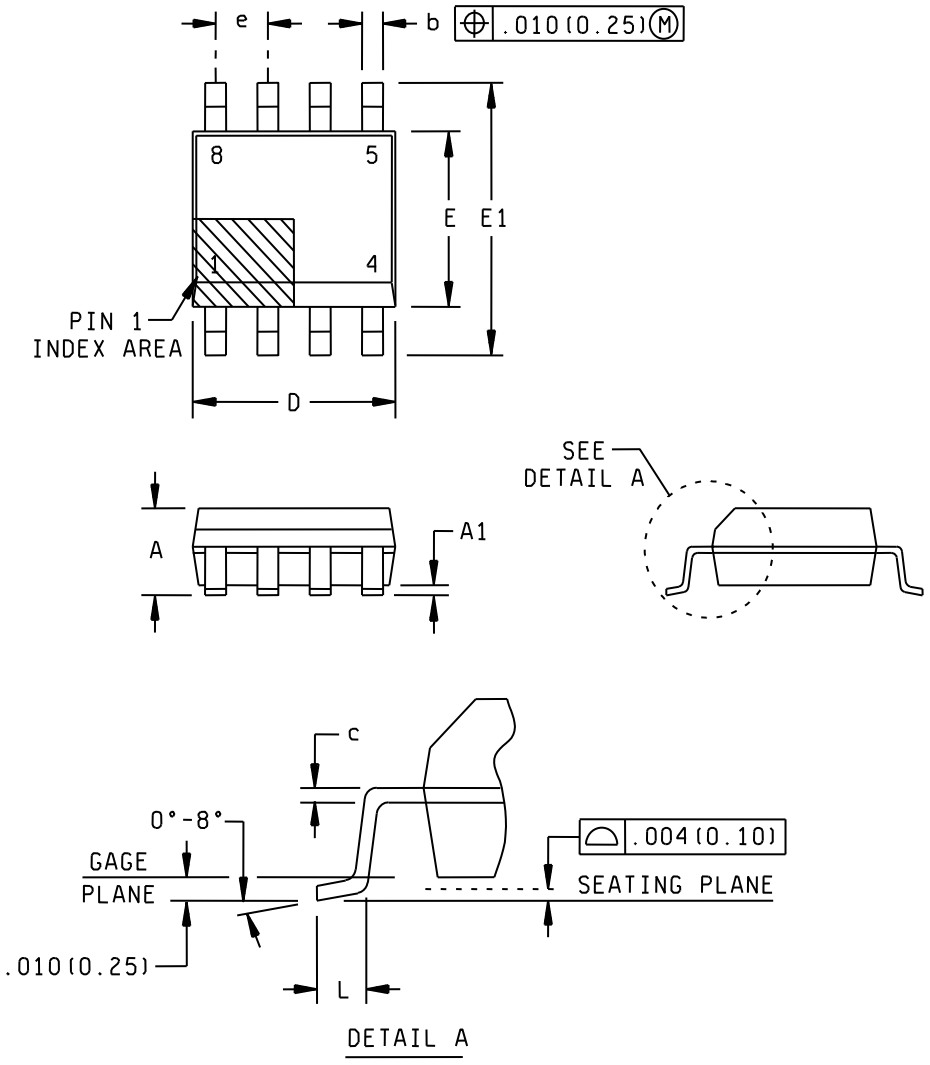


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.81	3.98
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) each side.
3. For dimension E, body width does not include interlead flash.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	R
2	$\overline{RE}$
3	DE
4	D
5	GND
6	A
7	B
8	V_{CC}

FIGURE 2. Terminal connections.

Driver function table

Input	Enable	Outputs	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	Open	Z	Z
Open	H	H	L

H = High level
L = Low level
X = Don't care
Z = High impedance (off)
? = Indeterminate

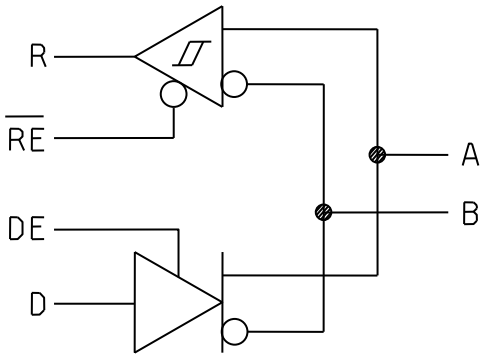
Receiver function table

Differential input	Enable	Output
$V_{ID} = (V_A - V_B)$	$\overline{RE}$	R
$0.2\ V \leq V_{ID}$	L	H
$-0.2\ V < V_{ID} < 0.2\ V$	L	H (see note)
$V_{ID} \leq -0.2\ V$	L	L
X	H	Z
X	Open	Z
Open circuit	L	H
Short circuit	L	H
Idle (terminated) bus	L	H

H = High level, L = Low level, Z = High impedance (off)

NOTE: If the differential input V_{ID} remains within the transition range for more than 250 μs, the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See figure 19.

FIGURE 3. Truth tables.



POSITIVE LOGIC

FIGURE 4. Logic diagram.

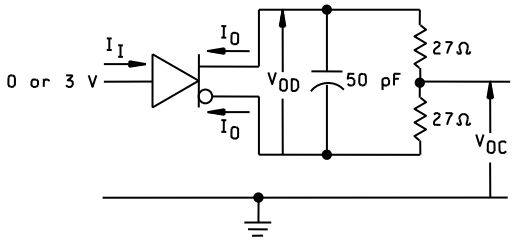


FIG 5. DRIVER TEST CIRCUIT, V_{OD} AND V_{OC} WITHOUT COMMON-MODE LOADING

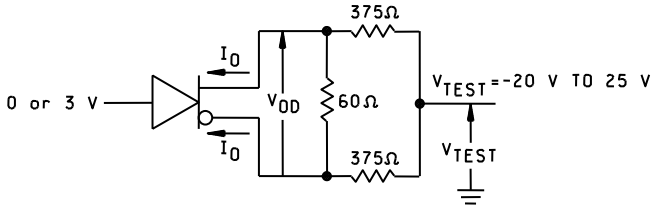


FIG 6. DRIVER TEST CIRCUIT, V_{OD} WITH COMMON-MODE LOADING

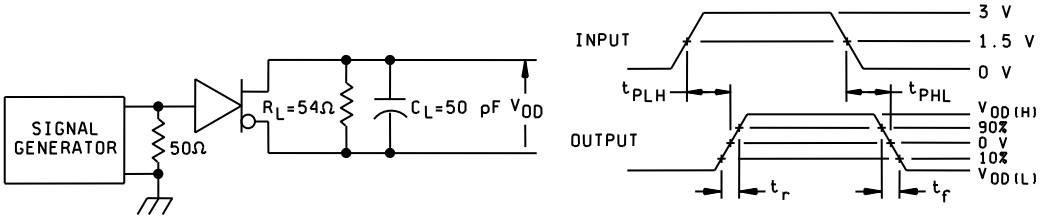


FIG 7. DRIVER SWITCHING TEST CIRCUIT AND WAVEFORMS

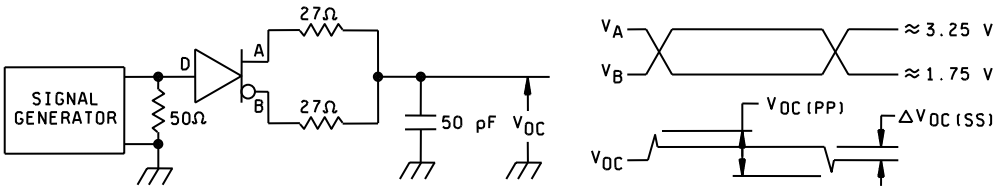


FIG 8. DRIVER V_{OC} TEST CIRCUIT AND WAVEFORMS

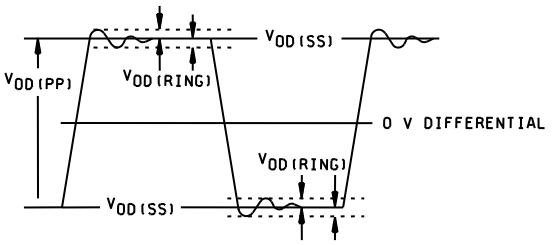


FIG 9. $V_{OD(RING)}$ WAVEFORMS AND DEFINITIONS

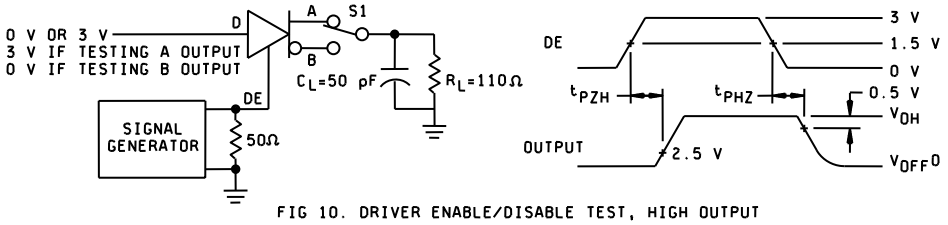


FIG 10. DRIVER ENABLE/DISABLE TEST, HIGH OUTPUT

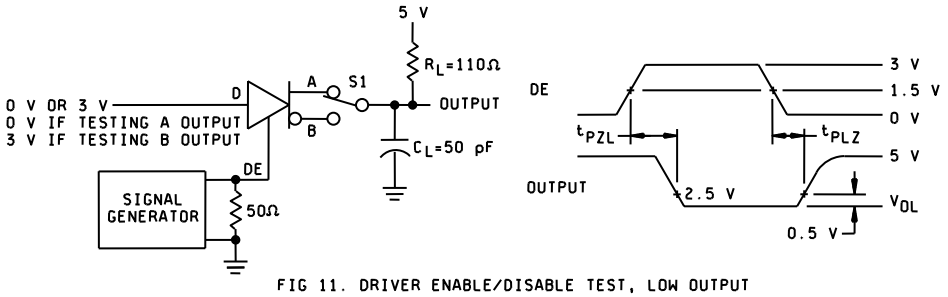


FIG 11. DRIVER ENABLE/DISABLE TEST, LOW OUTPUT

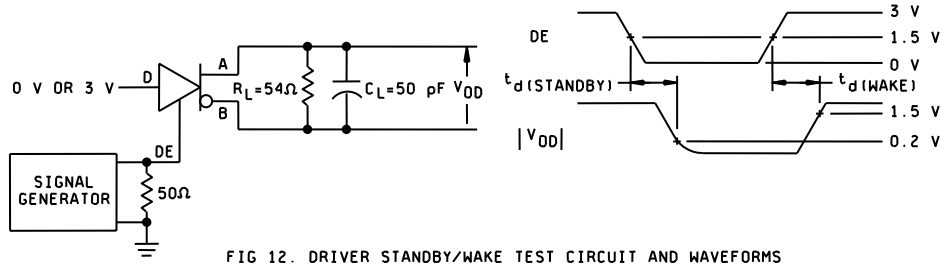


FIG 12. DRIVER STANDBY/WAKE TEST CIRCUIT AND WAVEFORMS

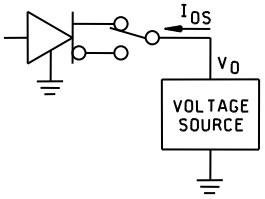


FIG 13. DRIVER SHORT-CIRCUIT TEST

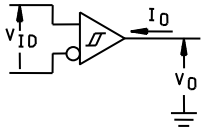


FIG 14. RECEIVER DC PARAMETER DEFINITIONS

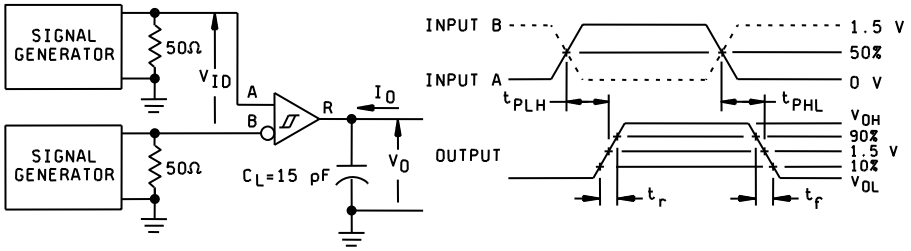


FIG 15. RECEIVER SWITCHING TEST CIRCUIT AND WAVEFORMS

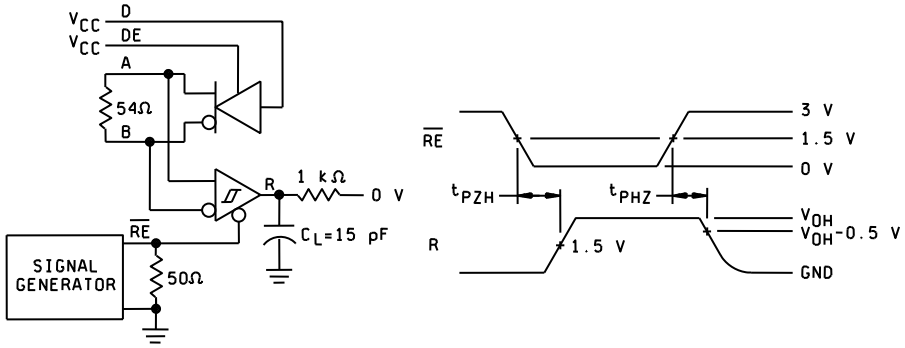


FIG 16. RECEIVER ENABLE TEST CIRCUIT AND WAVEFORMS, DATA OUTPUT HIGH

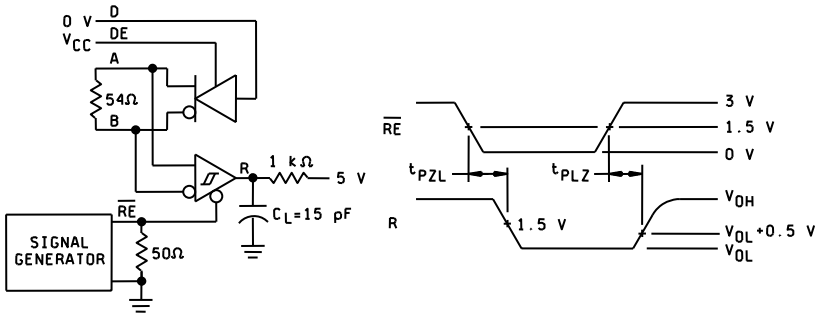


FIG 17. RECEIVER ENABLE TEST CIRCUIT AND WAVEFORMS, DATA OUTPUT LOW

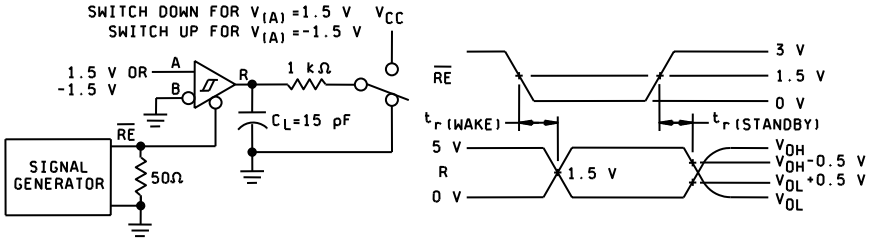


FIG 18. RECEIVER STANDBY AND WAKE TEST CIRCUIT AND WAVEFORMS

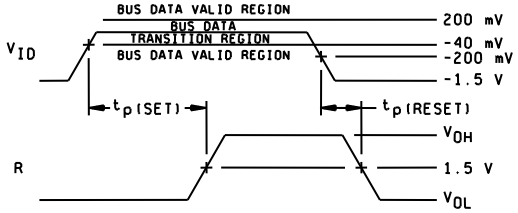


FIG 19. RECEIVER ACTIVE FAILSAFE DEFINITIONS AND WAVEFORMS

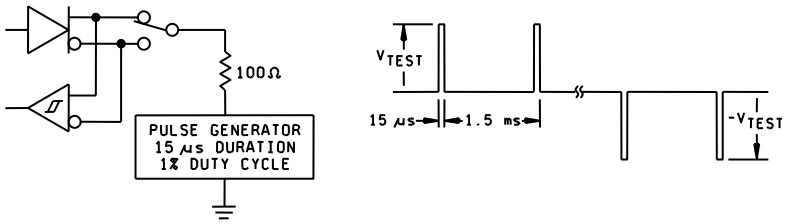


FIG 20. TEST CIRCUIT AND WAVEFORMS, TRANSIENT OVERVOLTAGE TEST

NOTES:

1. Test load capacitance includes probe and jig capacitance (unless otherwise specified).
2. Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50 % duty cycle Z_O = 50 Ω.
3. For figure 9, $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Cable length and 2/ signaling rate	Nodes	Tope side marking	Vendor part number
V62/06615-01XE	01295	Up to 150 m at 5 Mbps (with slew rate limit)	Up to 256	V21MEP	SN65HVD21MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Distance and signaling rate predictions based upon Belden 3105A cable and 15 % eye pattern jitter.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243