REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE	18																					
REV STATUS OF PAGES			**REV**																			
			PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-02-21	**CHECKED BY** TOM HESS **APPROVED BY** RAYMOND MONNIN	**TITLE** MICROCIRCUIT, LINEAR, PHASE SHIFT PULSE WIDTH MODULATION CONTROLLER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06614**
	REV	**PAGE** 1 **OF** 18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance phase shift pulse width modulation controller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	UCC2895-EP	Phase shift pulse width modulation controller

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013-AC	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage (with $I_{DD} < 10$ mA) ..... 17 V maximum
Supply current ..... 30 mA maximum
REF current ..... 15 mA maximum
OUT current ..... 100 mA maximum
Analog inputs:
EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB ..... -0.3 V to REF + 0.3 V
Power dissipation (P_D) at $T_A = 25°C$ ..... 650 mW
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Junction temperature range (T_J) ..... -55°C to 125°C
Lead temperature, soldering 10 seconds ..... 300°C
Thermal resistance, junction to ambient (θ_{JC}) ..... 29.8°C/W
Thermal resistance, junction to ambient (θ_{JA}) ..... 96.6°C/W

1.4 Recommended operating conditions. 3/

Supply voltage ..... 12 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Currents are positive into and negative out of the specified terminal.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Under voltage lock out (UVLO) section							
Start threshold			-55°C to +125°C	01	10.2	11.8	V
Stop threshold			-55°C to +125°C	01	8.2	9.8	V
Hysteresis			-55°C to +125°C	01	1	3	V
Supply voltage section							
Start up current		V_{DD} = 8 V	-55°C to +125°C	01		250	µA
I_{DD} active			-55°C to +125°C	01		6	mA
V_{CC} clamp voltage		I_{DD} = 10 mA	-55°C to +125°C	01	16.5	18.5	V
Voltage reference section							
Output voltage			T_J = +25°C	01	4.94	5.06	V
		10 V < V_{DD} < 17.5 V, 0 mA < I_{REF} < 5 mA	-55°C to +125°C		4.85	5.15	
Short circuit current		REF = 0 V	T_J = +25°C	01	10		mA
Error amplifier section							
Common mode input voltage			-55°C to +125°C	01	-0.1	3.6	V
Offset voltage			-55°C to +125°C	01	-7	7	mV
Input bias current (EAP, EAN)			-55°C to +125°C	01	-1	1	µA
EAOUT V_{OH}		EAP-EAN = 500 mV, I_{EAOUT} = -0.5 mA	-55°C to +125°C	01	4	5	V
EAOUT V_{OL}		EAP-EAN = 500 mV, I_{EAOUT} = 0.5 mA	-55°C to +125°C	01	0	0.4	V
EAOUT source current		EAP-EAN = 500 mV, EAOUT = 2.5 V	-55°C to +125°C	01	1		mA
EAOUT sink current		EAP-EAN = -500 mV, EAOUT = 2.5 V	-55°C to +125°C	01	2.5		mA
Open loop DC gain			-55°C to +125°C	01	75		dB
Unity gain bandwidth		3/	-55°C to +125°C	01	5		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Error amplifier section - continued							
Slew rate		EAN from 1 V to 0 V, 3/ EAP = 500 mV, EAOUT from 0.5 V to 3 V	-55°C to +125°C	01	1.5		V/µs
No load comparator turn-off threshold			-55°C to +125°C	01	0.45	0.55	V
No load comparator turn-on threshold			-55°C to +125°C	01	0.55	0.69	V
No load comparator hysteresis			-55°C to +125°C	01	0.035	0.165	V
Oscillator section							
Frequency			T_J = +25°C	01	473	527	kHz
Total variation		Line, temperature 3/	-55°C to +125°C	01		5	%
SYNC V_{IH}			-55°C to +125°C	01	2.05	2.32	V
SYNC V_{IL}			-55°C to +125°C	01	1.85	1.95	V
SYNC V_{OH}		I_{SYNC} = -400 µA, C_T = 2.6 V	-55°C to +125°C	01	4.1	5	V
SYNC V_{OL}		I_{SYNC} = 100 µA, C_T = 0 V	-55°C to +125°C	01	0	1	V
SYNC output pulse width		SYNC load = 3.9 kΩ and 30 pF in parallel	-55°C to +125°C	01		135	ns
R_T voltage			-55°C to +125°C	01	2.9	3.1	V
C_T peak voltage			-55°C to +125°C	01	2.25	2.55	V
C_T valley voltage			-55°C to +125°C	01	0	0.65	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
PWM comparator section							
EAOUT to RAMP/ input offset voltage		RAMP = 0 V, DELAB = DELCD = REF	-55°C to +125°C	01	0.72	1.05	V
Minimum phase shift (OUTA to OUTC, OUTB to OUTD)		RAMP = 0 V, EAOUT = 650 mV 4/	-55°C to +125°C	01	0	1.50	%
RAMP to OUTC/OUTD delay		RAMP from 0 V to 2.5 V, EAOUT = 1.2 V, DELAB = DELCD = REF 5/	-55°C to +125°C	01		120	ns
RAMP bias current		RAMP < 5 V, C_T < 2.2 V	-55°C to +125°C	01	-5	5	μA
RAMP sink current		RAMP = 5 V, C_T < 2.6 V	-55°C to +125°C	01	12		mA
Current sense section							
CS bias current		0 < CS < 2.5 V, 0 < ADS < 2.5 V	-55°C to +125°C	01	-4.5	20	μA
Peak current threshold			-55°C to +125°C	01	1.9	2.1	V
Over current threshold			-55°C to +125°C	01	2.4	2.6	V
CS to output delay		CS from 0 to 2.3 V DELAB = DELCD = REF	-55°C to +125°C	01		110	ns
Soft start / shutdown section							
Soft start source current		SS/DISB = 3 V, CS = 1.9 V	-55°C to +125°C	01	-40	-30	μA
Soft start sink current		SS/DISB = 3 V, CS = 2.6 V	-55°C to +125°C	01	325	375	μA
Soft start / disable comparator threshold			-55°C to +125°C	01	0.44	0.56	V
Delay set section							
DELAB / DELCD output voltage		ADS = CS = 0 V	-55°C to +125°C	01	0.45	0.55	V
		ADS = 0 V, CS = 2 V			1.9	2.1	
Output delay		ADS = CS = 0 V 3/ 5/	-55°C to +125°C	01	450	600	ns
ADS bias current		0 V < ADS < 2.5 V, 0 V < CS < 2.5 V	-55°C to +125°C	01	-20	20	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output section							
V_{OH} (all outputs)		I_{OUT} = -10 mA, V_{DD} to output	-55°C to +125°C	01		400	mV
V_{OL} (all outputs)		I_{OUT} = 10 mA	-55°C to +125°C	01		270	mV
Rise time		C_{LOAD} = 100 pF 3/	-55°C to +125°C	01		35	ns
Fall time		C_{LOAD} = 100 pF 3/	-55°C to +125°C	01		35	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 μF, C_{VDD} = 1 μF, and no load at outputs.

3/ Specified by design. Not production tested.

4/ Minimum phase shift is defined as:

$\Phi = 200 \times (t_{f(OUTA)} - t_{f(OUTC)}) / t_{PERIOD}$ or $\Phi = 200 \times (t_{f(OUTB)} - t_{f(OUTD)}) / t_{PERIOD}$

where: $t_{f(OUTA)}$ = falling edge of OUTA signal,

$t_{f(OUTB)}$ = falling edge of OUTB signal,

$t_{f(OUTC)}$ = falling edge of OUTC signal,

$t_{f(OUTD)}$ = falling edge of OUTD signal

t_{PERIOD} = period of OUTA or OUTB signal

5/ Output delay is measured between OUTA / OUTB or OUTC/ / OUTD. Output delay is shown in figure 4, where:

$t_{f(OUTA)}$ = falling edge of OUTA signal, $t_{r(OUTB)}$ = rising edge of OUTB signal

Case X

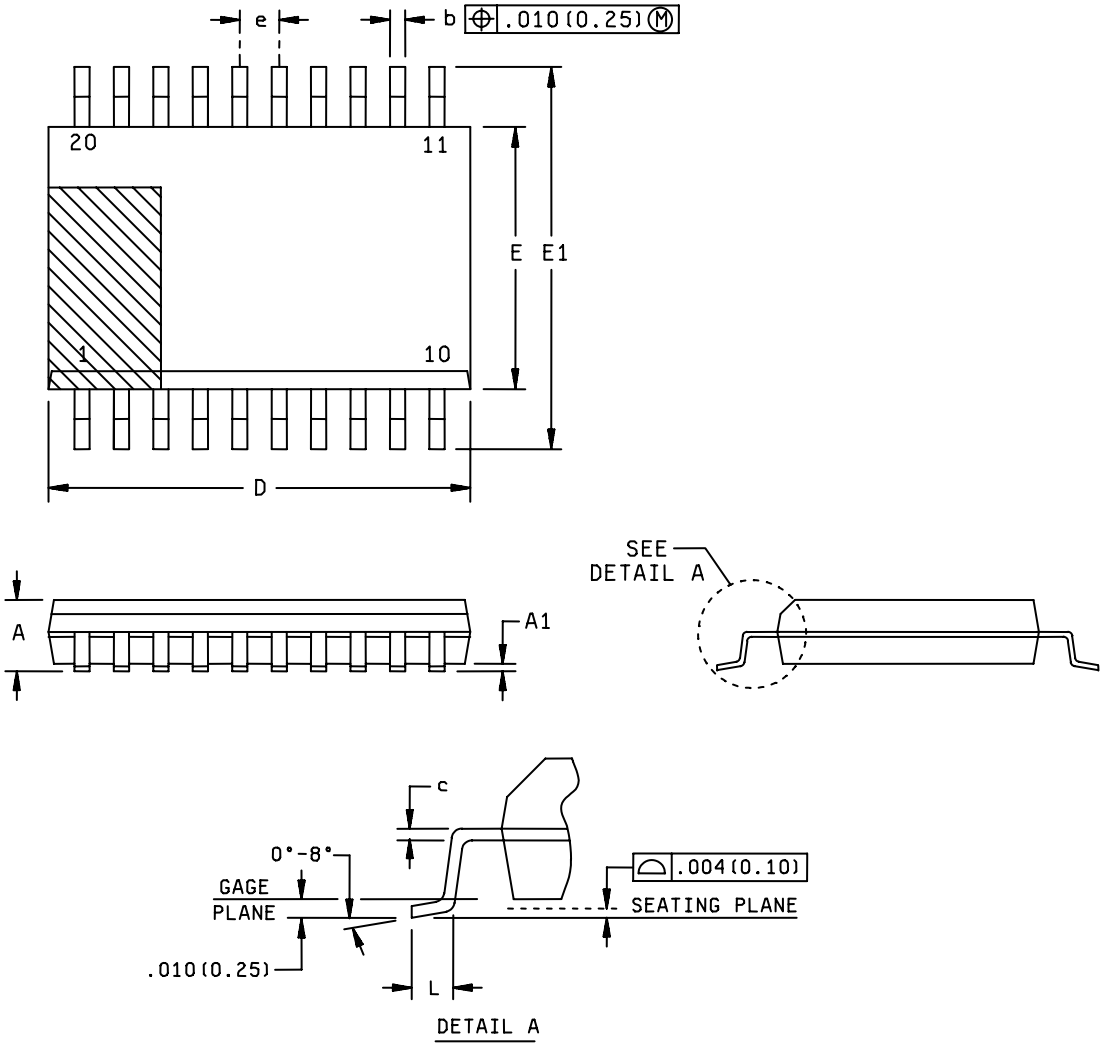


FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE **A**	CODE IDENT NO. **16236**	DWG NO. **V62/06614**
		REV	PAGE 9

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.104	---	2.65
A1	.004	.012	0.10	0.30
b	.012	.020	0.31	0.51
c	.008	.013	0.20	0.33
D	.496	.512	12.60	13.00
e	.050	NOM	1.27	NOM
E	.291	.299	7.40	7.60
E1	.393	.419	9.97	10.63
L	.016	.050	0.40	1.27
n		20		20

NOTES:
1. Controlling dimensions are inch. Millimeter dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion not to exceed .006 inch (0.15 mm).
3. Falls within JEDEC MS-013 variation AC.

FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	EAN
2	EAOUT
3	RAMP
4	REF
5	GND
6	SYNC
7	C_T
8	R_T
9	DELAB
10	DELCD
11	ADS
12	CS
13	OUTD
14	OUTC
15	V_{DD}
16	PGND
17	OUTB
18	OUTA
19	SS/DISB
20	EAP

FIGURE 2. Terminal connections.

Terminal symbol	Description
ADS	Adaptive delay set. This function sets the ratio between the maximum and minimum programmed output delay dead time. When ADS is directly connected to CS, no delay modulation occurs. Maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2 V (the peak current threshold). ADS changes the output voltage on the delay (DELAB and DELCD) pins by: $V_{DEL} = [0.75 \times (V_{CS} - V_{ADS})] + 0.5\ V$ where V_{CS} and V_{ADS} are in volts. ADS must be limited to between 0 V and 2.5 V and must be less than, or equal to CS. DELAB and DELCD also are clamped to minimum of 0.5 V
CS	Current sense. CS is the inverting input of the current sense comparator, and the noninverting input of the over current comparator and the ADS amplifier. The CS signal is used for cycle by cycle current limiting in peak current mode control, and for over current protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an over current fault also results in a restart cycle, called soft stop, with full soft start.
C_T	Oscillator timing capacitor (see figure 5). The device oscillator charges C_T via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by: $t_{OSC} = ((5 \times R_T \times C_T) / 48) + 120\ ns$ where C_T is in farads, R_T is in ohms, and t_{OSC} is in seconds. C_T can range from 100 pF to 880 pF. Note that a large C_T and a small R_T combination results in extended fall times on the C_T waveform. The increased fall time increases the SYNC pulse width, therefore, limiting the maximum phase shift between OUTA / OUTB and OUTC / OUTD outputs, which limits the maximum duty cycle of the converter.
DELAB, DELCD	Delay programming between complementary outputs. DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The device allows the user to select the delay in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half bridges to accommodate differences in resonant capacitor charging currents. The delay in each stage is set according to the formula: $t_{DELAY} = [((25 \times 10^{-12}) \times R_{DEL}) / V_{DEL}] + 25\ ns$ where V_{DEL} is in volts, R_{DEL} is in ohms, and t_{DELAY} is in seconds. DELAB and DELCD can source approximately 1 mA maximum. Delay resistors must be chosen so that this maximum is not exceeded. Programmable output delay can be defeated by tying DELAB and/or DELCD to REF. For optimum performance keep stray capacitance on these pins at $<$ 10 pF.

FIGURE 2. Terminal connections – Continued.

Terminal symbol	Description
EAN	Error amplifier negative. Inverting input to the error amplifier.
EAOUT	Error amplifier output. EAOUT also is connected internally to the noninverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft start voltage. The no load comparator shuts down the outputs stages when EAOUT falls below 500 mW, and allows the outputs to turn on again when EAOUT rises above 600 mV.
EAP	Error amplifier positive. Noninverting input to the error amplifier.
GND	Ground. Chip ground for all circuits except the output stages.
OUTA OUTB OUTC OUTD	Outputs. These outputs are 100 mA complementary MOS drivers, and are optimized to drive FET driver circuits. OUTA and OUTB are fully complementary (assuming no programmed delay). They operate near 50% duty cycle and one-half the oscillator frequency. OUTA and OUTB are intended to drive one half bridge circuit in an external power stage. OUTC and OUTD drive the other half bridge and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB. Note that changing the phase relationship of OUTC and OUTD, with respect to OUTA and OUTB, requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.
PGND	Output stage ground. To keep output switching noise from critical analog circuits, the device has two different ground connections. PGND is the ground connection for the high current output stages. Both GND and PGND must be electrically tied together closely near the integrated circuit. Also, since PGND carries high current, board traces must be low impedance.
RAMP	Inverting input of PWM comparator. RAMP receives either the C_T waveform in voltage and average current mode controls, or the current signal (plus slope compensation) in peak current mode control. An internal discharge transistor is provided on RAMP, which is triggered during the oscillator dead time.
R_T	Oscillator timing resistor (see figure 5). The oscillator in the device operates by charging an external timing capacitor, C_T, with a fixed current programmed by R_T. R_T current is calculated as: $I_{RT(A)} = 3\ V / R_T$ ohm where R_T is in ohms and I_{RT} is in amperes. R_T can range from 40 kΩ to 120 kΩ. Soft start charging and discharging current are also programmed by I_{RT}.
REF	5 V ±1.2% voltage reference. REF supplies power to internal circuitry, and can also supply up to 5 mA to external loads. The reference is shut down during undervoltage lockout but is operational during all other disable modes. For best performance, bypass with a 0.1 μF low ESR, low ESL capacitor to ground.

FIGURE 2. Terminal connections – Continued.

Terminal symbol	Description
SS/DISB	Soft start/disable. SS/DISB combines two independent functions:
	Disable mode. A rapid shutdown of the chip is accomplished by any one of the following: externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, V_{DD} dropping below the UVLO threshold, or an overcurrent fault is sensed (CS = 2.5 V). In the case of REF pulled below 4 V or an UVLO condition, SS/DISB actively is pulled to ground via an internal MOSFET switch. If an overcurrent is sensed SS/DISB sinks a current of 10 x I_{RT} until SS/DISB falls below 0.5 V. Note that if SS/DISB is externally forced below 0.5 V, the pin starts to source current equal to I_{RT}. Also note that the only time the part switches into the low I_{DD} current mode is when the part is in undervoltage lockout.
	Soft start mode. After a fault or disable condition has passed and V_{DD} is above the start threshold and/or SS/DISB falls below 0.5 V during a soft start, SS/DISB switches to a soft start mode. The pin now sources current equal to I_{RT}. A user selected capacitor on SS/DISB determines the soft start and soft start time. In addition, a resistor in parallel with the capacitor may be used, limiting the maximum voltage on SS/DISB. Note that SS/DISB actively clamps the EAOUT voltage to approximately the SS/DISB voltage during both soft start, soft stop, and disable conditions.
SYNC	Synchronization (see figure 5). SYNC is bidirectional. When used as an output, SYNC can be used as a clock, which is the same as the chip's internal clock. When used as an input, SYNC overrides the chip's internal oscillator and acts as its clock signal. This bidirectional feature allows synchronization of multiple power supplies. SYNC also internally discharges the C_T capacitor and any filter capacitors that are present on RAMP. The internal SYNC circuitry is level sensitive, with an input low threshold of 1.9 V and an input high threshold of 2.1 V. A resistor as small as 3.9 kΩ may be tied between SYNC and GND to reduce the synchronization pulse width.
V_{DD}	Power supply. V_{DD} must be bypassed with a minimum of a 1.0 μF low ESR, low ESL capacitor to ground.

FIGURE 2. Terminal connections – Continued.

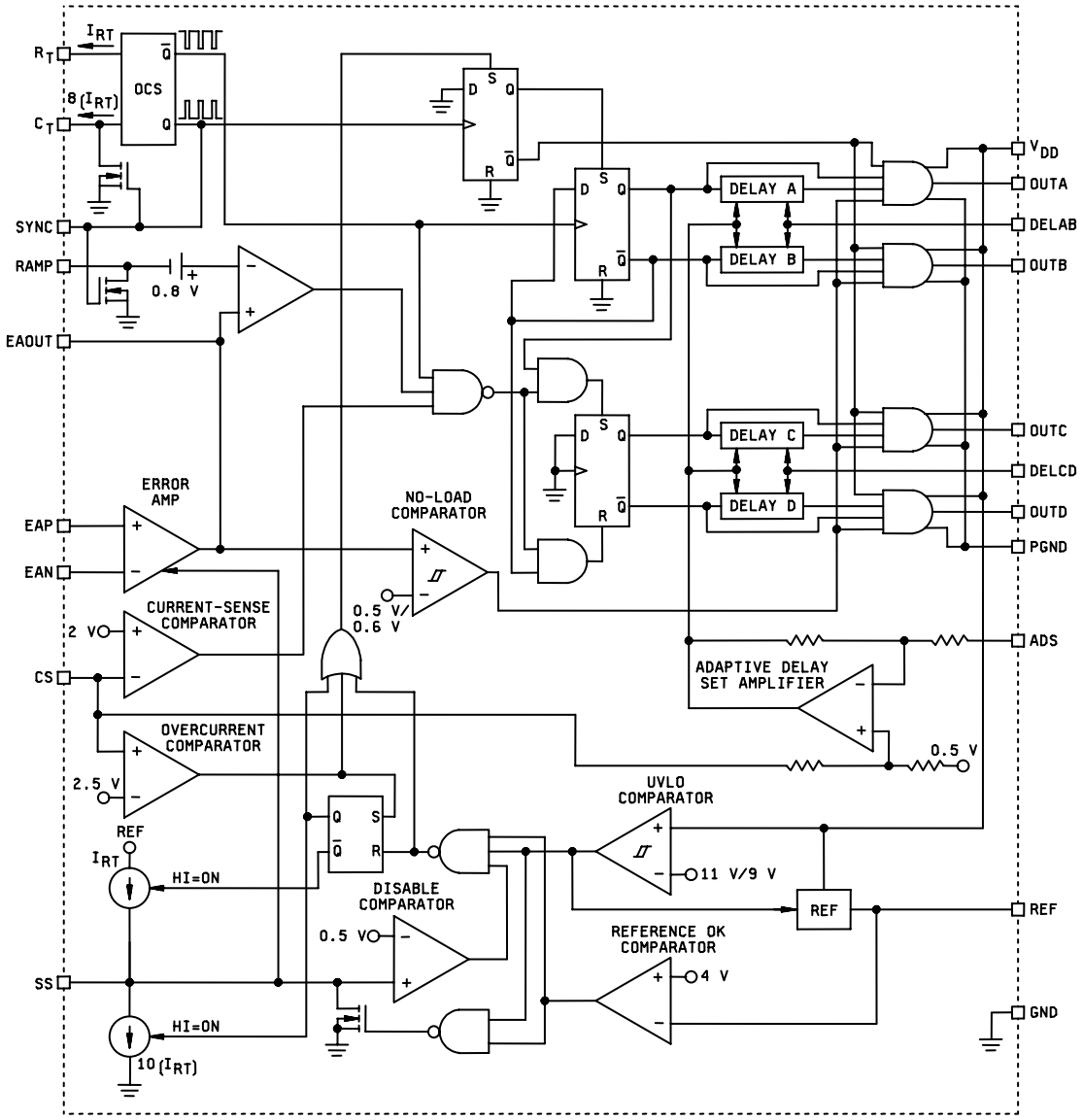
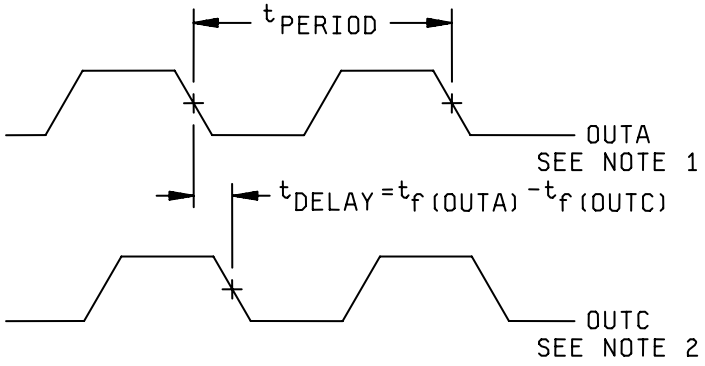
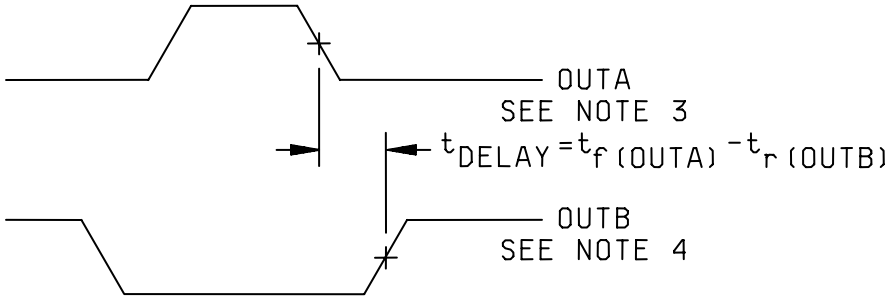


FIGURE 3. Logic diagram.



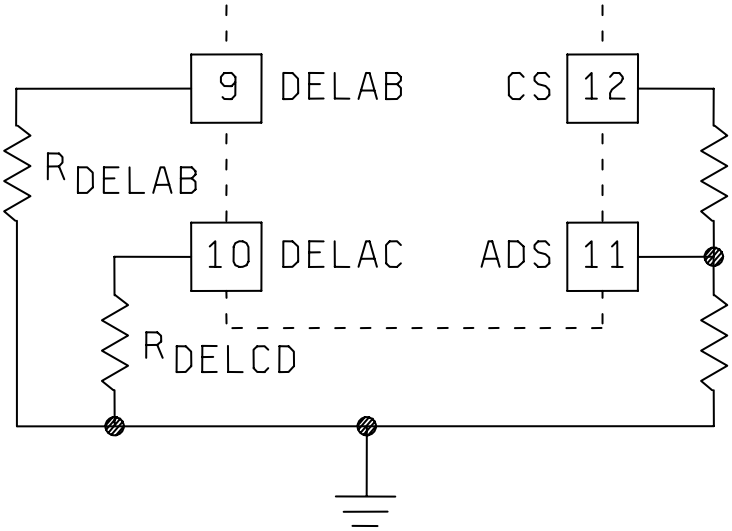
OUTA / OUTC output delay



OUTA / OUTB output delay

NOTES:
1. Also applies to OUTB.
2. Also applies to OUTD.
3. Also applies to OUTC.
4. Also applies to OUTD.

FIGURE 4. Timing waveforms.



NOTE: This figure shows the resistors needed to program the delay periods and the ADS function.

FIGURE 5. Resistors needed in programming.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Vendor part number	Top side marking
V62/06614-01XE	01295	SOIC - DW	UCC2895MDWREP	UCC2895MEPG4

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493