| REVISIONS | | | |
|---|---|---|---|
| **LTR** | **DESCRIPTION** | **DATE** | **APPROVED** |
| A | Update document paragraphs to current requirements. - ro | 14-06-25 | C. SAFFLE |
| B | Update JEDEC package from MO-178-AB to MO-178. Update the maxim “L” dimension under Figure 1. Separate figure 5 timing diagrams into single figure numbers and delete paragraph 3.5.5. Update document paragraphs to current requirements. - ro | 20-06-17 | J. ESCHMEYER |

**CURRENT DESIGN ACTIVITY CAGE CODE 16236**
**HAS CHANGED NAMES TO:**
**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV** | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | |
| **REV** | B | B | | | | | | | | | | | | | | | | | | | |
| **PAGE** | 18 | 19 | | | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV STATUS OF PAGES** | **REV** | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| | **PAGE** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |

| | | |
|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>RICK OFFICER | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43218-3990** |
| Original date of drawing<br>YY-MM-DD<br>06-01-24 | **CHECKED BY**<br>TOM HESS | **TITLE**<br>MICROCIRCUIT, DIGITAL-LINEAR, 1 OHM, SPDT ANALOG SWITCH, MONOLITHIC SILICON |
| | **APPROVED BY**<br>RAYMOND MONNIN | |
| | **SIZE** **A** / **CODE IDENT. NO.** **16236** | **DWG NO.** **V62/06613** |
| | **REV** **B** | **PAGE** 1 **OF** 19 |

AMSC N/A

5962-V033-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance one ohm SPDT analog switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/06613 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | TS5A3159-EP | 1 ohm SPDT analog switch |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 6 | MO-178 | Plastic small outline |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Supply voltage range ( V+ ) ..... -0.5 V to 6.5 V 2/
Analog voltage range ( $V_{NO}$, $V_{COM}$ ) .....-0.5 V to V+ + 0.5 V 2/ 3/ 4/
Analog port diode current ( $I_{I/OK}$ ) :
$V_{NO}$, $V_{COM}$ < 0 or $V_{NO}$, $V_{COM}$ > V+ ..... ±50 mA
On state switch current ( $I_{NO}$, $I_{COM}$ ):
$V_{NO}$, $V_{COM}$ = 0 to V+ ..... ±200 mA
On state peak switch current ..... ±400 mA 5/
Digital input voltage range ( $V_{IN}$ ) ..... -0.5 V to 6.5 V 2/ 3/
Digital input clamp current ($I_{IK}$) ( $V_{IN}$ < 0 ) ..... -50 mA
Continuous current through V+ or GND ..... ±100 mA
Storage temperature range ( Tstg ) ..... -65°C to +150°C
Package thermal impedance ( $\theta_{JA}$ ) ..... 165°C/W 6/

1.4 Recommended operating conditions. 7/

Supply voltage range ( V+ ) ..... -4.5 V to 5.5 V
Operating free-air temperature range ($T_A$) ..... -55°C to +125°C

---

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages are with respect to ground, unless otherwise specified.
3/ The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
4/ This value is limited to 5.5 V maximum.
5/ Pulse at 1 ms duration < 10 % duty cycle.
6/ The package thermal impedance is calculated in accordance with JESD 51-7.
7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Parameter description table. The parameter description table shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Analog switch section | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NC}$, $V_{NO}$ | | -55°C to +125°C | 01 | 0 | V+ | V |
| Peak ON resistance | $r_{peak}$ | 0 ≤ $V_{NO}$ or $V_{NC}$ ≤ V+, switch on, $I_{COM}$ = -30 mA, see figure 5, V+ = 4.5 V | +25°C | 01 | | 1.5 | Ω |
| | | | -55°C to +125°C | | | 1.5 | |
| ON state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2.5 V, switch on, $I_{COM}$ = -30 mA, see figure 5, V+ = 4.5 V | +25°C | 01 | | 1.1 | Ω |
| | | | -55°C to +125°C | | | 1.3 | |
| ON state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2.5 V, switch on, $I_{COM}$ = -30 mA, see figure 5, V+ = 4.5 V | +25°C | 01 | 0.1 typical | | Ω |
| On state resistance flatness | $r_{on(flat)}$ | 0 ≤ $V_{NO}$ or $V_{INC}$ ≤ V+, switch on, $I_{COM}$ = -30 mA, see figure 5, V+ = 4.5 V | +25°C | 01 | 0.233 typical | | Ω |
| | | $V_{NO}$ or $V_{NC}$ = 1 V, 1.5 V, 2.5 V, $I_{COM}$ = -30 mA, switch on, see figure 5, V+ = 4.5 V | | | 0.15 typical | | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 4.5 V, $V_{COM}$ = 0 , V+ = 5.5 V, switch off, see figure 6 | +25°C | 01 | -6 | 4 | nA |
| | | | -55°C to +125°C | | -20 | 60 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 4.5 V, $V_{COM}$ = open , V+ = 5.5 V, switch on, see figure 7 | +25°C | 01 | -6 | 4 | nA |
| | | | -55°C to +125°C | | -40 | 70 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = 4.5 V, or open $V_{COM}$ = 4.5 V, V+ = 5.5 V, switch on, see figure 7 | +25°C | 01 | -4 | 7 | nA |
| | | | -55°C to +125°C | | -40 | 80 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Digital control input ( IN ) section | | | | | | | |
| Input logic high voltage | $V_{IH}$ | | -55°C to +125°C | 01 | 2.4 | 5.5 | V |
| Input logic low voltage | $V_{IL}$ | | -55°C to +125°C | 01 | 0 | 0.8 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0, V+ = 5.5 V | -55°C to +125°C | 01 | -1 | 1 | µA |
| Dynamic section | | | | | | | |
| Turn on time | $t_{ON}$ | $V_{COM}$ = V+, $C_L$ = 35 pF, $R_L$ = 50 Ω, see figure 8, V+ = 4.5 V to 5.5 V | +25°C | 01 | | 35 | ns |
| | | | -55°C to +125°C | | | 40 | |
| Turn off time | $t_{OFF}$ | $V_{COM}$ = V+, $C_L$ = 35 pF, $R_L$ = 50 Ω, see figure 8, V+ = 4.5 V to 5.5 V | +25°C | 01 | | 20 | ns |
| | | | -55°C to +125°C | | | 35 | |
| Break before make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = V+ / 2, $C_L$ = 35 pF, $R_L$ = 50 Ω, see figure 9, V+ = 4.5 V to 5.5 V | +25°C | 01 | 1 | 14.5 | ns |
| | | | -55°C to +125°C | | 1 | | |
| Charge injection | $Q_C$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, see figure 10, V+ = 5 V | +25°C | 01 | 36 typical | | pC |
| NC, NO, OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = V+ or GND, switch OFF, see figure 11, V+ = 5 V | +25°C | 01 | 23 typical | | pF |
| NC, NO, ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = V+ or GND, switch ON, see figure 11, V+ = 5 V | +25°C | 01 | 84 typical | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = V+ or GND, V+ 5 V, switch ON, see figure11 | +25°C | 01 | 84 typical | | pF |
| Digital input capacitance | $C_{IN}$ | $V_{IN}$ = V+ or GND, V+ = 5 V, see figure 11 | +25°C | 01 | 2.1 typical | | pF |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Dynamic section - continued | | | | | | | |
| Bandwidth | BW | $R_L$ = 50 Ω, switch ON, V+ = 5 V, see figure 12 | +25°C | 01 | 100 typical | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, switch OFF, V+ = 5 V, f = 1 MHz, see figure 13 | +25°C | 01 | -65 typical | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, switch ON, V+ = 5 V, f = 1 MHz, see figure 14 | +25°C | 01 | -65 typical | | dB |
| Talk harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, V+ = 5 V, f = 600 Hz to 20 kHz, see figure 15 | +25°C | 01 | 0.01 typical | | % |
| Supply section | | | | | | | |
| Positive supply current | I+ | $V_{IN}$ = V+ or GND, V+ = 5.5 V, switch ON or OFF | -55°C to +125°C | 01 | | 0.1 | μA |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V+ = 4.5 V to 5.5 V.

Case X

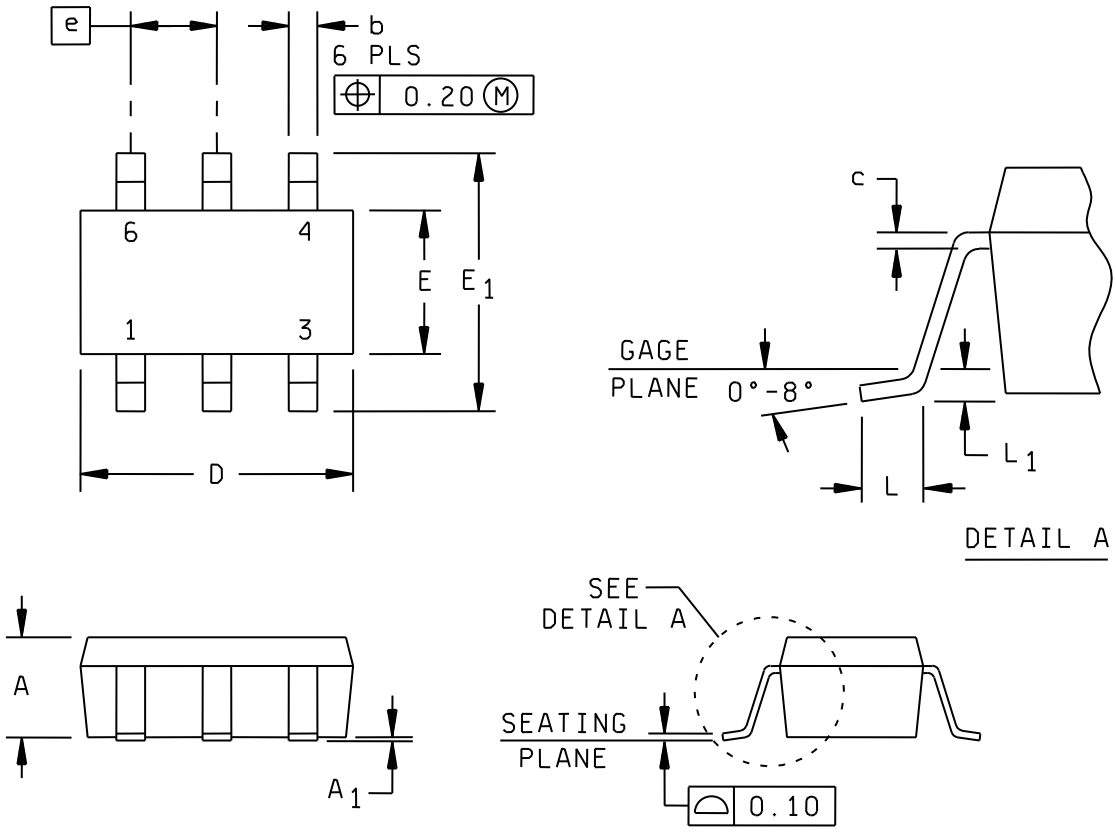



FIGURE 1. Case outline.

| DEFENSE SUPPLY CENTER, COLUMBUS<br>COLUMBUS, OHIO | SIZE<br>A | CODE IDENT NO.<br>16236 | DWG NO.<br>V62/06613 |
|---|---|---|---|
| | | REV B | PAGE 8 |

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | --- | 0.057 | --- | 1.45 |
| A1 | 0.000 | 0.005 | 0.00 | 0.15 |
| b | 0.009 | 0.019 | 0.25 | 0.50 |
| c | 0.003 | 0.008 | 0.08 | 0.22 |
| D | 0.108 | 0.120 | 2.75 | 3.05 |
| E | 0.057 | 0.068 | 1.45 | 1.75 |
| E1 | 0.102 | 0.118 | 2.60 | 3.00 |
| e | 0.037 BSC | | 0.95 BSC | |
| L | 0.011 | 0.024 | 0.30 | 0.60 |
| L1 | 0.009 BSC | | 0.25 BSC | |
| n | 6 | | 6 | |

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm ( .005 inch) per side.
3. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
4. Falls within JEDEC MO-178.

FIGURE 1. Case outline – Continued.

| Device type | 01 | |
|---|---|---|
| Case outline | X | |
| Terminal number | Terminal symbol | Description |
| 1 | NO | Normally open |
| 2 | GND | Digital ground |
| 3 | NC | Normally closed |
| 4 | COM | Common |
| 5 | V+ | Power supply |
| 6 | IN | Digital control pin to connect COM to NO or NC |

FIGURE 2. Terminal connections.

| IN | NC to COM, COM to NC | NO to COM, COM to NO |
|---|---|---|
| L | ON | OFF |
| H | OFF | ON |

FIGURE 3. Truth table.

| Symbol | Description |
|---|---|
| $V_{COM}$ | Voltage at COM. |
| $V_{NC}$ | Voltage at NC. |
| $V_{NO}$ | Voltage at NO. |
| $r_{on}$ | Resistance between COM and NO ports when the channel is ON. |
| $r_{peak}$ | Peak on state resistance over a specified voltage range. |
| $\Delta r_{on}$ | Difference of $r_{on}$ between channels in a specific device |
| $r_{on(flat)}$ | Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions. |
| $I_{NC(OFF)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst case input and output conditions. |
| $I_{NO(OFF)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state. |
| $I_{NC(ON)}$ | Leakage current measured at the NC port, with corresponding channel (NC to COM) in the ON state and the output (COM) open. |
| $I_{NO(ON)}$ | Leakage current measured at the NO port, with corresponding channel (NO to COM) in the ON state and the output (COM) open. |
| $I_{COM(ON)}$ | Leakage current measured at the COM port, with corresponding channel (COM to NO) in the ON state and the output (NO) open. |
| $V_{IH}$ | Minimum input voltage for logic high for the control input (IN). |
| $V_{IL}$ | Maximum input voltage for logic low for the control input (IN). |
| $V_{IN}$ | Voltage at IN. |
| $I_{IH}$, $I_{IL}$ | Leakage current measured at IN. |
| $t_{ON}$ | Turn on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON. |
| $t_{OFF}$ | Turn off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF. |

FIGURE 4. Parameter description table.

| Symbol | Description |
|---|---|
| $t_{BBM}$ | Break before make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state. |
| $Q_C$ | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.<br>Charge injection, $Q_C = C_L \times \Delta V_{COM}$, $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage. |
| $C_{NC(OFF)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF. |
| $C_{NO(OFF)}$ | Capacitance at the NO port when the corresponding channel (NC to COM) is OFF. |
| $C_{NC(ON)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON. |
| $C_{NO(ON)}$ | Capacitance at the NO port when the corresponding channel (NC to COM) is ON. |
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NO) is ON. |
| $C_{IN}$ | Capacitance of IN. |
| $O_{ISO}$ | OFF isolation of the switch is a measurement of OFF state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state. |
| $X_{TALK}$ | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain. |
| I+ | Static power supply current with the control (IN) pin at V+ or GND. |
| $\Delta$I+ | This is the increase in I+ for each control (IN) input that is at the specified voltage, rather than at V+ or GND. |

FIGURE 4. Parameter description table – Continued.

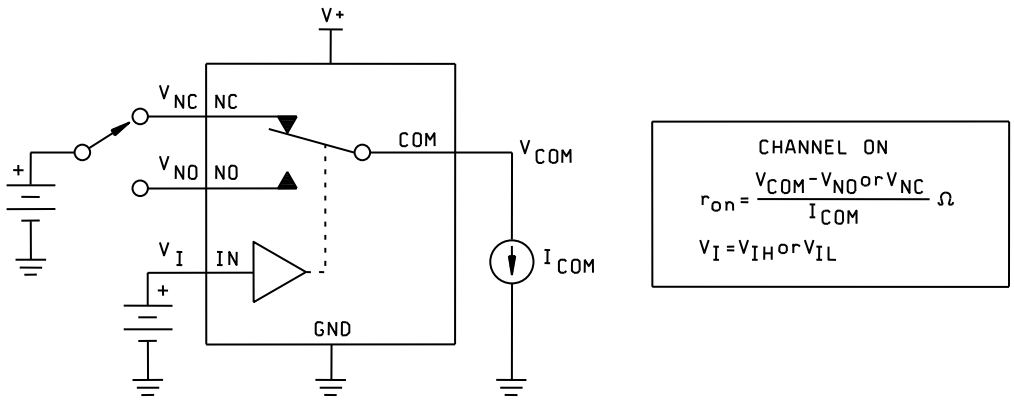



FIGURE 5. ON state resistance ( $r_{on}$ ).

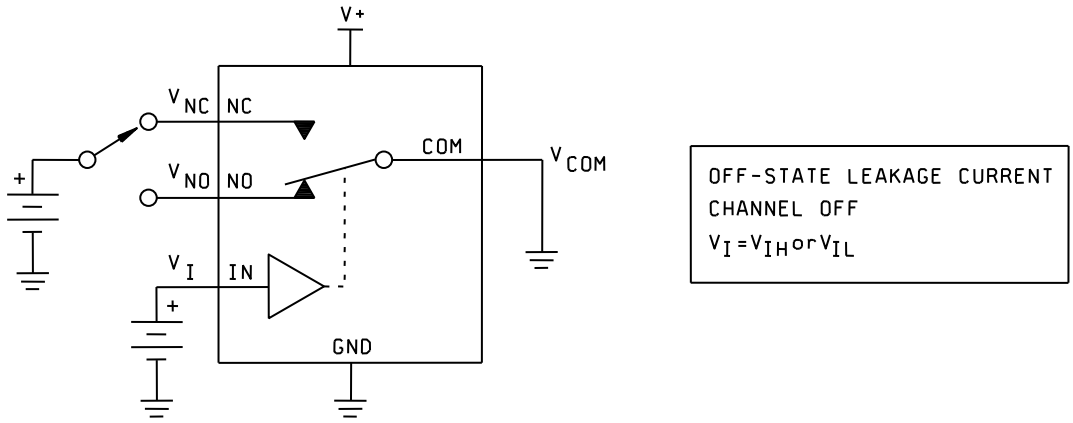
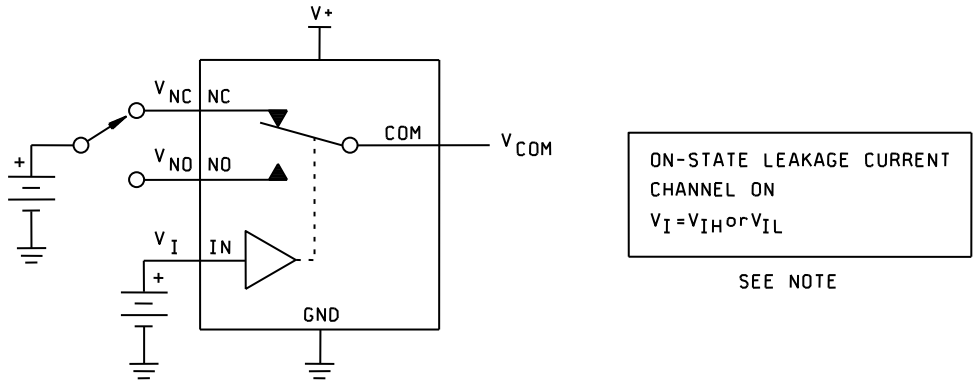
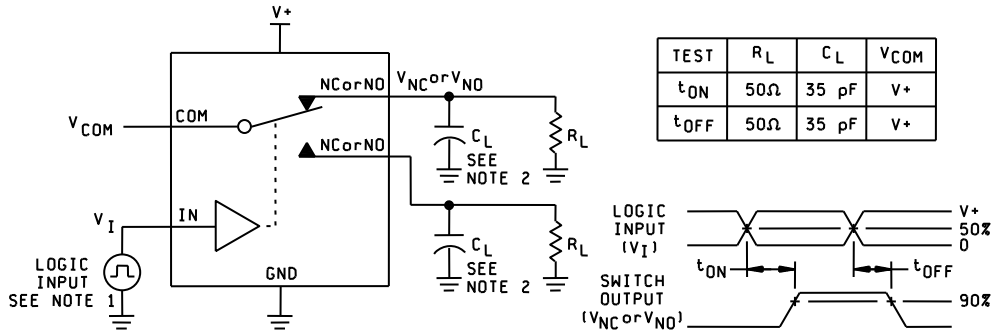



FIGURE 6. OFF state leakage current ( $I_{NC(OFF)}$, $I_{NO(OFF)}$ ).




NOTE: See electrical characteristics for test conditions.

FIGURE 7. ON state leakage current ( $I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$ ).

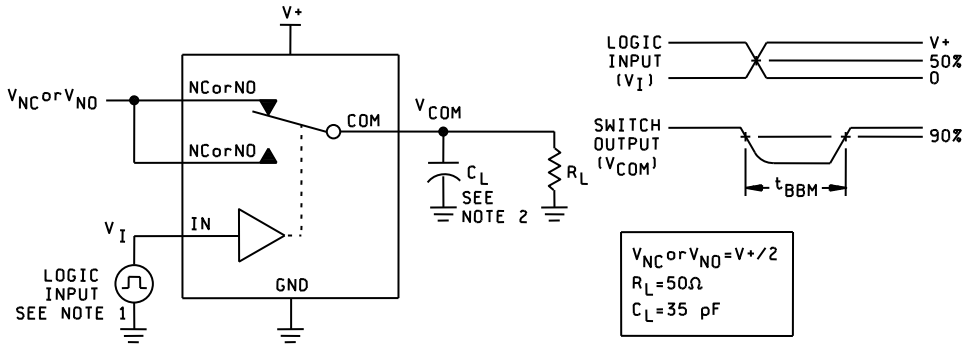



| TEST | $R_L$ | $C_L$ | $V_{COM}$ |
|---|---|---|---|
| $t_{ON}$ | 50Ω | 35 pF | V+ |
| $t_{OFF}$ | 50Ω | 35 pF | V+ |

NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.
2. $C_L$ includes probe and jig capacitance.

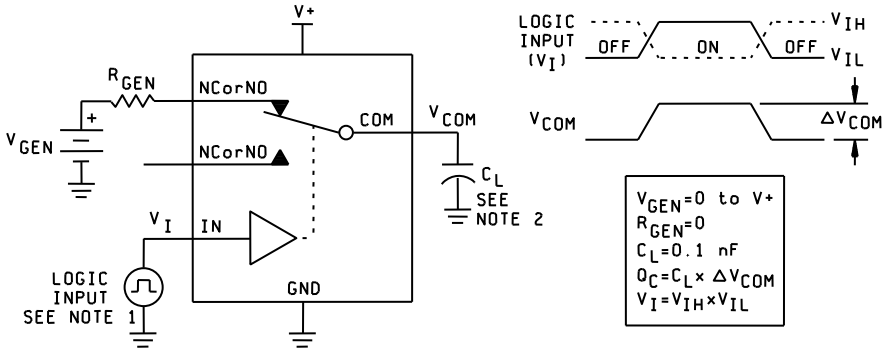
FIGURE 8. Turn on ( $t_{ON}$ ) and turn off time ( $t_{OFF}$ ).




NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.
2. $C_L$ includes probe and jig capacitance.

FIGURE 9. Break before make time ( $t_{BBM}$ ).




NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.
2. $C_L$ includes probe and jig capacitance.

FIGURE 10. Charge injection ( $Q_C$ ).

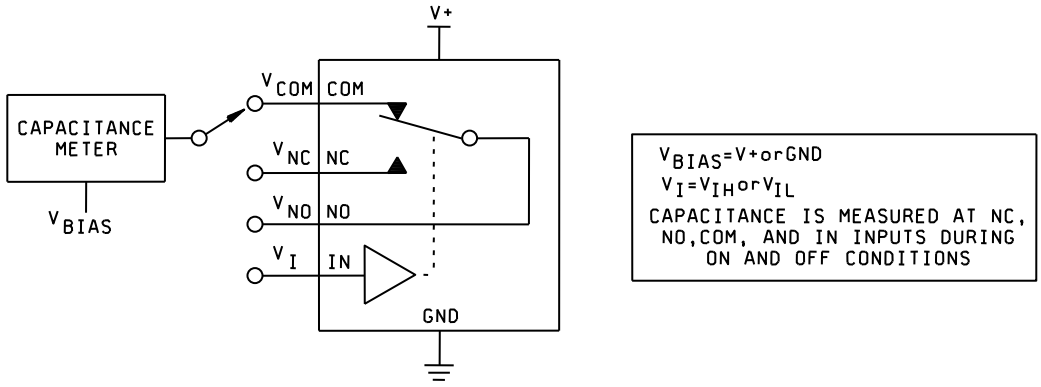



FIGURE 11. Capacitance ( $C_I$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$ ).

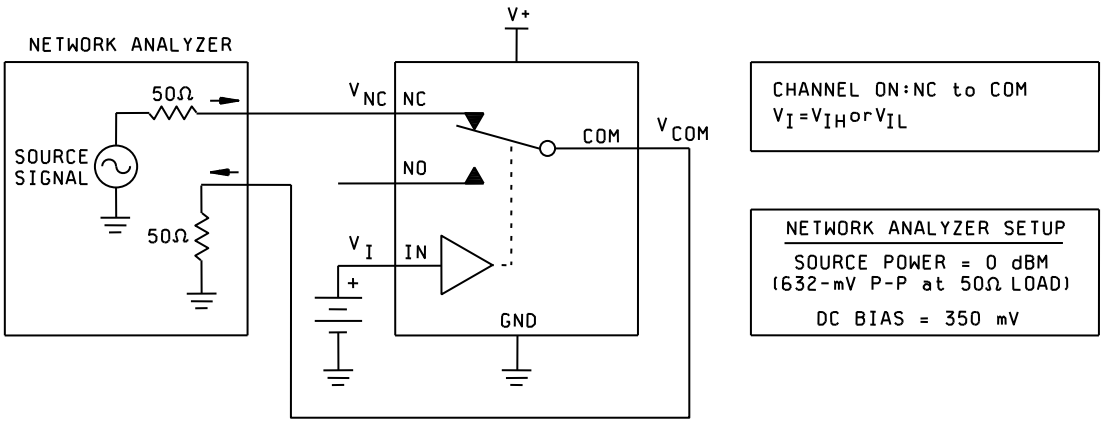



FIGURE 12. Bandwidth ( BW ).

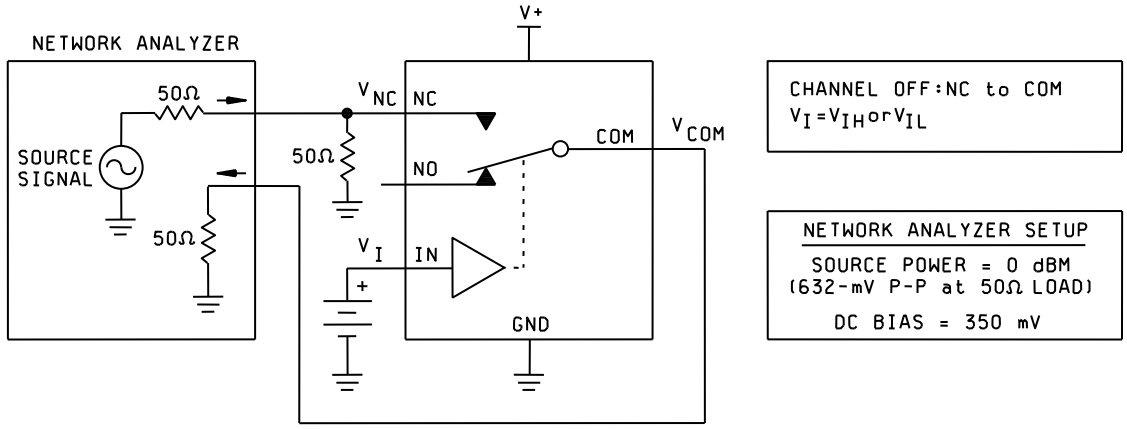



FIGURE 13. OFF isolation ( $O_{ISO}$ ).

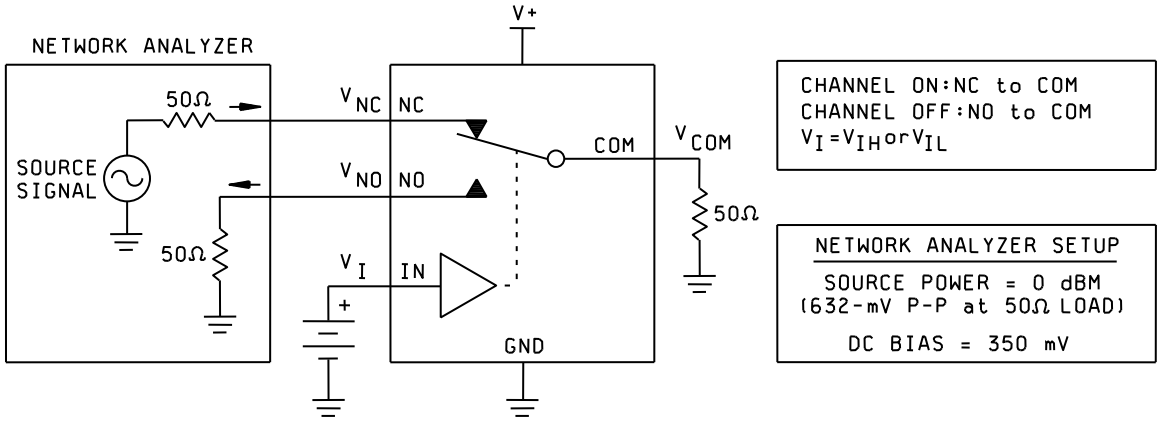
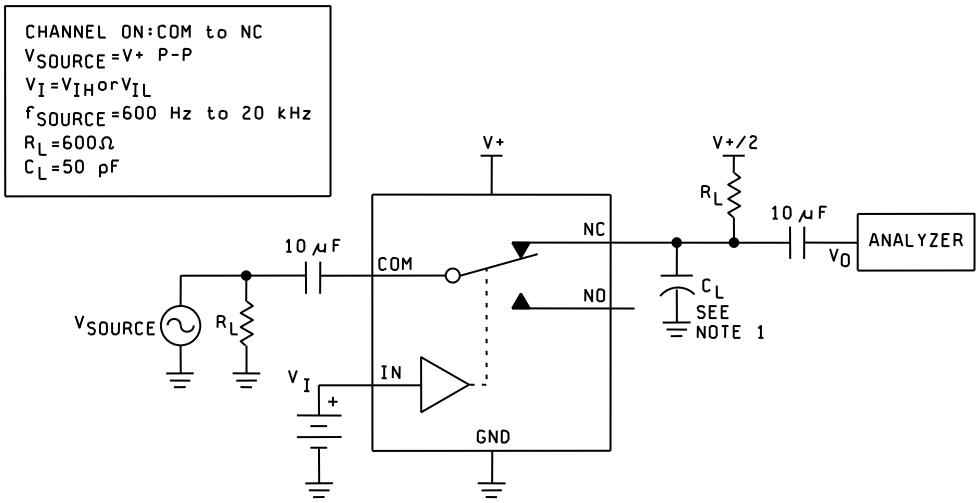



FIGURE 14. Crosstalk ( $X_{TALK}$ ).




NOTE:

1. $C_L$ includes probe and jig capacitance.

FIGURE 15. Total harmonic distortion ( THD ).

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Package 2/ | | Top side marking | Vendor part number |
|---|---|---|---|---|---|
| V62/06613-01XE | 01295 | SOT (SOT-23) - DBV | Tape and reel | JA8R | TS5A3159MDBVREP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available from manufacturer.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243 |