REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	13-12-11	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-05-17	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B									
	PAGE		1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 06-02-15	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/06605**
	REV B	**PAGE** 1 **OF** 10

AMSC N/A

5962-V054-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual positive-edge-triggered D-type flip-flop microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LV74A-EP	Dual positive-edge-triggered D-type flip-flop

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7 V
Input voltage range (V_I) ..... -0.5 V to 7 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Voltage range applied to any output in the high-impedance
or power-off state (V_O) ..... -0.5 V to 7 V 2/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -20 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}) ..... 113°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 2 V to 5.5 V
Minimum high level input voltage (V_{IH}):
V_{CC} = 2 V ..... 1.5 V
V_{CC} = 2.3 V to 2.7 V ..... V_{CC} x 0.7 V
V_{CC} = 3 V to 3.6 V ..... V_{CC} x 0.7 V
V_{CC} = 4.5 V to 5.5 V ..... V_{CC} x 0.7 V
Maximum low level input voltage (V_{IL}):
V_{CC} = 2 V ..... 0.5 V
V_{CC} = 2.3 V to 2.7 V ..... V_{CC} x 0.3 V
V_{CC} = 3 V to 3.6 V ..... V_{CC} x 0.3 V
V_{CC} = 4.5 V to 5.5 V ..... V_{CC} x 0.3 V
Input voltage range (V_I) ..... 0.0 V to 5.5 V
Output voltage range (V_O) ..... 0.0 V to V_{CC}
Maximum high level output current (I_{OH}):
V_{CC} = 2 V ..... -50 μA
V_{CC} = 2.3 V to 2.7 V ..... -2 mA
V_{CC} = 3 V to 3.6 V ..... -6 mA
V_{CC} = 4.5 V to 5.5 V ..... -12 mA
Maximum low level output current (I_{OL}):
V_{CC} = 2 V ..... 50 μA
V_{CC} = 2.3 V to 2.7 V ..... 2 mA
V_{CC} = 3 V to 3.6 V ..... 6 mA
V_{CC} = 4.5 V to 5.5 V ..... 12 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$):
V_{CC} = 2.3 V to 2.7 V ..... 200 ns/V
V_{CC} = 3 V to 3.6 V ..... 100 ns/V
V_{CC} = 4.5 V to 5.5 V ..... 20 ns/V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value is limited to 5.5 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA	2 V to 5.5 V	25°C, -55°C to 125°C	V_{CC} – 0.1		V
		I_{OH} = -2 mA	2.3 V		2		
		I_{OH} = -6 mA	3 V		2.48		
		I_{OH} = -12 mA	4.5 V		3.8		
Low level output voltage	V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
Input current	I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	μA
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	5.5 V			20	μA
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
Off-state current	I_{off}	V_I or V_O = 0 V to 5.5 V	0 V			5	μA
Input capacitance	C_i	V_I = V_{CC} or GND	3.3 V		2 TYP		pF
			5 V		2 TYP		
Power dissipation capacitance	C_{pd}	C_L = 50 pF, f = 10 MHz	3.3 V	25°C	21 TYP		pF
			5 V		23 TYP		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$ 2/	C_L = 50 pF	3.3 V	25°C		0.8	V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$ 2/		3.3 V			-0.8	V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$ 2/		3.3 V		3.2 TYP		V
High-level dynamic input voltage	$V_{IH(D)}$ 2/		3.3 V		2.31		V
Low-level dynamic input voltage	$V_{IL(D)}$ 2/		3.3 V			0.99	V
Pulse duration	t_w	$\overline{PRE}$ or $\overline{CLR}$ low See figure 5.	2.5 V ±0.2 V	25°C	8		ns
				-55°C to 125°C	9		
			3.3 V ±0.3 V	25°C	6		
				-55°C to 125°C	7		
			5 V ±0.5 V	25°C	5		
				-55°C to 125°C	5		
		CLK See figure 5.	2.5 V ±0.2 V	25°C	8		
				-55°C to 125°C	9		
			3.3 V ±0.3 V	25°C	6		
				-55°C to 125°C	7		
			5 V ±0.5 V	25°C	5		
				-55°C to 125°C	5		

See footnotes at end of table.

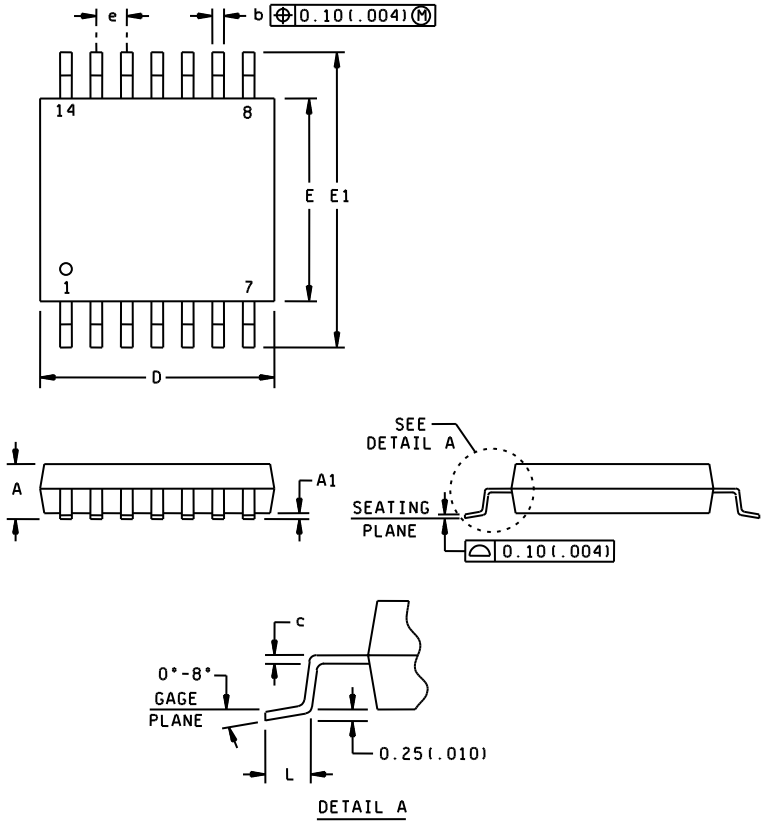
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Limits		Unit
					Min	Max	
Setup time before CLK ↑	t_{su}	Data See figure 5.	2.5 V ±0.2 V	25°C	8		ns
				-55°C to 125°C	9		
			3.3 V ±0.3 V	25°C	6		
				-55°C to 125°C	7		
			5 V ±0.5 V	25°C	5		
				-55°C to 125°C	5		
		$\overline{PRE}$ or $\overline{CLR}$ inactive See figure 5.	2.5 V ±0.2 V	25°C	7		
				-55°C to 125°C	7		
			3.3 V ±0.3 V	25°C	5		
				-55°C to 125°C	5		
			5 V ±0.5 V	25°C	3		
				-55°C to 125°C	3		
Hold time, data after CLK ↑	t_h	See figure 5.	2.5 V ±0.2 V	25°C	0.5		ns
				-55°C to 125°C	0.5		
			3.3 V ±0.3 V	25°C	1.45		
				-55°C to 125°C	2.15		
			5 V ±0.5 V	25°C	1.45		
				-55°C to 125°C	2.15		
Maximum clock frequency	f_{max}	C_L = 50 pF See figure 5.	2.5 V ±0.2 V	25°C	30		MHz
				-55°C to 125°C	25		
			3.3 V ±0.3 V	25°C	50		
				-55°C to 125°C	45		
			5 V ±0.5 V	25°C	90		
				-55°C to 125°C	75		
Propagation delay time, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$	t_{pd}	C_L = 50 pF See figure 5.	2.5 V ±0.2 V	25°C		17.4	ns
				-55°C to 125°C		20	
			3.3 V ±0.3 V	25°C		15.8	
				-55°C to 125°C		18	
			5 V ±0.5 V	25°C		9.7	
				-55°C to 125°C		12	
Propagation delay time, CLK to Q or $\overline{Q}$	t_{pd}	C_L = 50 pF See figure 5.	2.5 V ±0.2 V	25°C		20	ns
				-55°C to 125°C		23	
			3.3 V ±0.3 V	25°C		15.4	
				-55°C to 125°C		18	
			5 V ±0.5 V	25°C		9.9	
				-55°C to 125°C		13	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Characteristics are for surface-mount packages only.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.047	---	1.20	E	0.169	0.177	4.30	4.50
A1	0.002	0.006	0.05	0.15	E1	0.244	0.260	6.20	6.60
b	0.007	0.012	0.19	0.30	e	0.026 BSC		0.65 BSC	
c	0.006 NOM		0.15 NOM		L	0.020	0.030	0.50	0.75
D	0.193	0.201	4.90	5.10					

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 mm (0.006 inches).
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Inputs				Outputs	
PRE	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H 1/	H 1/
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High voltage level
L = Low voltage level
X = Immaterial
↑ = Transition from low to high level.
Q_0 or $\overline{Q}_0$ = Level of Q before the indicated steady-state input conditions were established.

1/ This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

FIGURE 2. Truth table.

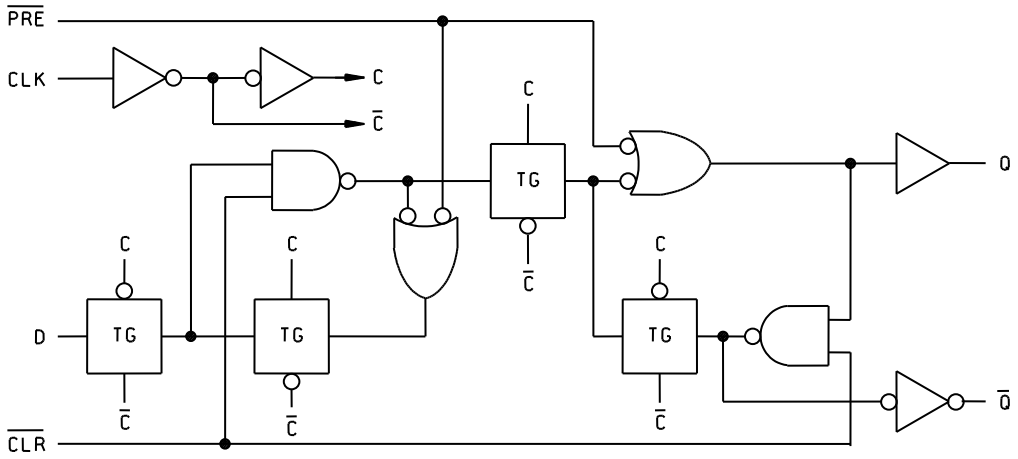
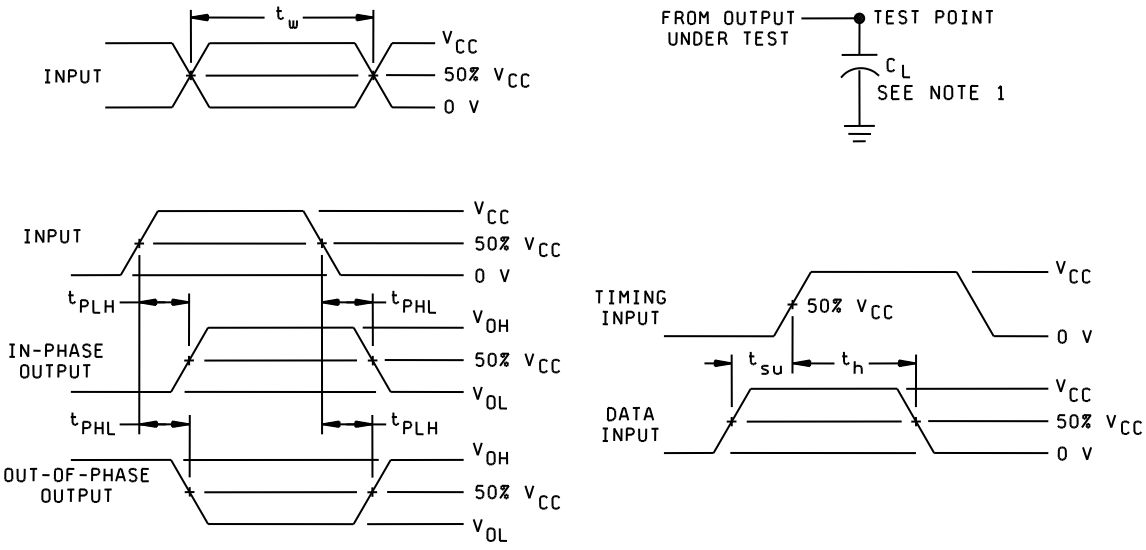


FIGURE 3. Logic diagram.

Device type 01			
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$1\overline{CLR}$	8	$2\overline{Q}$
2	1D	9	2Q
3	1CLK	10	$2\overline{PRE}$
4	$1\overline{PRE}$	11	2CLK
5	1Q	12	2D
6	$1\overline{Q}$	13	$2\overline{CLR}$
7	GND	14	V_{CC}

FIGURE 4. Terminal connections.



NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06605-01XE	01295	SN74LV74AMPWREP	LV74AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243