REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. - PHN	13-10-28	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-05-17	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV	B	B	B	B	B	B	B	B	B	B										
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY MM DD 06-03-09	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M.Hess	**TITLE** MICROCIRCUIT, DIGITAL, OCTAL BUFFER/DRIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/06604**
	REV B	**PAGE** 1 **OF** 10

AMSC N/A

5962-V053-21

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer/driver with three-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/06604	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LV244A-EP	Octal buffer/driver with three-state outputs

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to 7 V 2/
Output voltage range (V_O)	-0.5 V to V_{CC} +0.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Continuous output current (I_O) (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance (θ_{JA})	58°C/W 4/
Storage temperature range (T_{STG})	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value is limited to 5.5 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	2.0 V to 5.5 V
Minimum high level input voltage (V_{IH}):	
V_{CC} = 2 V	1.5 V
V_{CC} = 2.3 V to 2.7 V	V_{CC} x 0.7 V
V_{CC} = 3 V to 3.6 V	V_{CC} x 0.7 V
V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.7 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 2 V	0.5 V
V_{CC} = 2.3 V to 2.7 V	V_{CC} x 0.3 V
V_{CC} = 3 V to 3.6 V	V_{CC} x 0.3 V
V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.3 V
Input voltage (V_I)	0 V to 5.5 V
Output voltage (V_O):	
High or low state	0 V to V_{CC}
Three state	0 V to 5.5 V
Maximum high level output current (I_{OH}):	
V_{CC} = 2 V	-50 μA
V_{CC} = 2.3 V to 2.7 V	-2 mA
V_{CC} = 3 V to 3.6 V	-8 mA
V_{CC} = 4.5 V to 5.5 V	-16 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 2 V	50 μA
V_{CC} = 2.3 V to 2.7 V	2 mA
V_{CC} = 3 V to 3.6 V	8 mA
V_{CC} = 4.5 V to 5.5 V	16 mA
Maximum input transition rise or fall rate ($\Delta t / \Delta v$):	
V_{CC} = 2.3 V to 2.7 V	200 ns/V
V_{CC} = 3 V to 3.6 V	100 ns/V
V_{CC} = 4.5 V to 5.5 V	20 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA	2.0 V to 5.5 V	V_{CC} – 0.1		V
		I_{OH} = -2 mA	2.3 V	2		
		I_{OH} = -8 mA	3.0 V	2.48		
		I_{OH} = -16 mA	4.5 V	3.8		
Low level output voltage	V_{OL}	I_{OL} = 50 μA	2.0 V to 5.5 V		0.1	V
		I_{OL} = 2 mA	2.3 V		0.4	
		I_{OL} = 8 mA	3.0 V		0.44	
		I_{OL} = 16 mA	4.5 V		0.55	
Input current	I_I	V_I = 5.5 V or GND	0 to 5.5 V		±1	μA
Input impedance	I_{OZ}	V_O = V_{CC} or GND	5.5 V		±5	μA
Supply current	I_{CC}	V_I = V_{CC} or GND, I_O = 0,	5.5V		20	μA
Off current	I_{off}	V_I or V_O = 0 to 5.5 V	0		5	μA
Input capacitance	C_i	V_I = V_{CC} or GND	3.3 V	2.3 Typ		pF
Power dissipation capacitance	C_{pd}	C_L = 50 pF, f = 10 MHz, T_A = 25°C	3.3 V	14 Typ		
			5.0 V	16 Typ		
Noise characteristics 2/						
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	C_L = 50 pF, T_A = 25°C	3.3 V	0.55 Typ		V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$			-0.5 Typ		
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$			2.9 Typ		
High level dynamic input voltage	$V_{IH(D)}$			2.31		
Low level dynamic input voltage	$V_{IL(D)}$				0.99	

See footnotes at end of table.

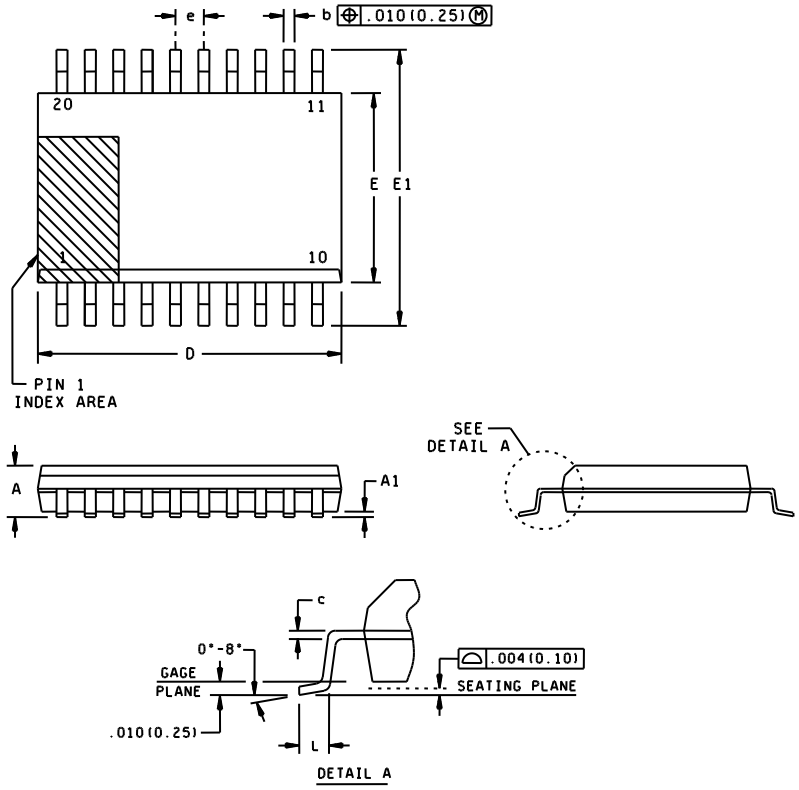
TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions	V_{CC}	T_A = 25°C		-55°C ≤ T_A ≤ 125°C		Unit
				Min	Max	Min	Max	
Switching characteristics								
Propagation delay time, from input A to output Y	t_{pd}	C_L = 50 pF	2.5 V ±0.2 V		15.3	1	18	ns
Enable time from input $\overline{OE}$ to output Y	T_{en}				17.8	1	21	
Disable time from input $\overline{OE}$ to output Y	t_{dis}				19.2	1	21	
Skew time	$t_{sk(o)}$				2		2	
Propagation delay time, from input A to output Y	t_{pd}		3.3 V ±0.3 V		11.9	1	13.5	
Enable time from input $\overline{OE}$ to output Y	T_{en}				14.1	1	16	
Disable time from input $\overline{OE}$ to output Y	t_{dis}				16	1	18	
Skew time	$t_{sk(o)}$				1.5		1.5	
Propagation delay time, from input A to output Y	t_{pd}		5.0 V ±0.5 V		7.5	1	8.5	
Enable time from input $\overline{OE}$ to output Y	T_{en}				9.3	1	10.5	
Disable time from input $\overline{OE}$ to output Y	t_{dis}				14.2	1	15.5	
Skew time	$t_{sk(o)}$				1		1	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Characteristics are for surface mount packages only.

Case X



Dimension									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		2.65		0.104	E	7.40	7.60	0.291	0.299
A1	0.10	0.30	0.004	0.012	E1	9.97	10.63	0.393	0.419
b	0.31	0.51	0.012	0.020	e	1.27 Nom		0.050 Nom	
c	0.20	0.33	0.008	0.013	L	0.40	1.27	0.016	0.050
D	12.60	13.00	0.496	0.512					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches).
3. Falls within JEDEC MS-013 variation AC.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{OE}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2 $\overline{OE}$
10	GND	20	V_{CC}

FIGURE 2. Terminal connections.

(Each Buffer)

Inputs		Output Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

FIGURE 3. Function table.

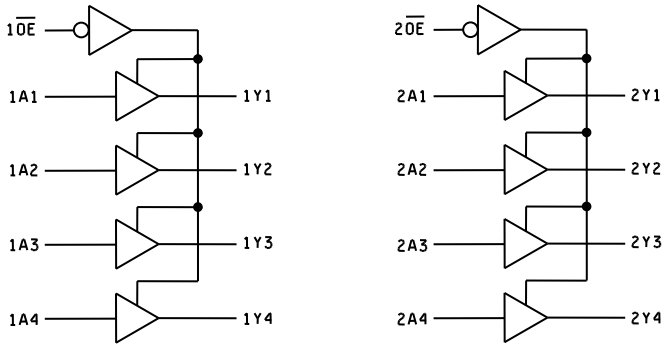
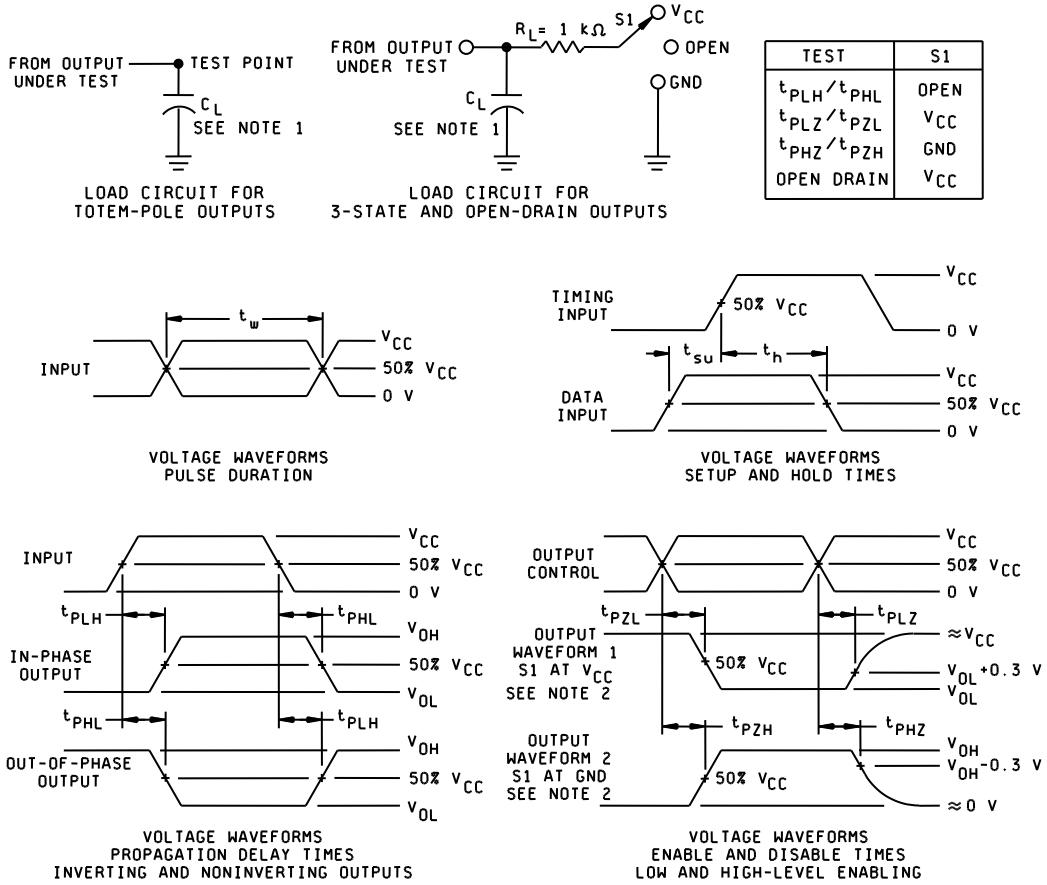


FIGURE 4. Logic diagram.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PHL} and t_{PLH} are the same as t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06604-01XE	01295	SN74LV244AMDWREP	LV244AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243