REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	12-01-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-05-17	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B										
	PAGE	1	2	3	4	5	6	7	8	9	10										

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 05-10-19	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, DUAL 2-INPUT POSITIVE-NAND GATE, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/05623**
	REV B	**PAGE** 1 **OF** 10

AMSC N/A

5962-V051-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual 2-input positive-NAND gate microcircuit, with an operating temperature range of -55°C to +115°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05623	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC2G00W-EP	Dual 2-input positive-NAND gate

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MO-187	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V to +6.5 V
Input voltage range, (V_I)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power-off state, (V_O)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or slow state, (V_O)	-0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current, (I_{IK}) (V_I < 0)	-50 mA
Output clamp current, (I_{OK}) (V_O < 0)	-50 mA
Continuous output current, (I_O)	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance (θ_{JA})	220°C/W 4/
Storage temperature range, (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage, (V_{CC}):	
Operating range	+1.65 V to +5.5 V
Minimum data retention only	+1.5 V
Minimum high level input voltage, (V_{IH}):	
V_{CC} = 1.65 V to 1.95 V	+0.65 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	+1.7 V
V_{CC} = 3 V to 3.6 V	+2 V
V_{CC} = 4.5 V to 5.5 V	+0.7 x V_{CC}
Maximum low level input voltage, (V_{IL}):	
V_{CC} = 1.65 V to 1.95 V	+0.35 x V_{CC}
V_{CC} = 2.3 V to 2.7 V	+0.7 V
V_{CC} = 3 V to 3.6 V	+0.8 V
V_{CC} = 4.5 V to 5.5 V	+0.3 x V_{CC}
Input voltage range, (V_I)	0 V to 5.5 V
Output voltage range, (V_O)	0 V to V_{CC}
Maximum high level output current, (I_{OH}):	
V_{CC} = 1.65 V	-4 mA
V_{CC} = 2.3 V	-8 mA
V_{CC} = 3 V	-16 mA
V_{CC} = 3 V	-24 mA
V_{CC} = 4.5 V	-32 mA
Maximum low level output current, (I_{OL}):	
V_{CC} = 1.65 V	4 mA
V_{CC} = 2.3 V	8 mA
V_{CC} = 3 V	16 mA
V_{CC} = 3 V	24 mA
V_{CC} = 4.5 V	32 mA
Maximum Input transition rise or fall rate ($\Delta t/\Delta v$):	
V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20 ns/V
V_{CC} = 3.3 V ± 0.3 V	10 ns/V
V_{CC} = 5 V ± 0.5 V	5 ns/V
Operating free air temperature, (T_A)	-55°C to +115°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may exceeded if the input and output clamp-current ratings are observed.
3/ The value of V_{CC} is provided in recommended operating conditions.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

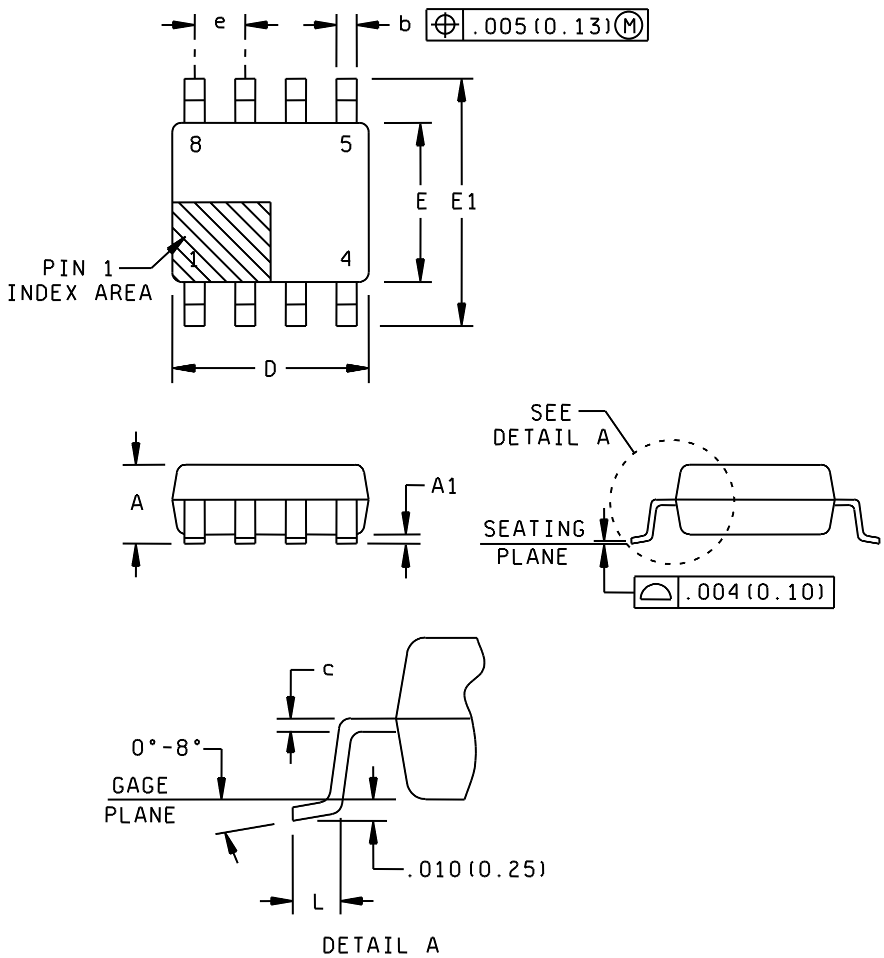
3.5.5 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \leq T_A \leq +115°C$ unless otherwise specified		V_{CC}	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}		I_{OH} = -100 µA	1.65 V to 5.5 V	V_{CC} – 0.1		V
			I_{OH} = -4 mA	1.65 V	1.2		
			I_{OH} = -8 mA	2.3 V	1.9		
			I_{OH} = -16 mA	3 V	2.4		
			I_{OH} = -24 mA		2.3		
			I_{OH} = -32 mA	4.5 V	3.8		
Low level output voltage	V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V		0.1	
			I_{OL} = 4 mA	1.65 V		0.45	
			I_{OL} = 8 mA	2.3 V		0.3	
			I_{OL} = 16 mA	3 V		0.4	
			I_{OL} = 24 mA			0.55	
			I_{OL} = 32 mA	4.5 V		0.57	
Input current, A or B inputs	I_I	V_I = 5.5 V or GND		0 to 5.5 V		±5	µA
Input/output power off leakage current	I_{off}	V_I or V_O = 5.5 V		0 V		±10	µA
Quiescent supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0		1.65 V to 5.5 V		10	µA
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 5.5 V		500	µA
Input capacitance	C_i	V_I = V_{CC} or GND, T_A = 25°C		3.3 V	5 Typ		pF
Propagation delay time, from input A or B to output Y	t_{pd}	See figure 5.		1.8 V ±0.15 V	3.7	8.9	ns
				2.5 V ±0.2 V	1.6	5.8	
				3.3 V ±0.3 V	1.1	5.3	
				5 V ±0.5 V	1	4.3	
Power dissipation capacitance	C_{pd}	T_A = 25°C f = 10 MHz		1.8 V	19 Typ		pF
				2.5 V	19 Typ		
				3.3 V	20 Typ		
				5.0 V	22 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. Falls within JEDEC MO-187 variation DA.

FIGURE 1. Case outline.

Case X

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	---	1.30	---	0.051
A1	0.00	0.10	0.000	0.004
b	0.15	0.30	0.006	0.012
c	0.15 NOM		0.006 NOM	
D	2.75	3.15	0.108	0.124
E	2.70	2.90	0.106	0.114
E1	3.75	4.25	0.148	0.167
e	0.65 BSC		0.026 BSC	
L	0.20	0.60	0.008	0.024

FIGURE 1. Case outline - Continued.

Case outline:	X
Terminal number	Terminal name
1	1A
2	1B
3	2Y
4	GND
5	2A
6	2B
7	1Y
8	V_{CC}

FIGURE 2. Terminal connections.

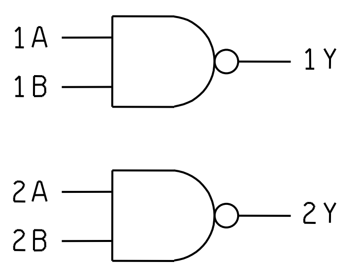
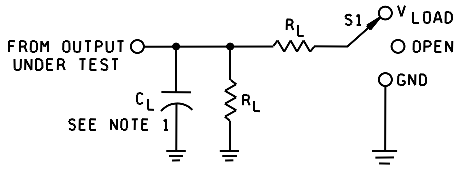


FIGURE 3. Logic diagram.

(Each gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

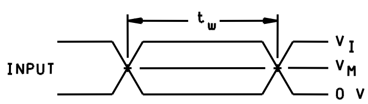
FIGURE 4. Function Table



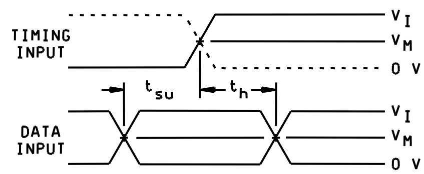
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

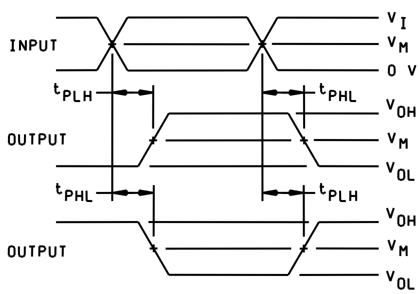
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500Ω	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500Ω	0.3 V



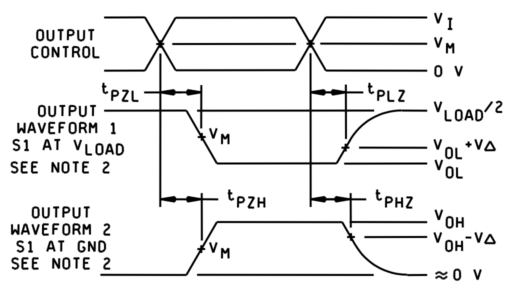
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

Notes:
1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and switching waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-side marking 2/
V62/05623-01XE	01295	SN74LVC2G00WDCTREP	C00_ _ _

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243