

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Changes were made to the following tests under Table I; quiescent current, hysteresis voltage, Internally set-free running frequency range, externally set-free running frequency range, input bias current, VSENSE pin, internal slow start time, charge current, SS/ENA pin, discharge current, SS/ENA pin, output saturation voltage PWRGD pin, leakage current PWRGD, current limit trip point, and power MOSFET switches. Changes were also made to footnote 7/ under Table I, note under figure 1, and BOOT description under figure 2. Updating document to current requirements. - ro	10-11-08	C. SAFFLE
B	Make change to Discharge current, SS/ENA pin test conditions column SS/ENA limit as specified under Table I. Update document paragraphs to current requirements. - ro	16-10-04	C. SAFFLE



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990																		
Original date of drawing YY-MM-DD 05-10-05	CHECKED BY TOM HESS	TITLE MICROCIRCUIT, DIGITAL-LINEAR, 3 V to 6 V INPUT, 6 A OUTPUT SYNCHRONOUS PULSE WIDTH MODULATOR, MONOLITHIC SILICON																		
	APPROVED BY RAYMOND MONNIN																			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/05622																	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3 V to 6 V input, 6 A output synchronous pulse width modulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/05622</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>	<u>Output voltage</u>
01	TPS54610-EP	3 V to 6 V input, 6 A output synchronous pulse width modulator	Adjustable down to 0.9 V

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	28	MO-153	Plastic small outline package with a thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage range (VI):	
VIN, SS/ENA, FSEL pins	-0.3 V to 7 V
RT pin	-0.3 V to 6 V
VSENSE pin	-0.3 V to 4 V
BOOT pin	-0.3 V to 17 V
Output voltage range (VO):	
VBIAS, COMP, PWRGD pins	-0.3 V to 7 V
PH pin	-0.6 V to 10 V
Source current (IO):	
PH pin	Internally limited
COMP, VBIAS pin	6 mA
Sink current (IS):	
PH pin	12 A
COMP pin	6 mA
SS/ENA, PWRGD pins	10 mA
Voltage differential (AGND to PGND pins)	±0.3 V
Operating virtual junction temperature range (TJ)	-55°C to +150°C
Storage temperature range (TSTG)	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	300°C

1.4 Recommended operating conditions. 2/

Input voltage range (VI)	3 V to 6 V
Operating virtual junction temperature range (TJ)	-55°C to +125°C

1.5. Power dissipation rating table. 3/ 4/

Package	Thermal impedance junction-to-ambient	TA = 25°C power rating	TA = 70°C power rating	TA = 85°C power rating
Case X with solder	18.2°C/W	5.49 W 5/	3.02 W	2.2 W
Case X without solder	40.5°C/W	2.48 W	1.36 W	0.99 W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 3/ For more information on the case X (PWP) package, see the manufacturer’s technical brief SLMA002.
- 4/ Test board conditions:
- 3 inch x 3 inch, 4 layers, thickness: 0.062 inch.
 - 1.5 ounce copper traces located on the top of the printed circuit board (PCB).
 - 1.5 ounce copper ground plane on the bottom of the printed circuit board (PCB).
 - 0.5 ounce copper ground planes on the 2 internal layers.
 - 12 thermal vias (see recommended land pattern section in the applications section of the data sheet).
- 5/ Maximum power dissipation may be limited by over current protection.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Test circuit. The test circuit shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Supply voltage (V _{IN}) section							
Input voltage range	V _{IN}		-55°C to +125°C	01	3	6	V
Quiescent current	I(Q)	f _S = 350 kHz, FSEL ≤ 0.8 V, RT open, phase pin open	-55°C to +125°C	01		19	mA
		f _S = 550 kHz, FSEL ≥ 2.5 V, RT open, phase pin open				25	
		Shutdown, SS/ENA = 0 V				1.4	
Under voltage lock out (UVLO) section							
Start threshold voltage			-55°C to +125°C	01		3	V
Stop threshold voltage			-55°C to +125°C	01	2.7		V
Hysteresis voltage			-55°C to +125°C	01	0.12		V
Rising and falling <u>3/</u> edge deglitch			-55°C to +125°C	01	2.5 typical		μs
Bias voltage (VBIAS) section							
Output voltage		I(VBIAS) = 0	-55°C to +125°C	01	2.7	2.95	V
Output current <u>4/</u>			-55°C to +125°C	01		100	μA
Cumulative reference section							
Accuracy <u>3/</u>	VREF		-55°C to +125°C	01	0.882	0.9	V
Regulation section							
Line regulation <u>3/ 5/</u>		I _L = 3 A, f _S = 350 kHz	+125°C	01		0.07	%V
		I _L = 3 A, f _S = 550 kHz	+125°C			0.07	
Load regulation <u>3/ 5/</u>		I _L = 0 A to 6 A, f _S = 350 kHz	+125°C	01		0.03	%A
		I _L = 0 A to 6 A, f _S = 550 kHz	+125°C			0.03	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Oscillator section							
Internally set – free running frequency		FSEL ≤ 0.8 V, RT open	-55°C to +125°C	01	270	425	kHz
		FSEL ≥ 2.5 V, RT open			415	662	
Externally set – free running frequency range		RT = 180 kΩ (1 % resistor to AGND) <u>3/</u>	-55°C to +125°C	01	245	315	kHz
		RT = 160 kΩ (1 % resistor to AGND)			285	360	
		RT = 68 kΩ (1 % resistor to AGND) <u>3/</u>			655	773	
High level threshold, FSEL pin			-55°C to +125°C	01	2.5		V
Low level threshold, FSEL pin			-55°C to +125°C	01		0.8	V
Pulse duration, external synchronization, FSEL pin		<u>3/</u>	-55°C to +125°C	01	50		ns
Frequency range, FSEL pin		<u>3/ 6/</u>	-55°C to +125°C	01	330	700	kHz
Ramp valley <u>3/</u>			-55°C to +125°C	01	0.75 typical		V
Ramp amplitude (peak to peak)		<u>3/</u>	-55°C to +125°C	01	1 typical		V
Minimum controllable on time		<u>3/</u>	-55°C to +125°C	01		200	ns
Maximum duty cycle		<u>3/</u>	-55°C to +125°C	01	90%		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Error amplifier section							
Error amplifier open loop voltage gain		1 kΩ COMP to AGND <u>3/</u>	-55°C to +125°C	01	90		dB
Error amplifier unity gain bandwidth		Parallel 10 kΩ, <u>3/</u> 160 pF COMP to AGND	-55°C to +125°C	01	3		MHz
Error amplifier common mode input voltage range		Powered by internal low drop out (LDO) regulator <u>3/</u>	-55°C to +125°C	01	0	VBIAS	V
Input bias current, VSENSE pin		VSENSE = VREF <u>3/</u>	-55°C to +125°C	01	60 typical		nA
Output voltage slew rate (symmetric), COMP		<u>3/</u>	-55°C to +125°C	01	1		V/μs
PWM comparator section							
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)		10 mV overdrive <u>3/</u>	-55°C to +125°C	01		85	ns
Slow start / enable section							
Enable threshold voltage, SS/ENA pin			-55°C to +125°C	01	0.82	1.4	V
Enable hysteresis voltage, SS/ENA pin			-55°C to +125°C	01	0.03 typical		V
Falling edge deglitch, SS/ENA pin		<u>3/</u>	-55°C to +125°C	01	2.5 typical		μs
Internal slow start time		<u>3/</u>	-55°C to +125°C	01	2	4.5	ms
Charge current, SS/ENA pin		SS/ENA = 0 V	-55°C to +125°C	01	2.5	8	μA
Discharge current, SS/ENA pin		SS/ENA = 1.2 V, V _I = 2.7 V	-55°C to +125°C	01	1.1	4	mA
Power good section							
Power good threshold voltage		VSENSE falling	-55°C to +125°C	01	90 typical		%VREF
Power good hysteresis voltage		<u>3/</u>	-55°C to +125°C	01	3 typical		%VREF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Power good section - Continued							
Power good falling edge deglitch		<u>3/</u>	-55°C to +125°C	01	35 typical		μs
Output saturation voltage, PWRGD pin		I(sink) = 2.5 mA	-55°C to +125°C	01		0.31	V
Leakage current, PWRGD pin		V _I = 5.5 V	-55°C to +125°C	01	100 typical		nA
Current limit section							
Current limit trip point		V _I = 3 V <u>3/</u>	-55°C to +125°C	01	10 typical		A
		V _I = 6 V <u>3/</u>			12 typical		
Current limit leading edge blanking time		<u>3/</u>	-55°C to +125°C	01	100 typical		ns
Current limit total response time		<u>3/</u>	-55°C to +125°C	01	200 typical		ns
Thermal shutdown section							
Thermal shutdown trip point		<u>3/</u>	-55°C to +125°C	All	135	165	°C
Thermal shutdown hysteresis		<u>3/</u>	-55°C to +125°C	All	10 typical		°C
Output power MOSFETs - section							
Power MOSFET switches	r _{DS(on)}	V _I = 6 V <u>7/</u>	-55°C to +125°C	All		51	mΩ
		V _I = 3 V <u>7/</u>				67	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, T_J = -55°C to +125°C and V_I = 3 V to 6 V.
- 3/ Specified by design.
- 4/ Static resistive loads only.
- 5/ Tested using circuit in figure 4.
- 6/ To ensure proper operation when the RC filter is used between the external clock and the FSEL pin, the recommended values are R ≤ 1 kΩ and C ≤ 120 pF.
- 7/ Matched metal oxide semiconductor field effect transistors (MOSFETs), low side r_{DS(on)} production tested, high side r_{DS(on)} specified by design.

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Case X

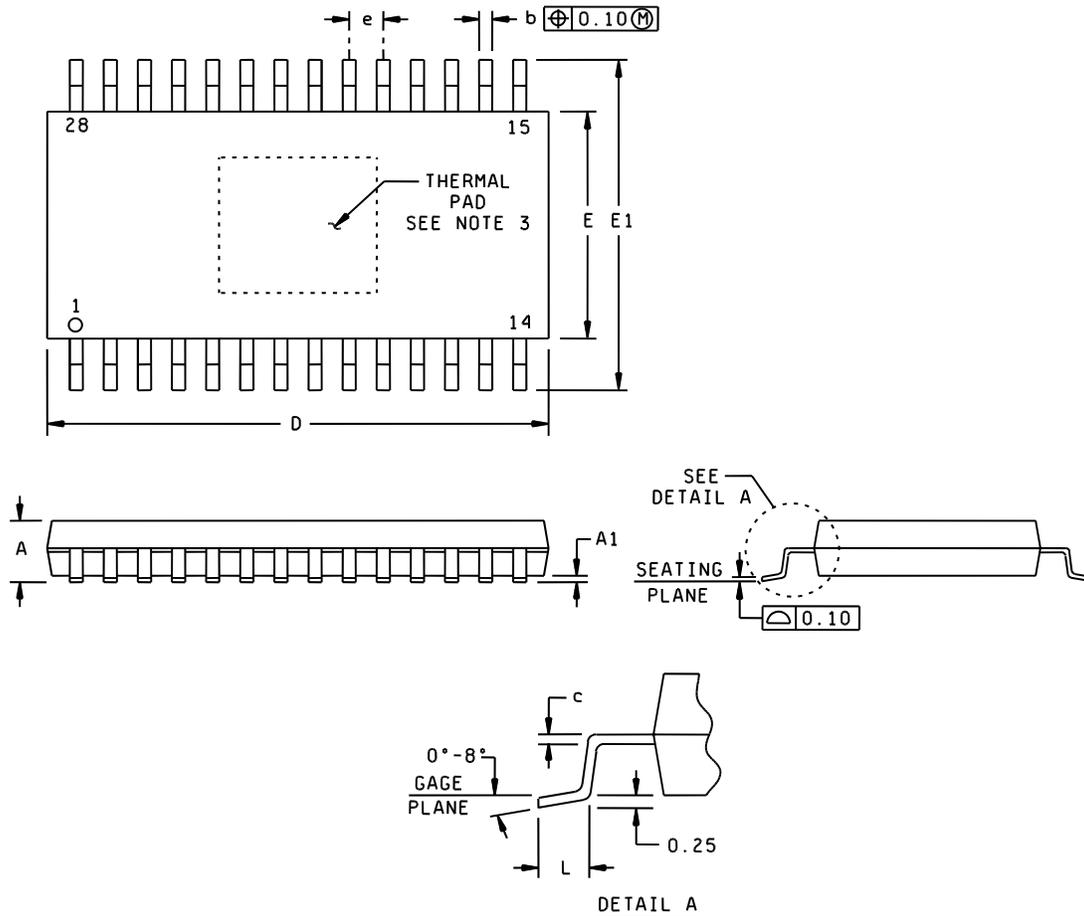


FIGURE 1. Case outline .

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.001	0.005	0.05	0.15
b	0.007	0.011	0.19	0.30
c	0.005 nominal		0.15 nominal	
D	0.377	0.385	9.60	9.80
e	0.025 BSC		0.65 BSC	
E	0.169	0.177	4.30	4.50
E1	0.244	0.259	6.20	6.60
L	0.019	0.029	0.50	0.75
n	28 leads		28 leads	

NOTE:

1. Controlling dimensions are in millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 inch) per side.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline – Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	AGND
2	VSENSE
3	COMP
4	PWRGD
5	BOOT
6	PH
7	PH
8	PH
9	PH
10	PH
11	PH
12	PH
13	PH
14	PH
15	PGND
16	PGND
17	PGND
18	PGND
19	PGND
20	VIN
21	VIN
22	VIN
23	VIN
24	VIN
25	VBIAS
26	SS / ENA
27	FSEL
28	RT

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05622
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Terminal symbol	Description
AGND	Analog ground. Return for compensation network / output divider, slow-start capacitor, VBIAS capacitor, RT resistor and FSEL pin. Make thermal pad connection to AGND.
BOOT	Bootstrap output. A 0.022 μ F to 0.1 μ F low equivalent series resistance (ESR) capacitor connected from BOOT to PH generates a floating drive for the high side field effect transistor (FET) driver.
COMP	Error amplifier output. Connect frequency compensation network from COMP to VSENSE.
PGND	Power ground. High current return for the low side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	Phase output. Junction of the internal high side and low side power MOSFETs and output inductor.
PWRGD	Power good open drain output. High when VSENSE \geq 90% V_{ref} , otherwise PWRGD is low. Note that output is low when SS / ENA is low or internal shutdown signal is active.
RT	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the FSEL pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency.
SS / ENA	Slow start / enable input / output. Dual function pin which provides logic input to enable / disable device operation and capacitor input to externally set the start up time.
FSEL	Synchronization input. A dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin AGND pin with a high quality, low equivalent series resistance (ESR) 0.1 μ F to 1 μ F ceramic capacitor.
VIN	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with high quality, low equivalent series resistance (ESR) 10 μ F ceramic capacitor.
VSENSE	Error amplifier inverting input. Connect to output voltage through compensation network / output divider.

FIGURE 2. Terminal connections – Continued.

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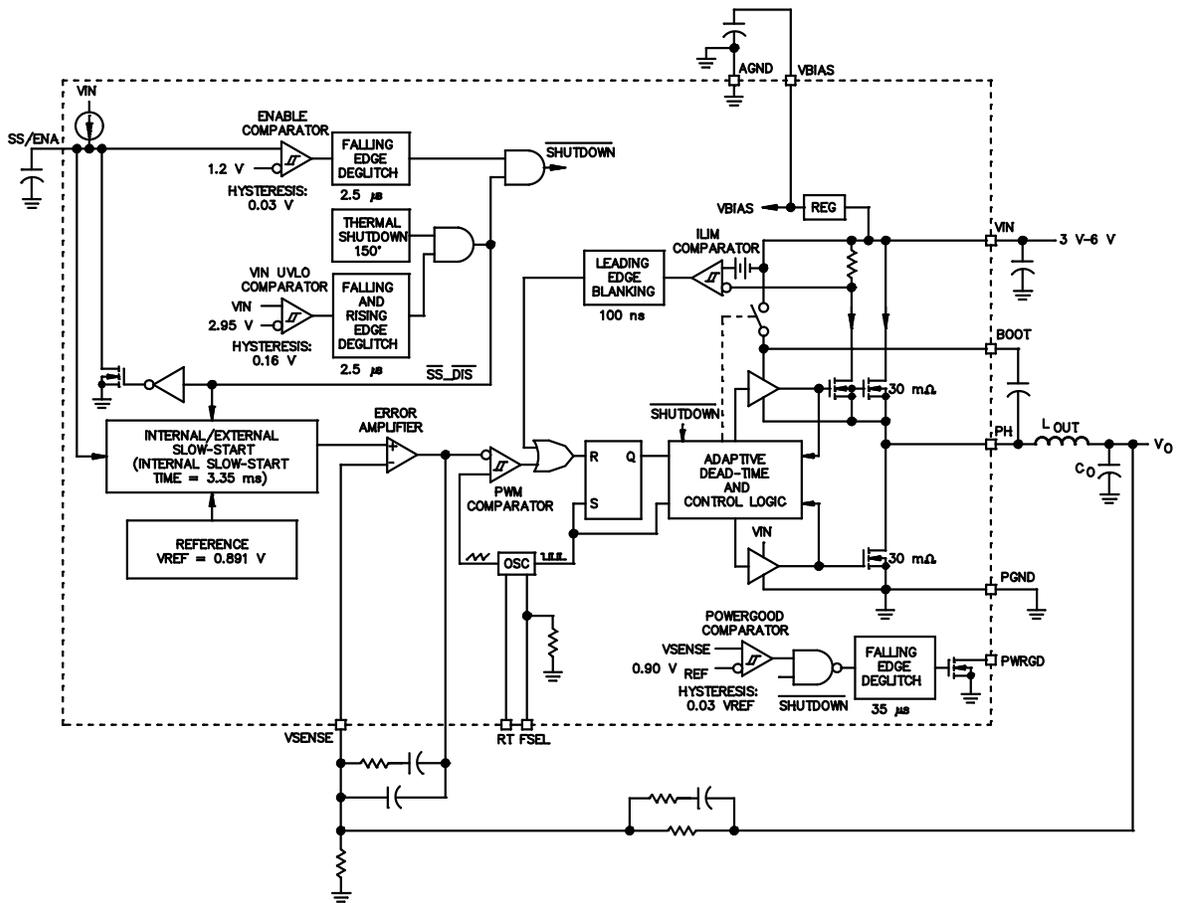


FIGURE 3. Logic diagram.

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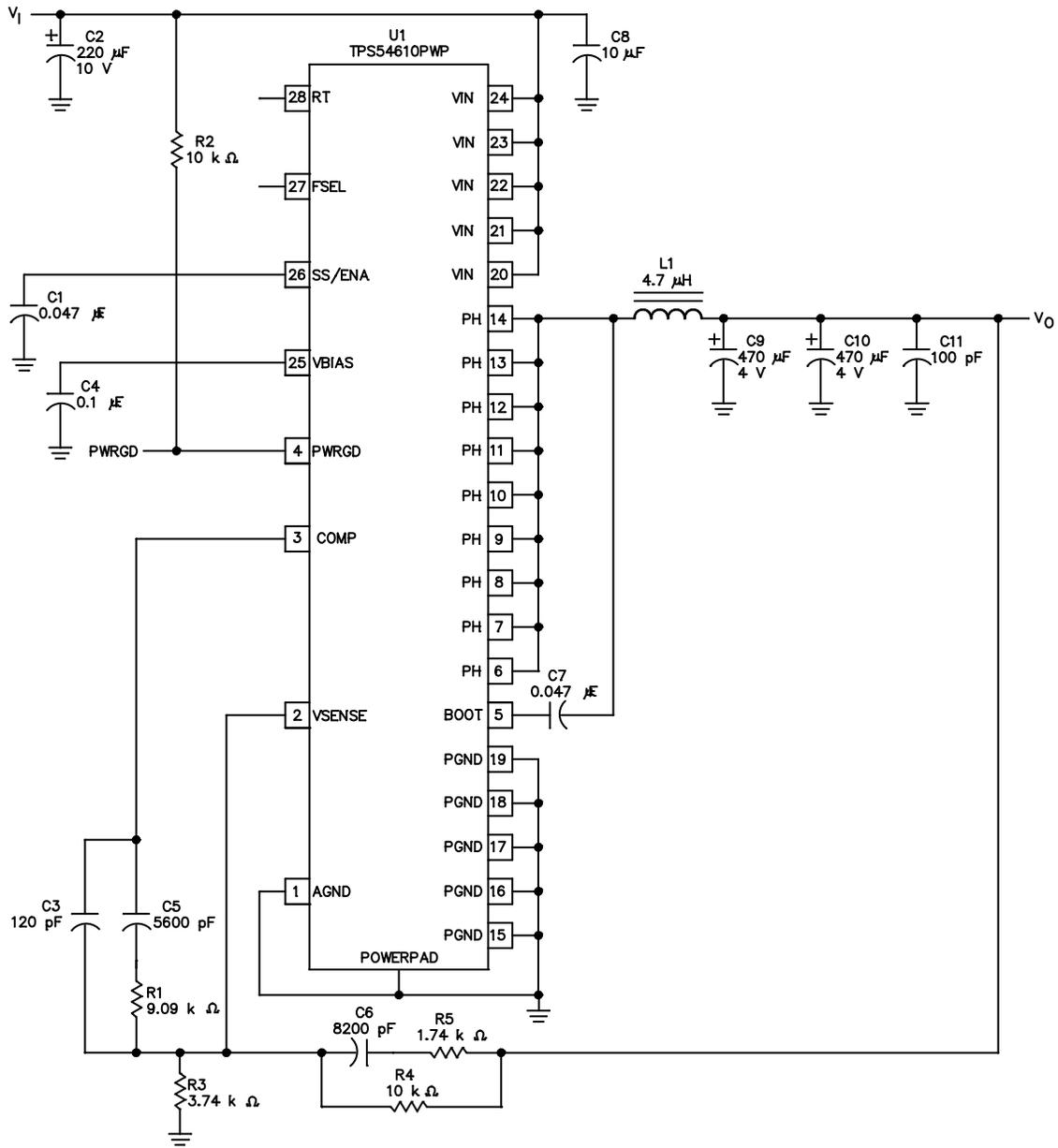


FIGURE 4. Test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Output voltage	Package <u>2/</u>	Vendor part number
V62/05622-01XE	01295	Adjustable down to 0.9 V	Plastic HTSSOP (PWP)	TPS54610MPWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ The package is taped and reeled as indicated by the R suffix on the device type (for example, TPS54610MPWPREP). See the application section of the vendor data sheet for the drawing and layout information.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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