

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single positive-edge-triggered D-type flip-flop microcircuit, with an operating temperature range of -55°C to +115°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/05621</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC1G79-EP	Single positive-edge-triggered D-type flip-flop

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	JEDEC MO-203	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range, (V _{CC})	-0.5 V to +6.5 V
Input voltage range, (V _I)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power-off state, (V _O)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or slow state, (V _O)	-0.5 V to V _{CC} + 0.5 V 2/ 3/
Input clamp current, (I _{IK}) (V _I < 0)	-50 mA
Output clamp current, (I _{OK}) (V _O < 0)	-50 mA
Continuous output current, (I _O)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance (θ _{JA})	252°C/W 4/
Storage temperature range, (T _{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage, (V _{CC}):	
Minimum operating	+1.65 V
Minimum data retention only	+1.5 V
Minimum high level input voltage, (V _{IH}):	
V _{CC} = 1.65 V to 1.95 V	+0.65 x V _{CC}
V _{CC} = 2.3 V to 2.7 V	+1.7 V
V _{CC} = 3 V to 3.6 V	+2 V
V _{CC} = 4.5 V to 5.5 V	+0.7 x V _{CC}
Maximum low level input voltage, (V _{IL}):	
V _{CC} = 1.65 V to 1.95 V	+0.35 x V _{CC}
V _{CC} = 2.3 V to 2.7 V	+0.7 V
V _{CC} = 3 V to 3.6 V	+0.8 V
V _{CC} = 4.5 V to 5.5 V	+0.3 x V _{CC}
Input voltage range, (V _I)	0 V to 5.5 V
Output voltage range, (V _O)	0 V to V _{CC}
Maximum high level output current, (I _{OH}):	
V _{CC} = 1.65 V	-4 mA
V _{CC} = 2.3 V	-8 mA
V _{CC} = 3 V	-16 mA
V _{CC} = 3 V	-24 mA
V _{CC} = 4.5 V	-32 mA
Maximum low level output current, (I _{OL}):	
V _{CC} = 1.65 V	4 mA
V _{CC} = 2.3 V	8 mA
V _{CC} = 3 V	16 mA
V _{CC} = 3 V	24 mA
V _{CC} = 4.5 V	32 mA
Maximum Input transition rise or fall rate (Δt/Δv):	
V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20 ns/V
V _{CC} = 3.3 V ± 0.3 V	10 ns/V
V _{CC} = 5 V ± 0.5 V	5 ns/V
Operating free air temperature, (T _A)	-55°C to +115°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.

3/ The value of V_{CC} is provided in recommended operating conditions.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -55°C ≤ T _A ≤ +115°C unless otherwise specified	V _{CC}	Limits		Unit
				Min	Max	
High level output voltage	V _{OH}		I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1	V
			I _{OH} = -4 mA	1.65 V	1.2	
			I _{OH} = -8 mA	2.3 V	1.9	
			I _{OH} = -16 mA	3 V	2.4	
			I _{OH} = -24 mA		2.3	
			I _{OH} = -32 mA	4.5 V	3.8	
Low level output voltage	V _{OL}		I _{OL} = 100 μA	1.65 V to 5.5 V	0.1	
			I _{OL} = 4 mA	1.65 V	0.45	
			I _{OL} = 8 mA	2.3 V	0.3	
			I _{OL} = 16 mA	3 V	0.4	
			I _{OL} = 24 mA		0.55	
			I _{OL} = 32 mA	4.5 V	0.55	
Input current, CLK or D inputs	I _I	V _I = 5.5 V or GND	0 to 5.5 V		±10	μA
Input/output power off leakage current	I _{off}	V _I or V _O = 5.5 V	0 V		±10	μA
Quiescent supply current	I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	μA
Quiescent supply current delta	ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μA
Input capacitance	C _i	V _I = V _{CC} or GND, T _A = 25°C	3.3 V	4 Typ		pF
Clock frequency	f _{clock}	See figure 5.	1.8 V ±0.15 V		160	MHz
			2.5 V ±0.2 V		160	
			3.3 V ±0.3 V		160	
			5 V ±0.5 V		160	
Pulse duration, CLK high or low	t _w	See figure 5.	1.8 V ±0.15 V	2.5		ns
			2.5 V ±0.2 V	2.5		
			3.3 V ±0.3 V	2.5		
			5 V ±0.5 V	2.5		
Setup time, before CLK ↑	t _{su}	Data high See figure 5.	1.8 V ±0.15 V	2.2		ns
			2.5 V ±0.2 V	1.4		
			3.3 V ±0.3 V	1.3		
			5 V ±0.5 V	1.2		
		Data low See figure 5.	1.8 V ±0.15 V	2.6		
			2.5 V ±0.2 V	1.4		
			3.3 V ±0.3 V	1.3		
			5 V ±0.5 V	1.2		

See footnotes at end of table.

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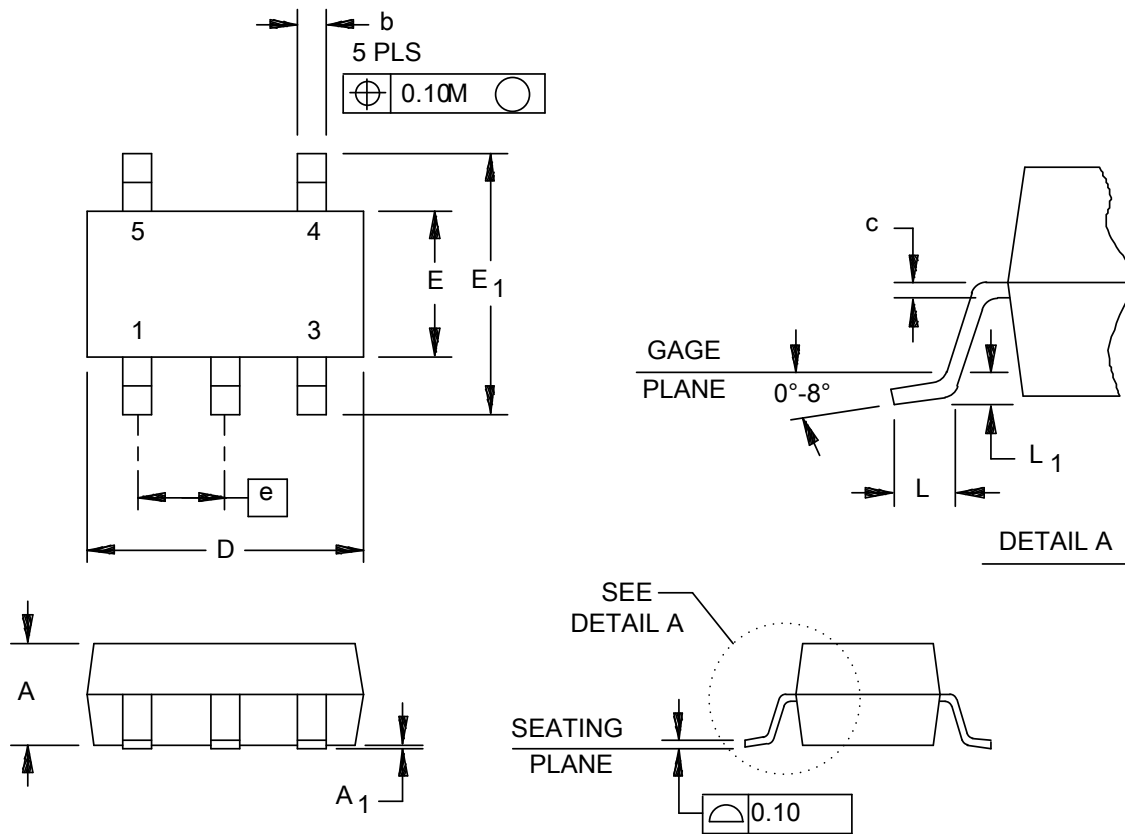
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C ≤ T _A ≤ +115°C unless otherwise specified	V _{CC}	Limits		Unit
				Min	Max	
Hold time, data after CLK ↑	t _h	See figure 5.	1.8 V ±0.15 V	0.3		ns
			2.5 V ±0.2 V	0.4		
			3.3 V ±0.3 V	1		
			5 V ±0.5 V	0.5		
Maximum frequency	f _{max}	See figure 5.	1.8 V ±0.15 V	160		MHz
			2.5 V ±0.2 V	160		
			3.3 V ±0.3 V	160		
			5 V ±0.5 V	160		
Propagation delay time, from input CLK to output Q	t _{pd}	See figure 5.	1.8 V ±0.15 V	3.9	10.1	ns
			2.5 V ±0.2 V	2	7	
			3.3 V ±0.3 V	1.7	5	
			5 V ±0.5 V	1	4.5	
Power dissipation capacitance	C _{pd}	T _A = 25°C f = 10 MHz	1.8 V	26 Typ		pF
			2.5 V	26 Typ		
			3.3 V	27 Typ		
			5.0 V	30 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.031	.043	0.80	1.10	E	.043	.055	1.10	1.40
A1	.000	.004	0.00	0.10	E1	.070	.094	1.80	2.40
b	.006	.012	0.15	0.30	e	.025 BSC		0.65 BSC	
c	.005 NOM		0.13 NOM		L	.010	.018	0.26	0.46
D	.072	.084	1.85	2.15	L1	.006 TYP		0.15 TYP	

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. Falls within JEDEC MO-203.

FIGURE 1. Case outline.

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Case outline:	X
Terminal number	Terminal name
1	D
2	CLK
3	GND
4	Q
5	V _{CC}

FIGURE 2. Terminal connections.

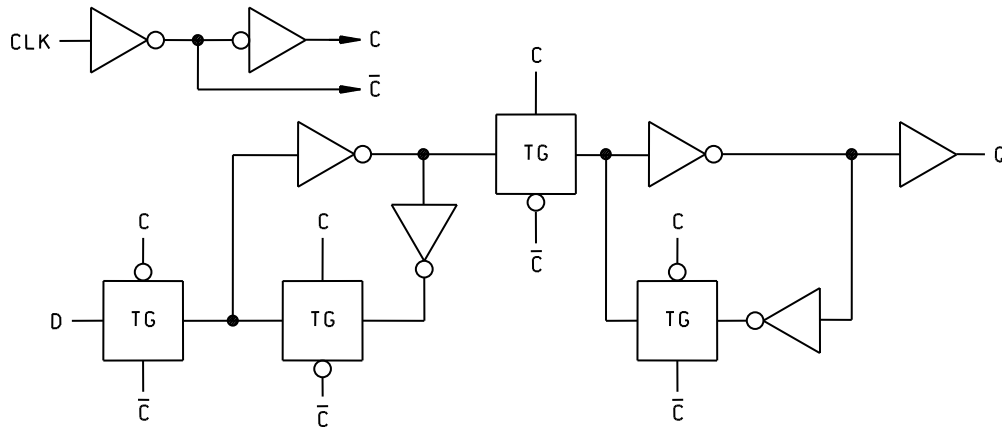
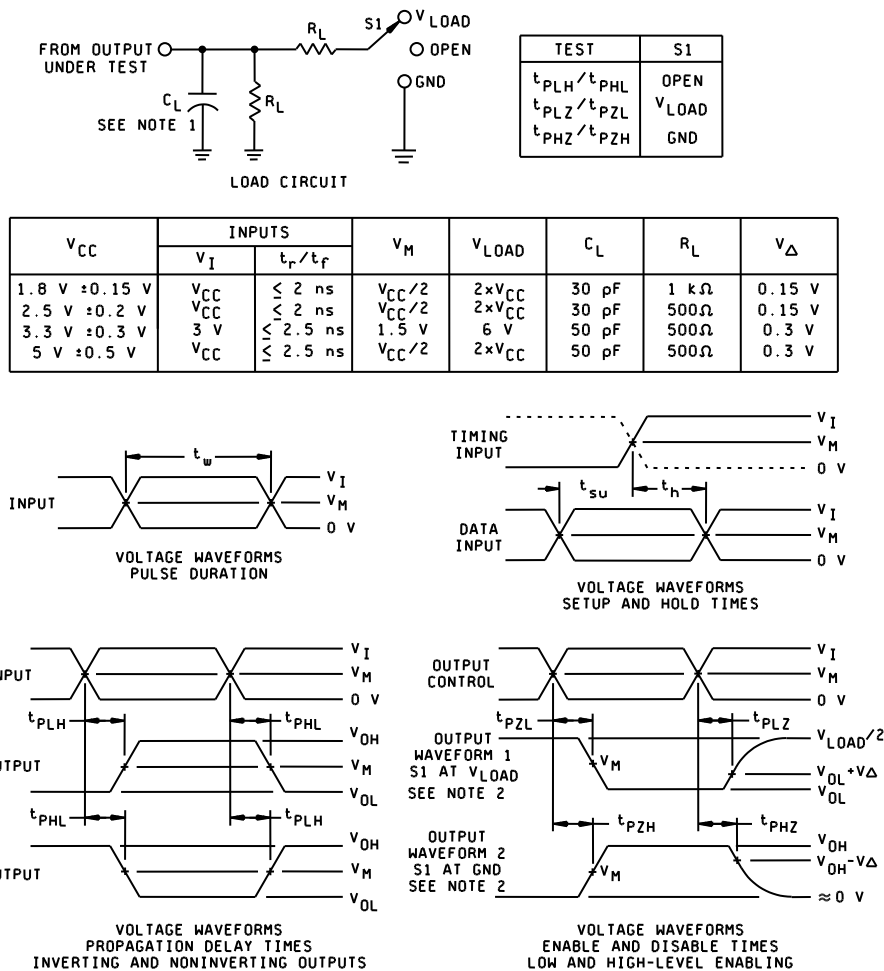


FIGURE 3. Logic diagram.

Inputs		Output
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q ₀

FIGURE 4. Function Table

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Notes:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and switching waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-side marking <u>2/</u>
V62/05621-01XE	01295	SN74LVC1G79WDCKREP	CR_

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ The actual top-side marking has one additional character that designates the assembly/test site.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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