REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. Update boilerplate to current revision. - CFS	06-12-15	Thomas M. Hess
B	Correct circuit function descriptions in paragraph 1.2.1 to accurately describe devices. - CFS	07-05-18	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	13-10-28	Thomas M. Hess
D	Add Mode of transportation and quantity column to paragraph 6.3. Update document paragraphs to current requirements. - ro	20-08-13	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**	D	D	D	D	D	D	D	D	D	D	D	D	D	D			
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-09-29	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 400 MSPS DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/05619**
	REV **D**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V058-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 14 bit, 400 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DAC5675-EP	14 bit, 400 MSPS digital to analog converter
02	DAC5675-EP	14 bit, 400 MSPS digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic quad flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:

AV_{DD}	-0.3 V to +3.6 V 2/
DV_{DD}	-0.3 V to +3.6 V 3/
AV_{DD} to DV_{DD}	-3.6 V to +3.6 V
Voltage between AGND and DGND	-0.3 V to +0.5 V
CLK, CLKC	-0.3 V to AV_{DD} +0.3 V 2/
Digital input D[13…0]A, D[13…0]B(3), SLEEP, DLLOFF	-0.3 V to DV_{DD} +0.3 V
IOUT1, OUT2	-1 V to AV_{DD} + 0.3 V 2/
EXTIO, BIAS	-1 V to AV_{DD} + 0.3 V 2/
Peak input current (any input)	20 mA
Peak total input current (all inputs)	-30 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds	+260°C

1.4 Recommended operating conditions. 4/

Supply voltage :

AV_{DD}	3.3 V
DV_{DD}	3.3 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1.5 Thermal characteristics.

Parameter	Symbol	Same package form without thermal pad	Thermal pad connected to PCB thermal plane
Thermal resistance, junction-to-ambient 5/ 6/	$R_{\theta JA}$	108.71°C/W	29.11°C/W
Thermal resistance, junction-to-case 5/ 6/	$R_{\theta JC}$	18.18°C/W	1.14°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Measured with respect to AGND.
3/ Measured with respect to DGND.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ Airflow is at 0 LFM (no airflow).
6/ Specified with the thermal bond pad on the backside of the package soldered to a 2 ounce CU plate PCB thermal plane.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +125°C	All	14		Bit
DC accuracy section 3/							
Integral nonlinearity	INL	T_{MIN} to T_{MAX}	-55°C to +125°C	All	-4	4.6	LSB
Differential nonlinearity	DNL	T_{MIN} to T_{MAX}	-55°C to +125°C	All	-2	2.2	LSB
Monotonicity			-55°C to +125°C	All	Monotonic 12 b level		
Analog output section							
Full scale output current	$I_{O(FS)}$		-55°C to +125°C	All	2	20	mA
Output compliance range		AV_{DD} = 3.15 V to 3.45 V, $I_{O(FS)}$ = 20 mA	-55°C to +125°C	All	AV_{DD} - 1	AV_{DD} +0.3	V
Offset error			+25°C	All	0.01 typical		%/FSR
Gain error		Without internal reference	-55°C to +125°C	All	-10	10	%/FSR
		With internal reference			-10	10	
Output resistance			+25°C	All	300 typical		kΩ
Output capacitance			+25°C	All	5 typical		pF
Reference output section							
Reference voltage	$V_{(EXTIO)}$		-55°C to +125°C	All	1.17	1.29	V
Reference output current 4/			+25°C	All	100 typical		nA
Reference input section							
Input reference voltage	$V_{(EXTIO)}$		-55°C to +125°C	All	0.6	1.25	V
Input resistance	R_{IN}		+25°C	All	1 typical		MΩ
Small signal resistance	SSBW		+25°C	All	1.4 typical		MHz
Input capacitance	C_{IN}		+25°C	All	100 typical		pF
Temperature coefficients section							
Offset drift			+25°C	All	12 typical		ppm of FSR/°C
Reference voltage drift	$\Delta V_{(EXT10)}$		+25°C	All	±50 typical		ppm/°C
Power supply section							
Analog supply voltage	AV_{DD}		-55°C to +125°C	All	3.15	3.6	V
Digital supply voltage	DV_{DD}		-55°C to +125°C	All	3.15	3.6	V
Analog supply current	$I_{(AVDD)}$	5/	+25°C	All	115 typical		mA
Digital supply current	$I_{(DVDD)}$	5/	+25°C	All	85 typical		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section – continued.							
Power dissipation	P_D	Sleep mode	+25°C	All	18 typical		mW
		AV_{DD} = 3.3 V, DV_{DD} = 3.3 V	-55°C to +125°C			900	
Analog and digital power supply rejection ratio	APSRR	AV_{DD} = 3.15 to 3.45 V	-55°C to +125°C	All	-0.9	0.9	%FSR /V
	DPSRR				-0.9	0.9	
Analog output section							
Output update rate	f_{CLK}		-55°C to +125°C	All		400	MSPS
Output settling time to 0.1%	$t_{S(DAC)}$	Transition: code x2000 to X23FF	+25°C	All	12 typical		ns
Output propagation delay	t_{PD}		+25°C	All	1 typical		ns
Output rise time, 10% to 90%	$t_{r(IOUT)}$		+25°C	All	2 typical		ns
Output fall time, 90% to 10%	$t_{f(IOUT)}$		+25°C	All	2 typical		ns
Output noise		$IOUT_{FS}$ = 20 mA	+25°C	All	55 typical		pA /$\sqrt{\text{Hz}}$
		$IOUT_{FS}$ = 2 mA			30 typical		
AC linearity section							
Total harmonic distortion	THD	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz	+25°C	All	73 typical		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			72 typical		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			68 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 20.1 MHz			72 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz			71 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 140 MHz			58 typical		
Spurious free dynamic range to Nyquist	SFDR	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz	+25°C	All	73 typical		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			73 typical		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			70 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 20.1 MHz			73 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz			74 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 140 MHz			60 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC linearity section – continued.							
Spurious free dynamic range within a window, 5 MHz span	SFDR	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz	+25°C	All	88 typical		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			87 typical		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			82 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 20.1 MHz			87 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz			82 typical		
		f_{CLK} = 400 MSPS, f_{OUT} = 140 MHz			75 typical		
Adjacent channel power ratio WCDMA with 3.84 MHz BW, 5 MHz channel spacing	ACPR	f_{CLK} = 122.88 MSPS, 6/ IF = 30.72 MHz	+25°C	All	73 typical		dBc
		f_{CLK} = 245.76 MSPS, 7/ IF = 61.44 MHz			71 typical		
		f_{CLK} = 399.32 MSPS, 8/ IF = 153.36 MHz			65 typical		
Two tone intermodulation to Nyquist (each tone at -6 dBfs)	IMD	f_{CLK} = 400 MSPS, f_{OUT1} = 70 MHz, f_{OUT2} = 71 MHz	+25°C	All	73 typical		dBc
		f_{CLK} = 400 MSPS, f_{OUT1} = 140 MHz, f_{OUT2} = 141 MHz			62 typical		
Four tone intermodulation, 15 MHz span, missing center tone (each tone at -16 dBfs)	IMD	f_{CLK} = 156 MSPS, f_{OUT} = 15.6 MHz, 15.8 MHZ, 16.2 MHZ, 16.4 MHZ	+25°C	All	82 typical		dBc
		f_{CLK} = 400 MSPS, f_{OUT} = 68.1 MHz, 69.3 MHZ, 71.2 MHZ, 72 MHZ			74 typical		
LVDS interface section: nodes D[13…0]A, D[13…0]B							
Positive going differential input voltage threshold	V_{ITH+}	See LVDS min/max threshold voltages table	+25°C	All	100 typical		mV
Negative going differential input voltage threshold	V_{ITH-}	See LVDS min/max threshold voltages table	+25°C	All	-100 typical		mV
Internal termination impedance	Z_T		-55°C to +125°C	All	90	132	Ω
Input capacitance	C_I		+25°C	All	2 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
CMOS interface (SLEEP) section							
High level input voltage	V_{IH}		-55°C to +125°C	All	2		V
Low level input voltage	V_{IL}		-55°C to +125°C	All		0.8	V
High level input current	I_{IH}		-55°C to +125°C	All	-100	100	µA
Low level input current	I_{IL}		-55°C to +125°C	All	-10	10	µA
Input capacitance	C_I		+25°C	All	2 typical		pF
Clock interface (CLK, CLKC) section							
Clock differential input voltage	|CLK-CLKC|		-55°C to +125°C	All	0.4	0.8	V_{PP}
Clock pulse width high	$t_{W(H)}$		+25°C	All	1.25 typical		ns
Clock pulse width low	$t_{W(L)}$		+25°C	All	1.25 typical		ns
Clock duty cycle			-55°C to +125°C	All	40	60	%
Common mode voltage range	V_{CM}		+25°C	All	2 ±20% typical		V
Input resistance		Node CLK, CLKC	+25°C	All	670 typical		Ω
Input capacitance		Node CLK, CLKC	+25°C	All	2 typical		pF
Input resistance		Differential	+25°C	All	1.3 typical		kΩ
Input capacitance		Differential	+25°C	All	1 typical		pF
Timing section							
Input setup time	t_{SU}		+25°C	All	1.5 typical		ns
Input hold time	t_H		+25°C	All	0.25 typical		ns
Input latch pulse high time	t_{LPH}		+25°C	All	2 typical		ns
Digital delay time	t_{DD}	DLL disabled, DLLOFF = 1	+25°C	All	3 typical		clk

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer-coupled output, and 50 Ω doubly terminated load.

3/ Measured differential at I_{OUT1} and I_{OUT2}; 25 Ω to AV_{DD}.

4/ Use an external buffer amplifier with high impedance input to drive any external load.

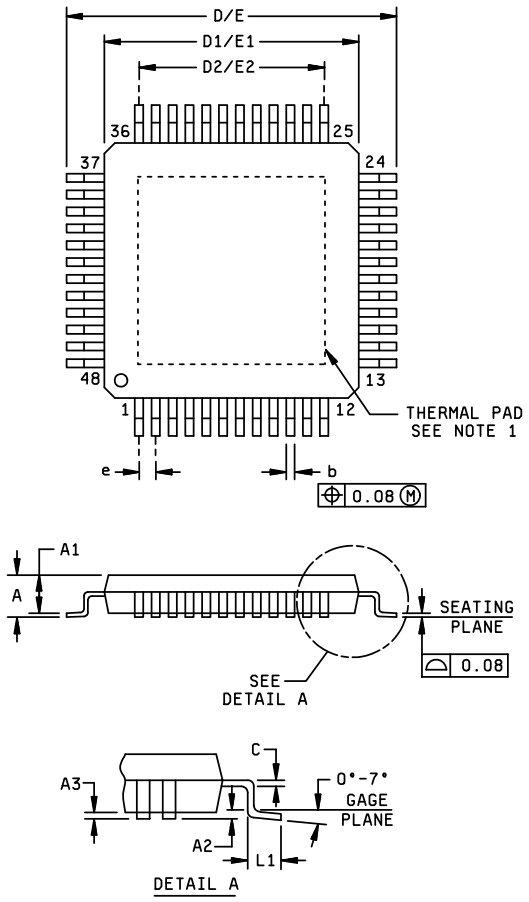
5/ Measured at f_{CLK} = 400 MSPS and f_{OUT} = 70 MHz.

6/ See figure 5.

7/ See figure 6.

8/ See figure 7.

Case outline X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.047		1.20	D1	0.267	0.283	6.80	7.20
A1	0.037	0.041	0.95	1.05	D2	0.216	---	5.50	---
A2	0.009	---	0.25	---	E	0.346	0.362	8.80	9.20
A3	0.001	0.005	0.05	0.15	E1	0.267	0.283	6.80	7.20
b	0.006	0.010	0.17	0.27	E2	0.216	---	5.50	---
c	0.005 NOM		0.13 NOM		e	0.019 NOM		0.50 NOM	
D	0.346	0.362	8.80	9.20	L1	0.017	0.029	0.45	0.75

NOTES:
1. The package is designed to be soldered to a thermal pad on the board. Refer to technical brief, thermal enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout.
2. Controlling dimensions are millimeter, inch dimensions are given for reference only.
3. Body dimensions do not include mold flash or protrusion.
4. Fall within JEDEC MS-026.

FIGURE 1. Case outlines.

Case outline X

Device type	All						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D13A	13	D7A	25	D5A	37	SLEEP
2	D13B	14	D7B	26	D5B	38	NC
3	D12A	15	DV_{DD}	27	D4A	39	BIASJ
4	D12B	16	DGND	28	D4B	40	EXTIO
5	D11A	17	DV_{DD}	29	D3A	41	AGND
6	D11B	18	DGND	30	D3B	42	AV_{DD}
7	D10A	19	AGND	31	D2A	43	IOUT1
8	D10B	20	AV_{DD}	32	D2B	44	IOUT2
9	D9A	21	CLKC	33	D1A	45	AV_{DD}
10	D9B	22	CLK	34	D1B	46	AGND
11	D8A	23	D6A	35	D0A	47	AGND
12	D8B	24	D6B	36	D0B	48	AV_{DD}

FIGURE 2. Terminal connections.

Terminal	I/O	Description
AGND	I	Analog negative supply voltage (ground); pin 47 internally connected to thermal pad.
AV_{DD}	I	Analog positive supply voltage
BIASJ	O	Full scale output current bias.
CLK	I	External clock input
CLKC	I	Complementary external clock input
D13A – D0A	I	LVDS positive input, data bits 0 through 13. D13A is the most significant data bit (MSB). D0A is the least significant data bit (LSB).
D13B – D0B	I	LVDS negative input, data bits 0 through 13. D13B is the most significant data bit (MSB). D0B is the least significant data bit (LSB).
DGND	I	Digital negative supply voltage (ground).
NC	---	Not connected in chip. Can be high or low.
DV_{DD}	I	Digital positive supply voltage.
EXTIO	I/O	Internal reference output or external reference input. Requires a 0.1 μF decoupling capacitor to AGND when used as reference output.
IOUT1	O	DAC current output. Full scale when all input bits are set 1. Connect the reference side of the DAC load resistors to AV_{DD}.
IOUT2	O	DAC complementary current output. Full scale when all input bits are 0. Connect the reference side of the DAC load resistors to AV_{DD}.
SLEEP	I	Asynchronous hardware power down input. Active high. Internal pull down.

FIGURE 2. Terminal connections – Continued.

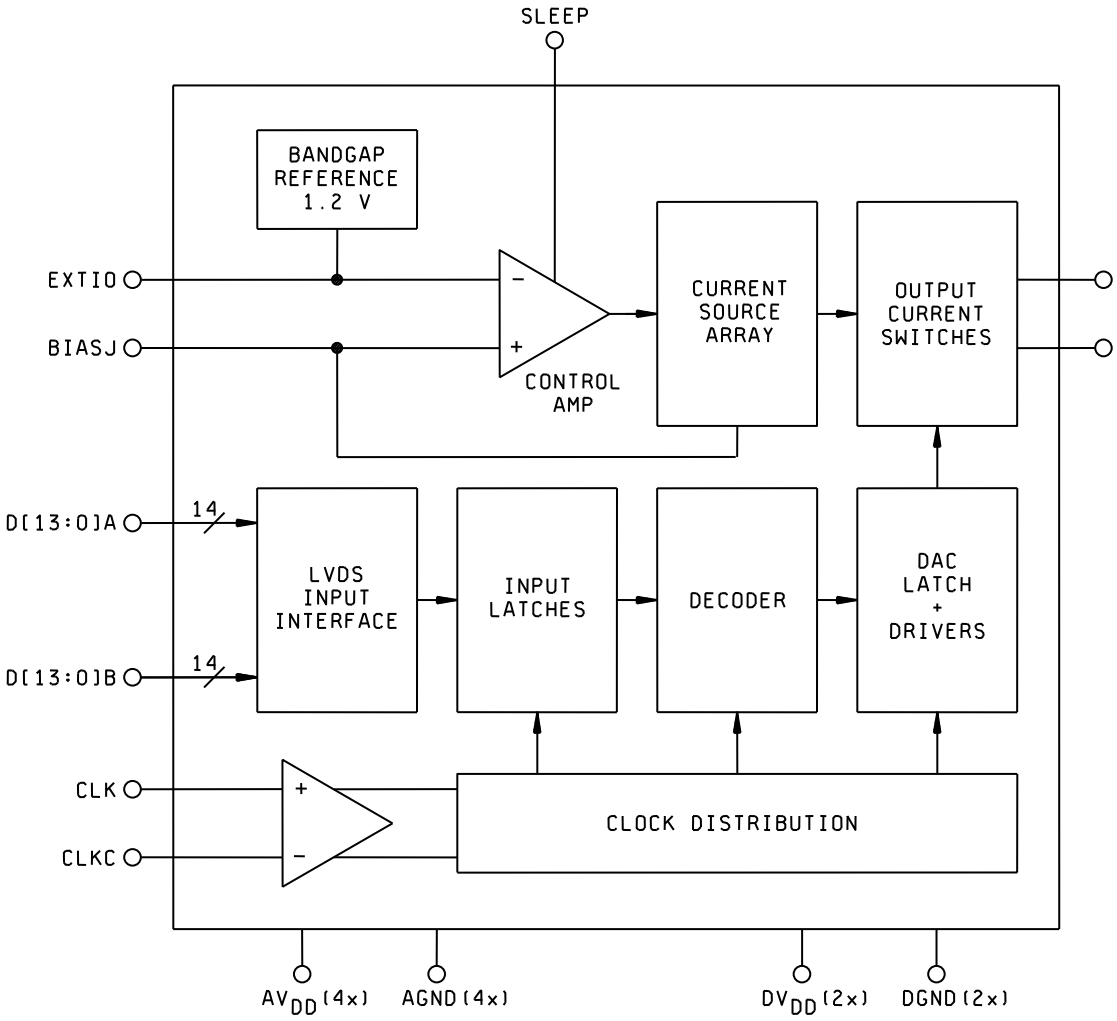


FIGURE 3. Block diagram.

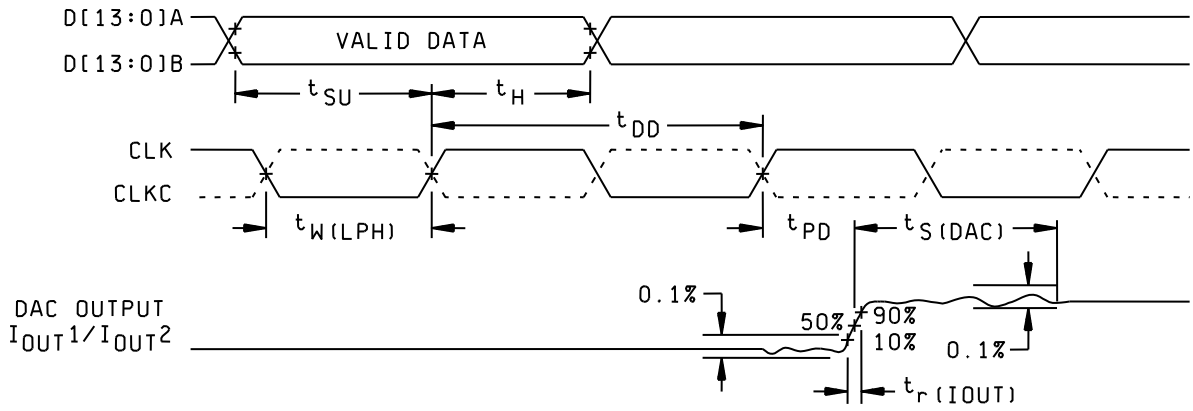


FIGURE 4. Timing waveforms.

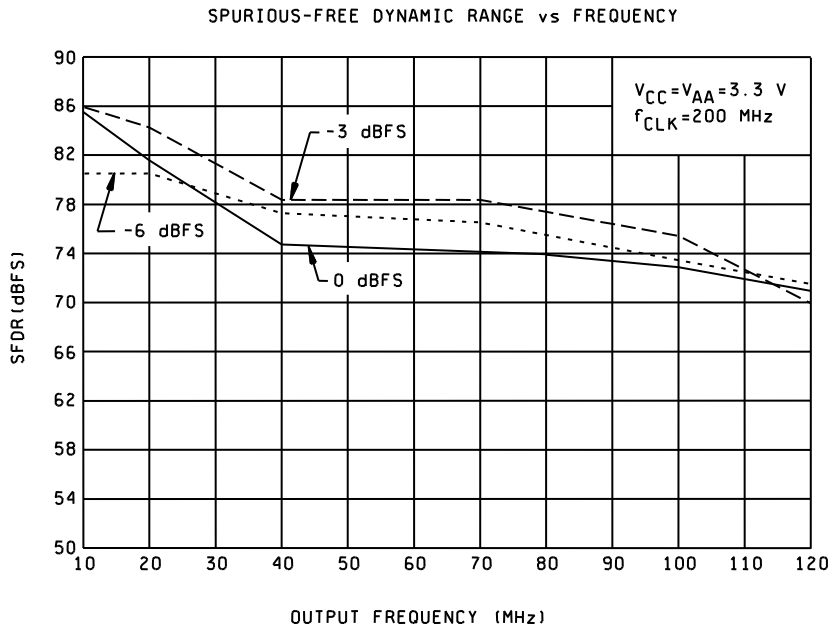


FIGURE 5. Spurious free dynamic range versus frequency.

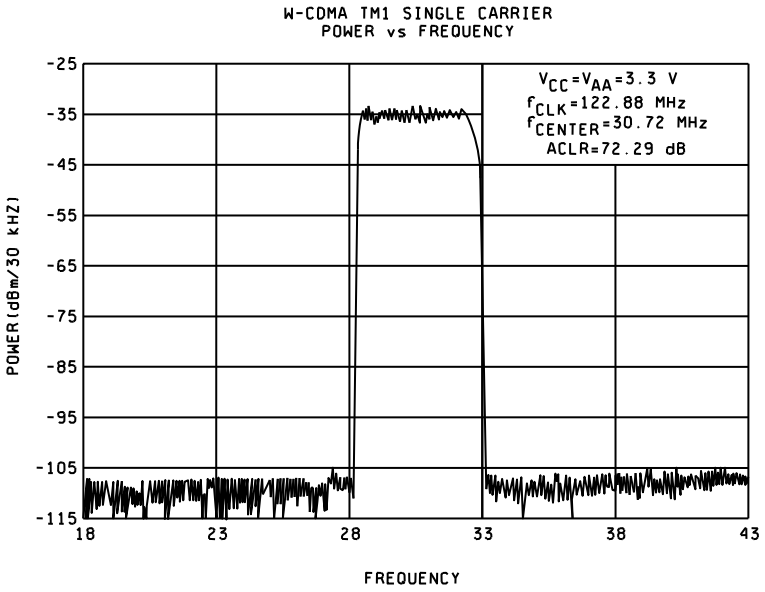


FIGURE 6. Power versus frequency.

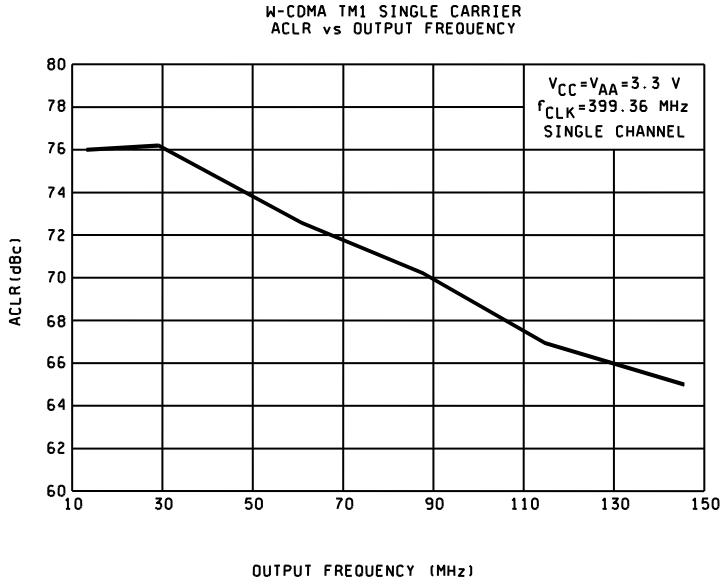


FIGURE 7. ACLR versus output frequency.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package designator	Mode of transportation and quantity	Top side marking	Vendor part number
V62/05619-01XE	01295	PHP	Tape and reel, 1000	DAC5675-EP	DAC5675MPHPREP
V62/05619-02XE	01295	PHP	Tray, 250	DAC5675-EP	DAC5675MPHPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243