

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct lead finish for device 01 on last page. - CFS	05-12-02	Thomas M. Hess
B	Update paragraph 6.3, device -02XA is no longer available. Update paragraphs to current requirements. - ro	13-12-16	Charles F. Saffle

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

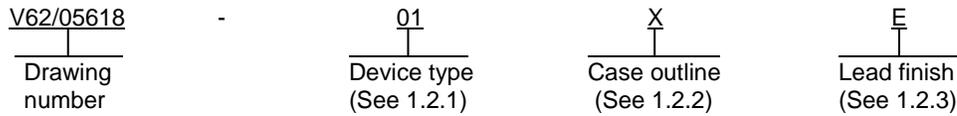
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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B								
	PAGE	1	2	3	4	5	6	7	8	9	10									

PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 05-09-01	CHECKED BY TOM HESS	TITLE MICROCIRCUIT, DIGITAL, TEMPERATURE SENSOR, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/05618
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance temperature sensor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TMP100-EP	Temperature sensor
02	TMP101-EP	Temperature sensor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	MO-178-AB	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V+)	7.5 V
Input voltage range (V _{IN})	-0.5 V to 7.5 V
Operating free-air temperature range (T _A)	-55°C to +125°C
Storage temperature range (T _{STG})	-60°C to 150°C
Maximum junction temperature (T _J)	150°C
Leading temperature soldering	300°C
Thermal resistance, junction to ambient (θ _{JA})	165°C/W 2/

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The thermal impedance, θ_{JA} for the DBV package is determined for JEDEC high-K PCB (JESD 51-7).

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1.4 Recommended operating conditions. 3/

Supply voltage range (V+) 2.7 V to 5.5 V
Operating free-air temperature range (T_A) -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- EIA/JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Temperature input section							
Range			-55°C to +125°C	01, 02	-55	+125	°C
Accuracy (temperature error)			-25°C to +85°C	01, 02		±2	°C
			-55°C to +125°C			±3	
Resolution		Selectable	-55°C to +125°C	01, 02	±0.0625 typical		°C
Digital input/output section							
High level input voltage	V_{IH}		-55°C to +125°C	01, 02	0.7 (V+)	(V+) +0.5	V
Low level input voltage	V_{IL}		-55°C to +125°C	01, 02	-0.5	0.3 (V+)	V
Input current	I_{IN}	$V_{IN} = 0 \text{ V to } 6 \text{ V}$	-55°C to +125°C	01, 02		1	µA
Low level output voltage	V_{OL}	$I_{OL} = 3 \text{ mA, SDA pin}$	-55°C to +125°C	01, 02	0	0.4	V
		$I_{OL} = 4 \text{ mA, ALERT pin}$	-55°C to +125°C	02	0	0.4	
Resolution		Selectable	-55°C to +125°C	01, 02	9 to 12 typical		bits
Conversion time		9 bit	-55°C to +125°C	01, 02		75	ms
		10 bit	-55°C to +125°C			150	
		11 bit	-55°C to +125°C			300	
		12 bit	-55°C to +125°C			600	
Conversion time		9 bit	-55°C to +125°C	01, 02	25 typical		s/s
		10 bit	-55°C to +125°C		12 typical		
		11 bit	-55°C to +125°C		6 typical		
		12 bit	-55°C to +125°C		3 typical		

See footnote at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
Quiescent current	I_Q	Serial bus inactive	-55°C to +125°C	01, 02		75	μA
		Serial bus active, SCL = 400 kHz	-55°C to +125°C		70 typical		
		Serial bus active, SCL = 3.4 MHz	-55°C to +125°C		150 typical		
Shutdown current	I_{SD}	Serial bus inactive	-55°C to +125°C	01, 02		1	μA
		Serial bus active, SCL = 400 kHz	-55°C to +125°C		20 typical		
		Serial bus active, SCL = 3.4 MHz	-55°C to +125°C		100 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X

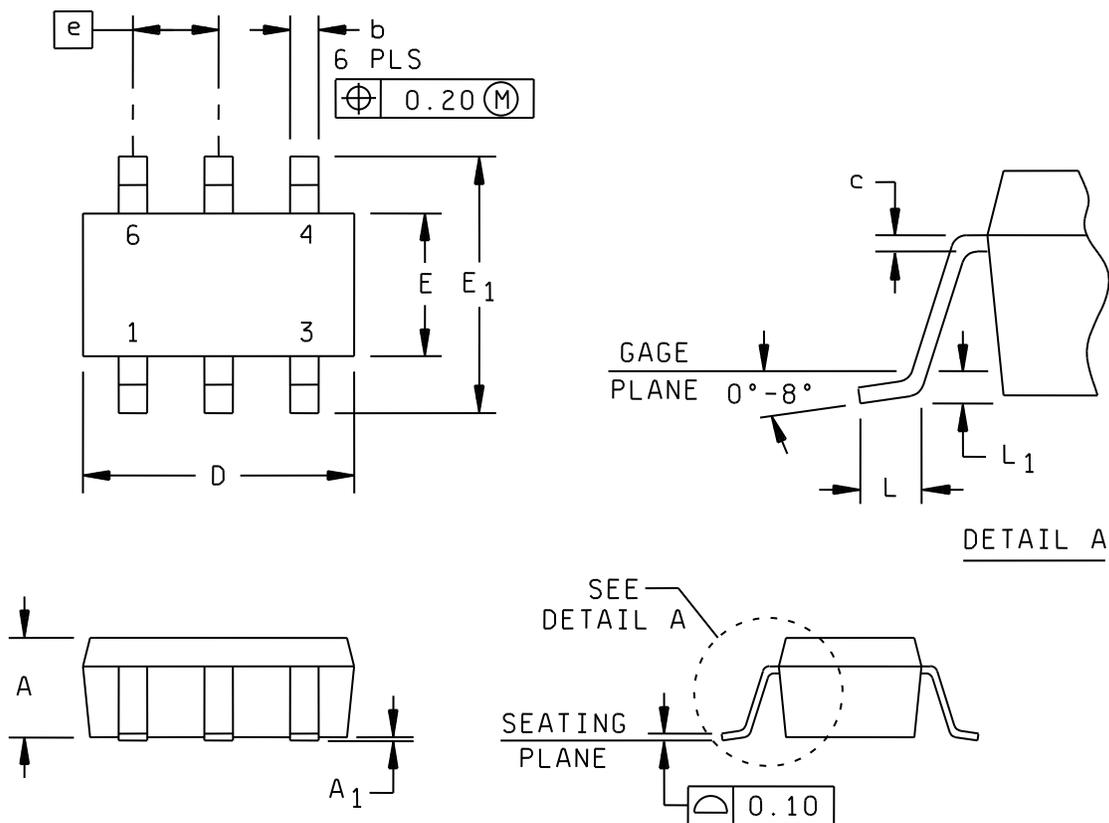


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05618</p>
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.057	---	1.45
A1	0.000	0.005	0.00	0.15
b	0.009	0.019	0.25	0.50
c	0.003	0.008	0.08	0.22
D	0.108	0.120	2.75	3.05
E	0.057	0.068	1.45	1.75
E1	0.102	0.118	2.60	3.00
e	0.037 BSC		0.95 BSC	
L	0.011	0.021	0.30	0.55
L1	0.009 NOM		0.25 NOM	
n	6		6	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
4. Falls within JEDEC MO-178 variation AB, except minimum lead width.

FIGURE 1. Case outline – Continued.

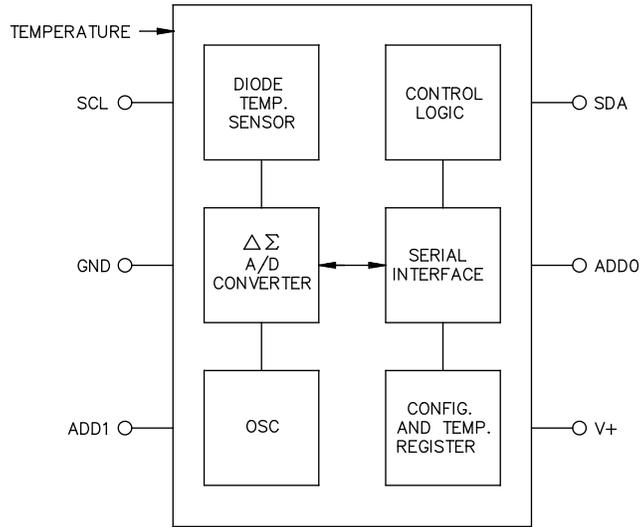
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Device types	01	02
Case outline	X	
Terminal number	Terminal symbol	
1	SCL	SCL
2	GND	GND
3	ADD1	ALERT
4	V+	V+
5	ADD0	ADD0
6	SDA	SDA

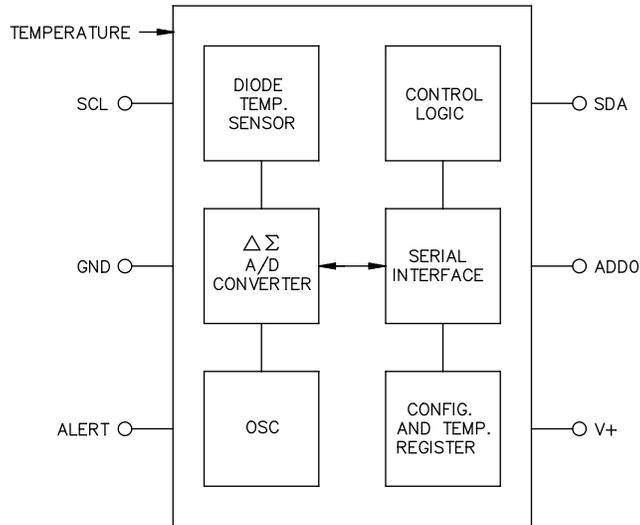
Terminal symbol	I/O	Description
SCL	I	Serial clock.
GND	---	Ground.
ADD1	I	Slave address select pin 1.
ALERT	O	Alert status pin.
V+	---	Supply voltage.
ADD0	I	Slave address select pin 0.
SDA	I/O	Serial data.

FIGURE 2. Terminal connections.

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DEVICE TYPE 01



DEVICE TYPE 02

FIGURE 3. Logic diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package <u>2/</u>	Top-side marking	Vendor part number
V62/05618-01XE	01295	SOT23	100E	TMP100MDBVREP
V62/05618-02XA	<u>3/</u>	SOT23-6 (DBV)	101E	TMP101MDBVREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available from the manufacturer. Available in reel of 3000.

3/ Not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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